

## Description

The RLSO8A2.84LV series of transient voltage suppressors are designed to protect low voltage, state-of-the-art CMOS semiconductors from transients caused by electrostatic discharge (ESD), cable discharge events (CDE), lightning and other induced voltage surges.

The devices are constructed using Semtech's proprietary EPD process technology. The EPD process provides low standoff voltages with significant reductions in leakage currents and capacitance over siliconavalanche diode processes. The RLSO8A2.84LV features integrated low capacitance compensation diodes that reduce the typical capacitance to 5pF per line. This, combined with low leakage current, means signal integrity is preserved in high-speed applications such as 10/100 Ethernet.

The RLSO8A2.84LV is in an SO-8 package and may be used to protect two high-speed line pairs. The "flow-thru" design minimizes trace inductance and reduces voltage overshoot associated with ESD events. The low clamping voltage of the RLSO8A2.84LV minimizes the stress on the protected IC.

The RLSO8A2.84LV series TVS diodes will meet the surge requirements of IEC 61000-4-2, Level 4.

## Features

- 400 Watts peak pulse power ( $t_p = 8/20\mu s$ )
- Transient protection for high speed data lines to IEC 61000-4-2 (ESD)  $\pm 15kV$  (air),  $\pm 8kV$  (contact) IEC 61000-4-4 (EFT) 40A (5/50ns) IEC 61000-4-5 (Lightning) 24A (8/20 $\mu s$ )
- Protects two line pairs (four lines)
- Comprehensive pin out for easy board layout
- Low capacitance
- Low leakage current
- Low operating and clamping voltages
- Solid-state EPD TVS process technology

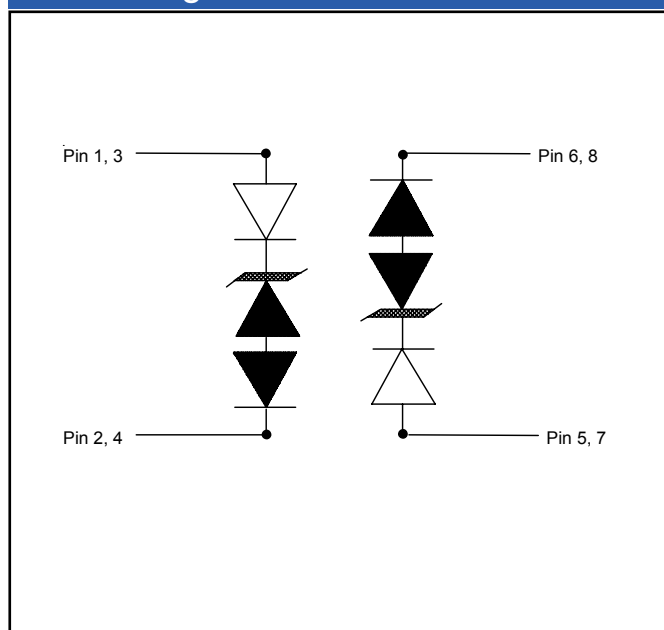
## Mechanical Characteristics

- JEDEC SO-8 package
- Molding compound flammability rating: UL 94V-0
- Marking : Part number, date code, logo
- Packaging : Tape and Reel

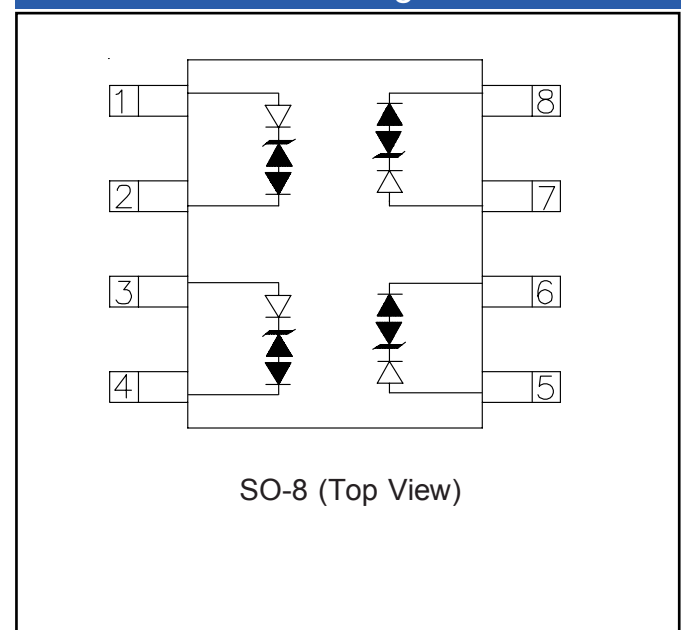
## Applications

- 10/100 Ethernet
- WAN/LAN Equipment
- Switching Systems
- Desktops, Servers, and Notebooks
- Instrumentation
- Base Stations
- Analog Inputs

## Circuit Diagram



## Schematic & PIN Configuration



## Protection Products

### Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	$P_{PK}$	400	Watts
Peak Pulse Current ( $t_p = 8/20\mu s$ )	$I_{PP}$	24	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	$V_{ESD}$	25 15	kV
Lead Soldering Temperature	$T_K$	260 (10 sec.)	°C
Operating Temperature	$T_J$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

### Electrical Characteristics

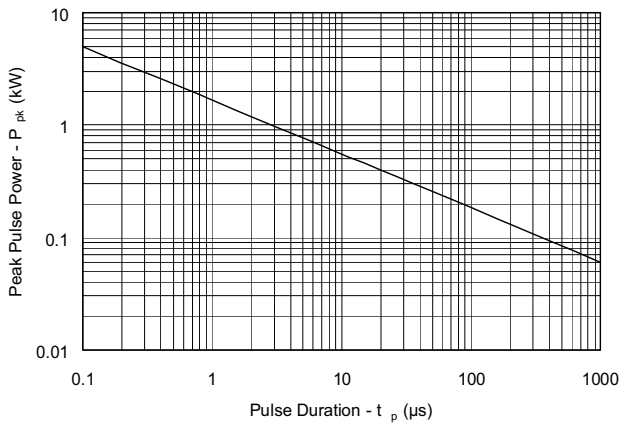
#### RLSO8A2.84LV

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$	-	-	-	2.8	V
Punch-Through Voltage	$V_{PT}$	$I_{PT}=2\mu A$	3.0	-	-	V
Snap-Back Voltage	$V_{SB}$	$I_{SB}=50mA$	2.8	-	-	V
Reverse Leakage Current	$I_R$	$V_{RWM}=2.8V, T=25^\circ C$ (Each Line)	-	-	1	$\mu A$
Clamping Voltage	$V_C$	$I_{PP}=1A, t_p = 8/20\mu s$ (Each Line)	-	-	5.5	V
Clamping Voltage	$V_C$	$I_{PP}=5A, t_p = 8/20\mu s$ (Each Line)	-	-	8.5	V
Clamping Voltage	$V_C$	$I_{PP}=24A, t_p = 8/20\mu s$ (Each Line)	-	-	15	V
Junction Capacitance	$C_j$	$V_R = 0V, f = 1MHz$ (Each Line)	-	5	-	pF

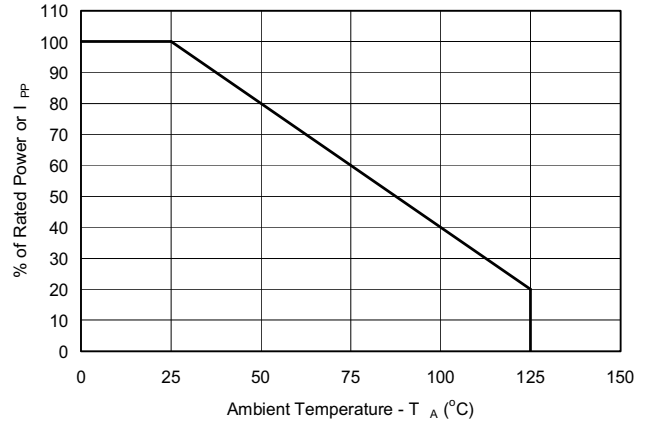
# Protection Products

## Typical Characteristics

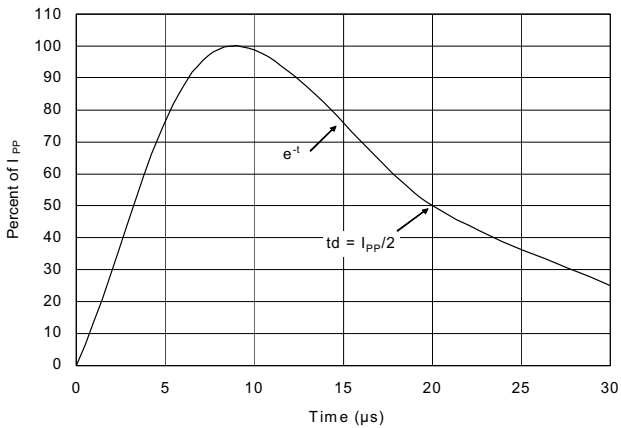
Non-Repetitive Peak Pulse Power vs. Pulse Time



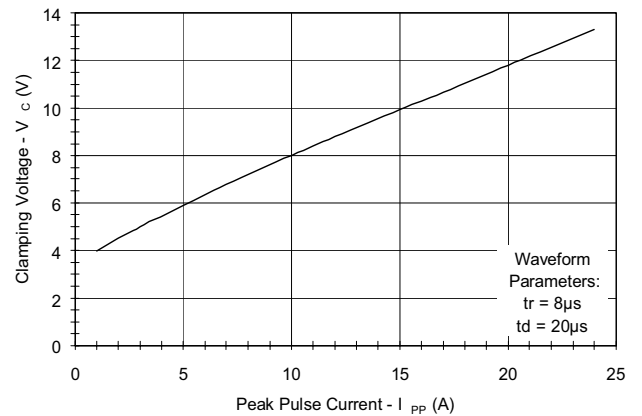
Power Derating Curve



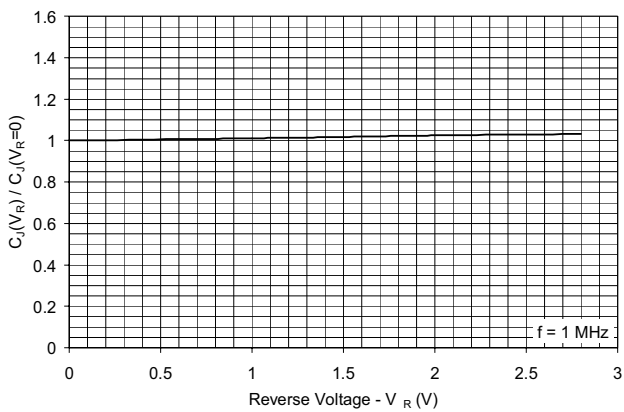
Pulse Waveform



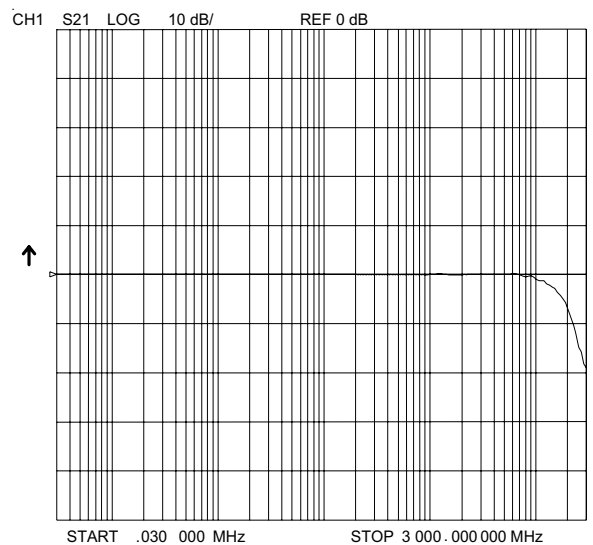
Clamping Voltage vs. Peak Pulse Current



Normalized Capacitance vs. Reverse Voltage

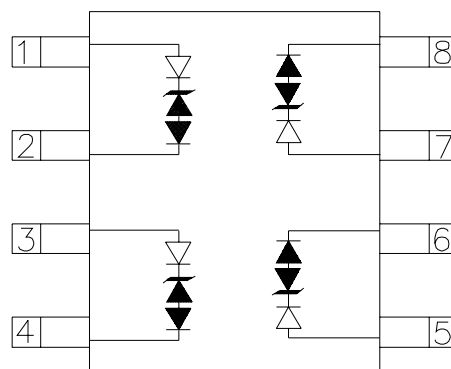


Insertion Loss S21



**Device Connection for Protection of Four Data Lines** Electronic equipment is susceptible to transient disturbances from a variety of sources including: ESD to an open connector or interface, direct or nearby lightning strikes to cables and wires, and charged cables “hot plugged” into I/O ports. The RLSO8A2.84LV is designed to protect sensitive components from damage and latchup which may result from such transient events. The RLSO8A2.84LV can be configured to protect two high-speed line pairs. The device is connected as follows:

1. Protection of two high-speed line pairs:  
The RLSO8A2.84LV is designed such that the data lines are routed through the device. The first line pair enters at pins 1 and 2 and exit at pins 8 and 7 respectively. The second line pair enters at pins 3 and 4 and exits at pins 6 and 5. The traces must be connected at the bottom of the device as shown.

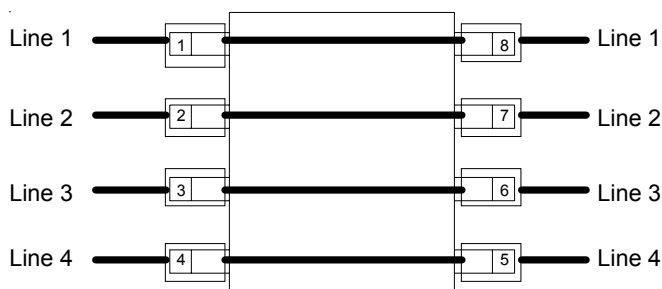


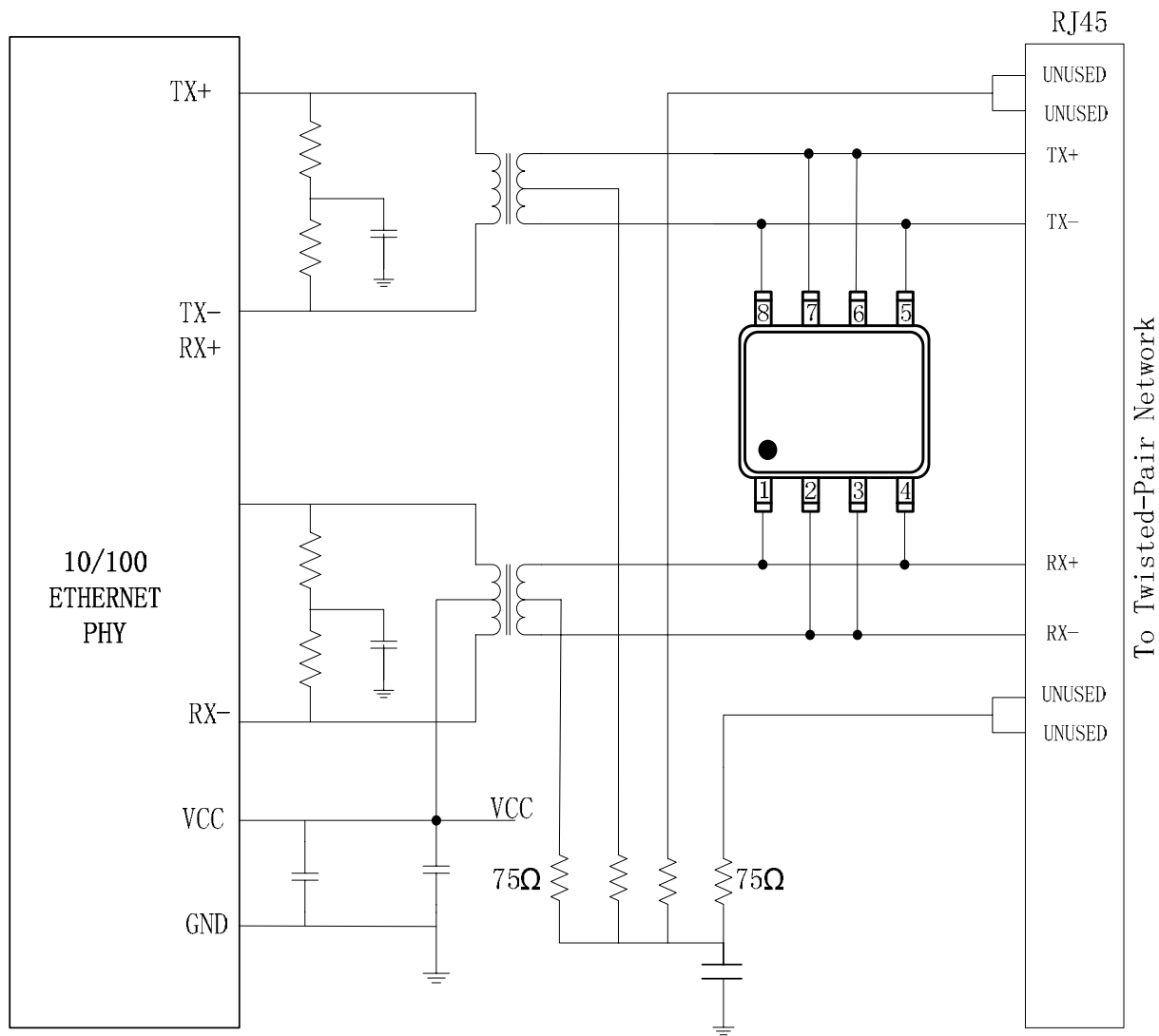
### Circuit Board Layout Recommendations for Suppression of ESD.

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- \* Place the RLSO8A2.84LV near the input terminals or connectors to restrict transient coupling.
- \* Minimize the path length between the TVS and the protected line.
- \* Minimize all conductive loops including power and ground loops.
- \* The ESD transient return path to ground should be kept as short as possible.
- \* Never run critical signals near board edges.
- \* Use ground planes whenever possible.

### Low Capacitance Protection of Two Differential Line Pairs





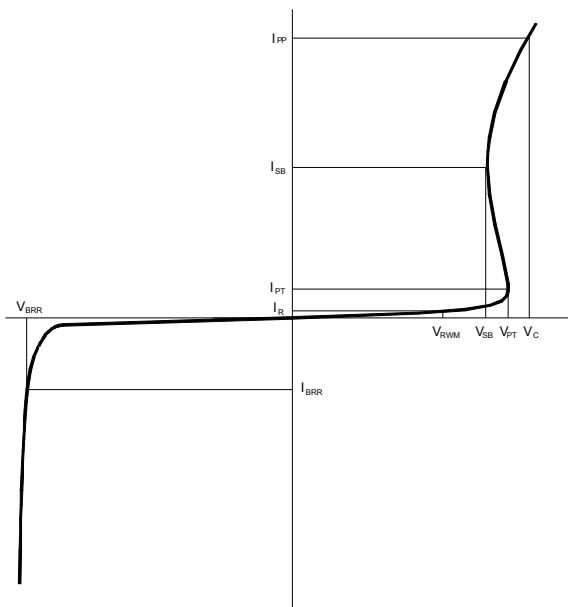
10/100 Ethernet Protection Circuit

### EPD TVS Characteristics

The RLSO8A2.84LV is constructed using Semtech's proprietary EPD technology. The structure of the EPD TVS is vastly different from the traditional pn-junction devices. At voltages below 5V, high leakage current and junction capacitance render conventional avalanche technology impractical for most applications. However, by utilizing the EPD technology, the RLSO8A2.84LV can effectively operate at 2.8V while maintaining excellent electrical characteristics.

The EPD TVS employs a complex nppn structure in contrast to the pn structure normally found in traditional silicon-avalanche TVS diodes. The EPD mechanism is achieved by engineering the center region of the device such that the reverse biased junction does not avalanche, but will "punch-through" to a conducting state. This structure results in a device with superior dc electrical parameters at low voltages while maintaining the capability to absorb high transient currents.

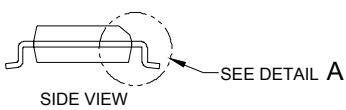
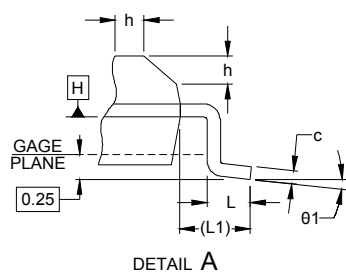
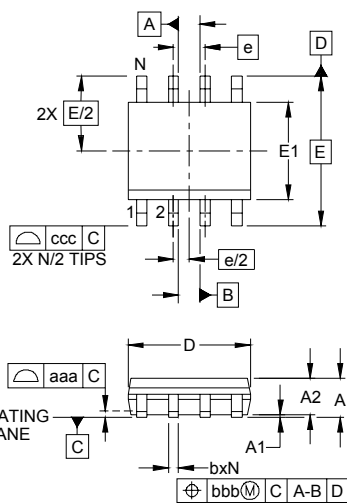
The IV characteristic curve of the EPD device is shown in Figure 1. The device represents a high impedance to the circuit up to the working voltage ( $V_{RWM}$ ). During a transient event, the device will begin to conduct as it is biased in the reverse direction. When the punchthrough voltage ( $V_{PT}$ ) is exceeded, the device enters a low impedance state, diverting the transient current away from the protected circuit. When the device is conducting current, it will exhibit a slight "snap-back" or negative resistance characteristic due to its structure. This must be considered when connecting the device to a power supply rail. To return to a non-conducting state, the current through the device must fall below the snap-back current (approximately  $< 50mA$ ).



EPD TVS IV Characteristic Curve

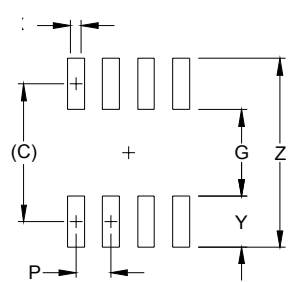
# Protection Products

## Outline Drawing - SO-8



DIM	INCHES		MILLIMETERS	
	MIN	NOM MAX	MIN	NOM MAX
A	.053	-.069	1.35	- 1.75
A1	.004	-.010	0.10	- 0.25
A2	.049	-.065	1.25	- 1.65
b	.012	-.020	0.31	- 0.51
c	.007	-.010	0.17	- 0.25
D	.189	.193 .197	4.80	4.90 5.00
E1	.150	.154 .157	3.80	3.90 4.00
E	.236 BSC		6.00 BSC	
e	.050 BSC		1.27 BSC	
h	.010	-.020	0.25	- 0.50
L	.016	.028 .041	0.40	0.72 1.04
L1	(0.041)		(1.04)	
N	8		8	
theta1	0°	- 8°	0°	- 8°
aaa	.004		0.10	
bbb	.010		0.25	
ccc	.008		0.20	

- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MS-012, VARIATION AA.



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
  2. REFERENCE IPC-SM-782A, RLP NO. 300A.

RUILONG.YUAN CO.,LTD  
Tel: +86- 0755-82908296  
Fax: +86- 0755-82908002

Email: [jack@ruilon.com](mailto:jack@ruilon.com)  
Website: <http://www.ruilon.com>

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