

4-Bit Bidirectional Voltage-Level Translator with Automatic Direction Sensing

1 FEATURES

- **No Direction-Control**
- **Data Rates**
100Mbps
- **1.2V to 3.6V on A ports and 1.65V to 5.5V on B Ports ($V_{CCA} \leq V_{CCB}$)**
- **V_{CC} Isolation Feature: If Either V_{CC} Input is at GND, Both Ports are in the High-Impedance State**
- **Output Enable (OE) Input Circuit Referenced to V_{CCA}**
- **Low Power Consumption, 10 μ A Maximum I_{CC}**
- **No Power-Supply Sequencing Required: Either V_{CCA} or V_{CCB} can be Ramped First**
- **I_{OFF} : Supports Partial-Power-Down Mode Operation**
- **Extended Temperature: -40°C to +85°C**

2 APPLICATIONS

- Handset
- Smartphone
- Tablet
- Desktop PC

3 DESCRIPTIONS

This 4-bit non-inverting translator is a bidirectional voltage-level translator and can be used to establish digital switching compatibility between mixed-voltage systems. It uses two separate configurable power-supply rails, with the A ports supporting operating voltages from 1.2V to 3.6V while it tracks the V_{CCA} supply, and the B ports supporting operating voltages from 1.65V to 5.5V while it tracks the V_{CCB} supply. This allows the support of both lower and higher logic signal levels while providing bidirectional translation capabilities between any of the 1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5V voltage nodes.

V_{CCA} must not exceed V_{CCB} .

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state, which significantly reduces the power-supply quiescent current consumption. OE has an internal pull-down current source, as long as V_{CCA} is powered.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

The RS0204 is available in Green QFN3.5x3.5-14L, QFN1.7x2-12L and TSSOP-14 packages. It operates over an ambient temperature range of -40°C to +85°C.

Device Information ⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS0204	QFN3.5x3.5-14L	3.50mmx3.50mm
	QFN2x1.7-12L	2.00mmx1.70mm
	TSSOP-14	5.00mmx4.40mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Functional Block Diagram

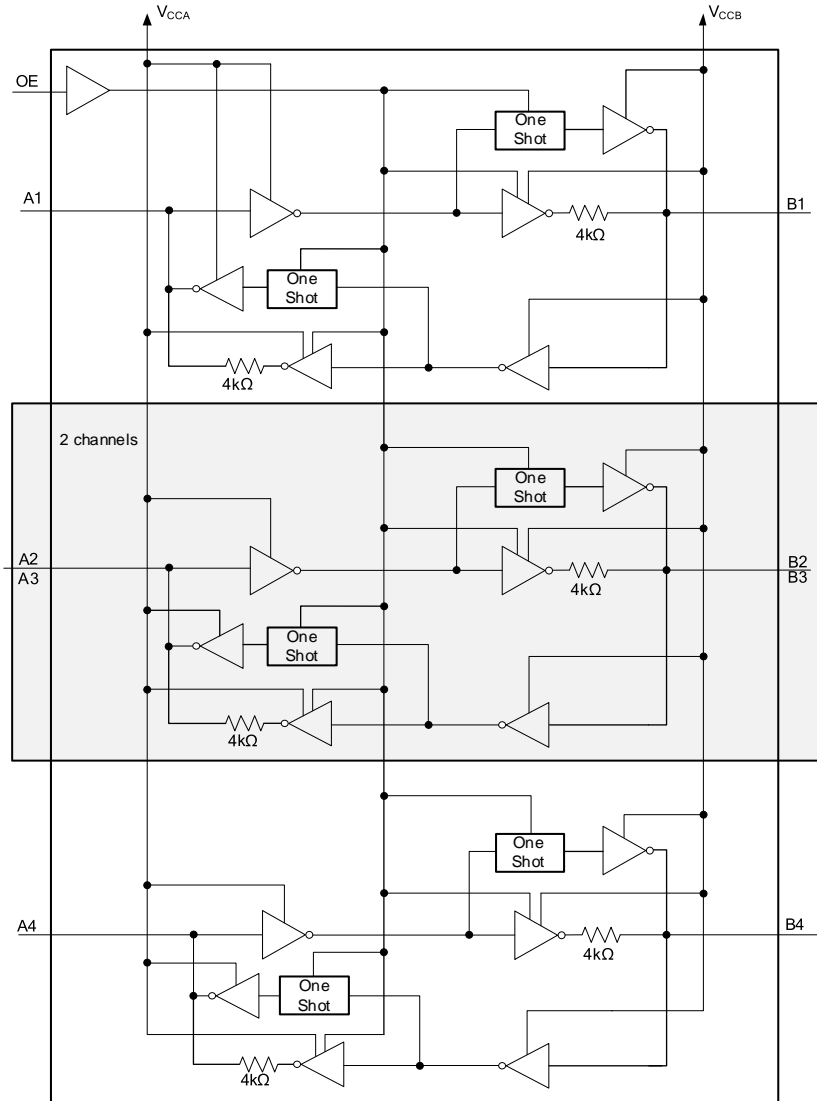


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5 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2021/01/20	Preview version completed
A.1	2021/04/27	Initial version completed
A.2	2021/05/27	Added TAPE AND REEL INFORMATION
A.3	2021/10/12	1. Change QFN3.5x3.5-14L PACKAGE OPTION @Page 9 2. Added Detailed Description and Application Information
A.4	2022/11/03	1. Change the Voltage Waveforms Enable and Disable diagram in Page 16@ A.3 Version 2. Update PACKAGE OPTION in Page 9@ A.3 Version

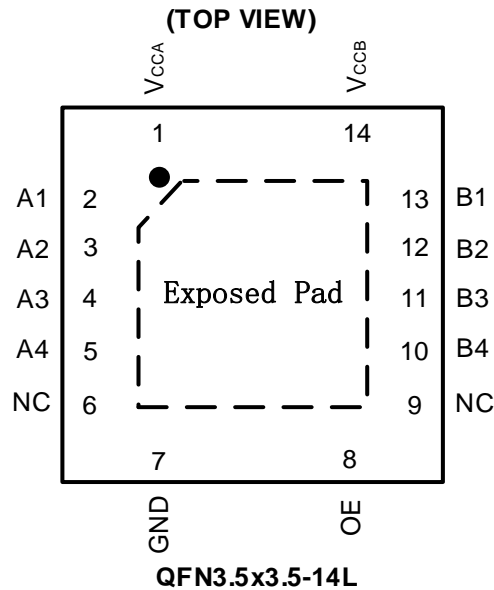
6 PACKAGE/ORDERING INFORMATION ⁽¹⁾

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING ⁽²⁾	MSL ⁽³⁾	PACKAGE OPTION
RS0204	RS0204YTQF14	-40°C ~+85°C	QFN3.5x3.5-14L	RS0204	MSL3	Tape and Reel,5000
	RS0204YUTQH12	-40°C ~+85°C	QFN1.7x2-12L	0204	MSL3	Tape and Reel,4000
	RS0204YQ	-40°C ~+85°C	TSSOP-14	RS0204	MSL3	Tape and Reel,4000

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) There may be additional marking, which relates to the lot trace code information(data code and vendor code), the logo or the environmental category on the device.
- (3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

7 PIN CONFIGURATIONS

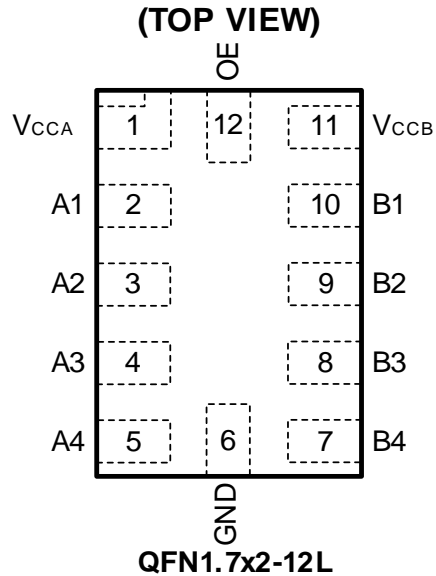


PIN DESCRIPTION

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
QFN3.5x3.5-14L			
1	V _{CCA}	P	A Port Supply Voltage. $1.2V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$.
2	A1	I/O	Input/output A1. Reference to V _{CCA} .
3	A2	I/O	Input/output A2. Reference to V _{CCA} .
4	A3	I/O	Input/output A3. Reference to V _{CCA} .
5	A4	I/O	Input/output A4. Reference to V _{CCA} .
6	NC	–	No internal connection.
7	GND	–	Ground.
8	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .
9	NC	–	No internal connection.
10	B4	I/O	Input/output B4. Reference to V _{CCB} .
11	B3	I/O	Input/output B3. Reference to V _{CCB} .
12	B2	I/O	Input/output B2. Reference to V _{CCB} .
13	B1	I/O	Input/output B1. Reference to V _{CCB} .
14	V _{CCB}	P	B Ports Supply Voltage. $1.65V \leq V_{CCB} \leq 5.5V$.
–	Exposed Pad	–	Exposed pad should be soldered to PCB board and connected to GND or left floating.

(1) I=input, O=output, I/O=input and output, P=power

PIN CONFIGURATIONS

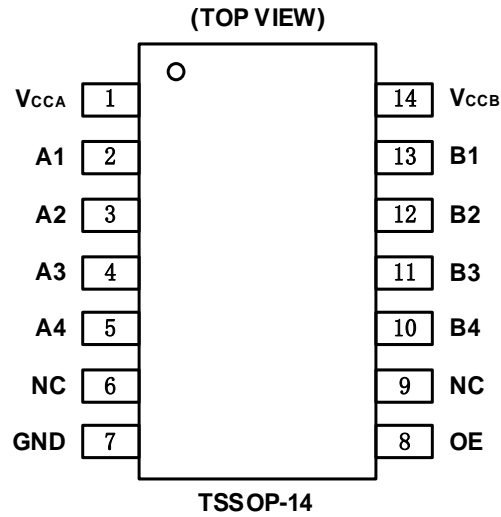


PIN DESCRIPTION

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
QFN1.7x2-12L			
1	V _{CCA}	P	A Port Supply Voltage. $1.2V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$.
2	A1	I/O	Input/output A1. Reference to V _{CCA} .
3	A2	I/O	Input/output A2. Reference to V _{CCA} .
4	A3	I/O	Input/output A3. Reference to V _{CCA} .
5	A4	I/O	Input/output A4. Reference to V _{CCA} .
6	GND	–	Ground.
7	B4	I/O	Input/output B4. Reference to V _{CCB} .
8	B3	I/O	Input/output B3. Reference to V _{CCB} .
9	B2	I/O	Input/output B2. Reference to V _{CCB} .
10	B1	I/O	Input/output B1. Reference to V _{CCB} .
11	V _{CCB}	P	B Ports Supply Voltage. $1.65V \leq V_{CCB} \leq 5.5V$.
12	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .

(1) I=input, O=output, I/O=input and output, P=power

PIN CONFIGURATIONS



PIN DESCRIPTION

PIN	NAME	TYPE ⁽¹⁾	FUNCTION
TSSOP-14			
1	V _{CCA}	P	A Port Supply Voltage. $1.2V \leq V_{CCA} \leq 3.6V$ and $V_{CCA} \leq V_{CCB}$
2	A1	I/O	Input/output A1. Reference to V _{CCA} .
3	A2	I/O	Input/output A2. Reference to V _{CCA} .
4	A3	I/O	Input/output A3. Reference to V _{CCA} .
5	A4	I/O	Input/output A4. Reference to V _{CCA} .
6	NC	-	No internal connection.
7	GND	—	Ground.
8	OE	I	Output Enable (Active High). Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .
9	NC	-	No internal connection.
10	B4	I/O	Input/output B4. Reference to V _{CCB} .
11	B3	I/O	Input/output B3. Reference to V _{CCB} .
12	B2	I/O	Input/output B2. Reference to V _{CCB} .
13	B1	I/O	Input/output B1. Reference to V _{CCB} .
14	V _{CCB}	P	B Ports Supply Voltage. $1.65V \leq V_{CCB} \leq 5.5V$.

(1) I=input, O=output, I/O=input and output, P=power

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

SYMBOL	PARAMETER		MIN	MAX	UNIT
V _{CCA}	Supply Voltage Range		-0.3	4.6	V
V _{CCB}	Supply Voltage Range		-0.3	6.5	V
V _I ⁽²⁾	Input Voltage Range	A port	-0.3	4.6	V
		B port	-0.3	6.5	
		OE	-0.3	4.6	
V _O ⁽²⁾	Voltage range applied to any output in the high-impedance or power-off state	A port	-0.3	4.6	V
		B port	-0.3	6.5	
V _O ⁽²⁾⁽³⁾	Voltage range applied to any output in the high or low state	A port	-0.3	V _{CCA} +0.3	V
		B port	-0.3	V _{CCB} +0.3	
I _{IK}	Input clamp current	V _I <0		-50	mA
I _{OK}	Output clamp current	V _O <0		-50	mA
I _O	Continuous output current			±50	mA
	Continuous current through V _{CCA} , V _{CCB} or GND			±100	mA
T _J	Junction Temperature ⁽⁴⁾		-40	150	°C
T _{stg}	Storage temperature		-65	+150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

(4) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±5000	V
		machine model (MM)	±300	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

V_{CCI} is the supply voltage associated with the input port. V_{CCO} is the supply voltage associated with the output port. ⁽¹⁾⁽²⁾

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Supply voltage	V_{CCA}		1.2		3.6	V
	V_{CCB}		1.65		5.5	
High-level input voltage (V_{IH})	A-port inputs	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	$V_{CCI} \times 0.65^{(3)}$		V_{CCI}	V
	B-port inputs	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	$V_{CCI} \times 0.65$		V_{CCI}	
	OE input	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	$V_{CCA} \times 0.65$		5.5	
Low-level input voltage (V_{IL})	A-port inputs	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	0		$V_{CCI} \times 0.35^{(3)}$	V
	B-port inputs	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	0		$V_{CCI} \times 0.35$	
	OE input	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	0		$V_{CCA} \times 0.35$	
Voltage applied to any output in the high-impedance or power-off state (V_o)	A-port	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	0		3.6	V
	B-port	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$	0		5.5	
Input transition rise or fall rate ($\Delta t/\Delta v$)	A-port inputs	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$ $V_{CCB} = 1.65\text{ V to }5.5\text{ V}$			40	ns/V
	B-port inputs	$V_{CCA} = 1.2\text{ V to }3.6\text{ V}$	$V_{CCB} = 1.65\text{ V to }3.6\text{ V}$		40	
$V_{CCB} = 4.5\text{ V to }5.5\text{ V}$				30		
T_A Operating free-air temperature			-40		85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, that is, both at V_{CCI} or both at GND.

(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.

(3) V_{CCI} is the supply voltage associated with the input port.

8.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) ⁽¹⁾ ⁽²⁾ ⁽³⁾

PARAMETER	CONDITIONS	V _{CCA}	V _{CCB}	TEMP	MIN ⁽⁴⁾	TYP ⁽⁵⁾	MAX ⁽⁴⁾	UNIT	
V _{OHA} Port A output high voltage	I _{OH} = -20 μA	1.2V		+25°C		1.1		V	
		1.4V to 3.6V		Full	V _{CCA} -0.4				
V _{OLA} Port A output low voltage	I _{OL} = 20 μA	1.2V		+25°C		0.3			
		1.4V to 3.6V		Full			0.4		
V _{OHB} Port B output high voltage	I _{OH} = -20 μA		1.65V to 5.5V	Full	V _{CCB} -0.4				
V _{OLB} Port B output low voltage	I _{OL} = 20 μA		1.65V to 5.5V	Full			0.4		
I _I Input leakage current	OE V _I =V _{CCI} or GND	1.2V to 3.6V	1.65V to 5.5V	+25°C			±1		μA
				Full			±2		
I _{off} Partial power down current	A Ports V _I or V _O =0 to 3.6V	0V	0V to 5.5V	+25°C			±1	μA	
				Full			±2		
	B Ports V _I or V _O =0 to 5.5V	0V to 3.6V	0V	+25°C			±1	μA	
				Full			±2		
I _{OZ} ⁽⁶⁾ High-impedance State output current	A or B port OE=GND	1.2V to 3.6V	1.65V to 5.5V	+25°C			±1	μA	
				Full			±2		
I _{CCA} V _{CCA} supply current	V _I =V _{CCI} or GND I _O = 0	1.2V	1.65V to 5.5V	+25°C		0.06		μA	
		1.4V to 3.6V	1.65V to 5.5V	Full			5		
		3.6V	0V	Full			2		
		0V	5.5V	Full			-2		
I _{CCB} V _{CCB} supply current	V _I =V _{CCI} or GND I _O = 0	1.2V	1.65V to 5.5V	+25°C		3.4		μA	
		1.4V to 3.6V	1.65V to 5.5V	Full			5		
		3.6V	0V	Full			-2		
		0V	5.5V	Full			2		
I _{CCA} + I _{CCB} Combined supply current	V _I = V _{CCI} or GND I _O = 0	1.2V	1.65V to 5.5V	+25°C		3.5		μA	
		1.4V to 3.6V	1.65V to 5.5V	Full			10		
I _{CCZA} V _{CCA} supply current	V _I = V _{CCI} or GND I _O = 0, OE=GND	1.2V	1.65V to 5.5V	+25°C		0.05		μA	
		1.4V to 3.6V	1.65V to 5.5V	Full			5		
I _{CCZB} V _{CCB} supply current	V _I = V _{CCI} or GND I _O = 0, OE=GND	1.2V	1.65V to 5.5V	+25°C		3.3		μA	
		1.4V to 3.6V	1.65V to 5.5V	Full			5		
C _i Input capacitance	OE	1.2V to 3.6V	1.65V to 5.5V	+25°C		4		pF	
C _{io} Input-to-output internal capacitance	A port	1.2V to 3.6V	1.65V to 5.5V	+25°C		5		pF	
	B port	1.2V to 3.6V	1.65V to 5.5V	+25°C		9			

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port

(3) V_{CCA} must be less than or equal to V_{CCB}.

(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(6) For I/O ports, the parameter I_{OZ} includes the input leakage current.

8.5 Timing Requirements:

8.5.1 $V_{CCA}=1.2V$

 $T_A=25^{\circ}C$, $V_{CCA}=1.2V$

		$V_{CCB}=1.8V$	$V_{CCB}=2.5V$	$V_{CCB}=3.3V$	$V_{CCB}=5V$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		20	20	20	20	Mbps
Pulse duration(t_w)	data inputs	50	50	50	50	ns

8.5.2 $V_{CCA}=1.5V\pm 0.1V$

 $T_A=25^{\circ}C$, $V_{CCA}=1.5V\pm 0.1V$ (unless otherwise noted)

		$V_{CCB}=1.8V \pm 0.15V$	$V_{CCB}=2.5V \pm 0.2V$	$V_{CCB}=3.3V \pm 0.3V$	$V_{CCB}=5V \pm 0.5V$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		40	40	40	40	Mbps
Pulse duration(t_w)	data inputs	25	25	25	25	ns

8.5.3 $V_{CCA}=1.8V\pm 0.15V$

 $T_A=25^{\circ}C$, $V_{CCA}=1.8V\pm 0.15V$ (unless otherwise noted)

		$V_{CCB}=1.8V \pm 0.15V$	$V_{CCB}=2.5V \pm 0.2V$	$V_{CCB}=3.3V \pm 0.3V$	$V_{CCB}=5V \pm 0.5V$	UNIT
		TYP	TYP	TYP	TYP	
Data rate		50	50	50	50	Mbps
Pulse duration(t_w)	data inputs	25	25	25	25	ns

8.5.4 $V_{CCA}=2.5V\pm 0.2V$

 $T_A=25^{\circ}C$, $V_{CCA}=2.5V\pm 0.2V$ (unless otherwise noted)

		$V_{CCB}=2.5V \pm 0.2V$	$V_{CCB}=3.3V \pm 0.3V$	$V_{CCB}=5V \pm 0.5V$	UNIT
		TYP	TYP	TYP	
Data rate		70	80	80	Mbps
Pulse duration(t_w)	data inputs	14	12	12	ns

8.5.5 $V_{CCA}=3.3V\pm 0.3V$

 $T_A=25^{\circ}C$, $V_{CCA}=3.3V\pm 0.3V$ (unless otherwise noted)

		$V_{CCB}=3.3V \pm 0.3V$	$V_{CCB}=5V \pm 0.5V$	UNIT
		TYP	TYP	
Data rate		80	100	Mbps
Pulse duration(t_w)	data inputs	12	10	ns

8.6 Switching Characteristics: $V_{CCA}=1.2V$

 $T_A=25^{\circ}C$, $V_{CCA}=1.2V$

PARAMETER	CONDITIONS	$V_{CCB}=1.8V$	$V_{CCB}=2.5V$	$V_{CCB}=3.3V$	$V_{CCB}=5V$	UNIT	
		TYP	TYP	TYP	TYP		
t_{PHL}	Propagation delay time high-to-low output	A-to-B	27.8	21.9	20.3	26.5	ns
t_{PLH}	Propagation delay time low-to-high output	A-to-B	26	19.1	18.6	22.1	ns
t_{PHL}	Propagation delay time high-to-low output	B-to-A	36.9	37.1	37.5	36.6	ns
t_{PLH}	Propagation delay time low-to-high output	B-to-A	34.5	34.4	32.8	33.2	ns
t_{en}	Enable time	OE-to-A or B	378	387	365	348	ns
t_{dis}	Disable time	OE-to-A or B	19	16	15	16	ns
t_{rA} , t_{fA}	Input rise time	A port rise and fall time	12.3	17.1	16.5	13.1	ns
t_{rB} , t_{fB}	Input rise time	B port rise and fall time	6.6	6.5	7.6	5.1	ns
$t_{sk(O)}$	Skew(time), output	Channel-to-Channel Skew	2.4	1.6	1.9	7.1	ns
Maximum data rate			20	20	20	20	Mbps

8.7 Switching Characteristics: $V_{CCA}=1.5V \pm 0.1V$

 over recommended operating free-air temperature range, $V_{CCA}=1.5V \pm 0.1V$ (unless otherwise noted)

PARAMETER	CONDITIONS	$V_{CCB}=1.8V \pm 0.15V$	$V_{CCB}=2.5V \pm 0.2V$	$V_{CCB}=3.3V \pm 0.3V$	$V_{CCB}=5V \pm 0.5V$	UNIT	
		TYP	TYP	TYP	TYP		
t_{PHL}	Propagation delay time high-to-low output	A-to-B	15.1	15.7	12.8	11.6	ns
t_{PLH}	Propagation delay time low-to-high output	A-to-B	17.9	15.2	11.5	9.8	ns
t_{PHL}	Propagation delay time high-to-low output	B-to-A	17.4	15.3	15.1	19.6	ns
t_{PLH}	Propagation delay time low-to-high output	B-to-A	14.3	15.3	15.7	21	ns
t_{en}	Enable time	OE-to-A or B	225	218	215	216	ns
t_{dis}	Disable time	OE-to-A or B	18.4	15.7	14.2	13.7	ns
t_{rA} , t_{fA}	Input rise time	A port rise and fall time	6.2	6.1	6.1	6.2	ns
t_{rB} , t_{fB}	Input rise time	B port rise and fall time	6.6	4.4	3.7	3.1	ns
$t_{sk(O)}$	Skew(time), output	Channel-to-Channel Skew	0.7	0.7	0.6	0.6	ns
Maximum data rate			40	40	40	40	Mbps

8.8 Switching Characteristics: $V_{CCA}=1.8V \pm 0.15V$

over recommended operating free-air temperature range, $V_{CCA}=1.8V \pm 0.15V$ (unless otherwise noted)

PARAMETER	CONDITIONS	$V_{CCB}=1.8V \pm 0.15V$	$V_{CCB}=2.5V \pm 0.2V$	$V_{CCB}=3.3V \pm 0.3V$	$V_{CCB}=5V \pm 0.5V$	UNIT
		TYP	TYP	TYP	TYP	
t_{PHL} Propagation delay time high-to-low output	A-to-B	13.8	9.1	6.9	7	ns
t_{PLH} Propagation delay time low-to-high output	A-to-B	16.4	9.5	7.7	6.5	ns
t_{PHL} Propagation delay time high-to-low output	B-to-A	13.3	9.3	8.6	8.1	ns
t_{PLH} Propagation delay time low-to-high output	B-to-A	10.2	8.3	8.6	8	ns
t_{en} Enable time	OE-to-A or B	185	178	183	167	ns
t_{dis} Disable time	OE-to-A or B	18.3	13	12.1	11.2	ns
t_{rA}, t_{fA} Input rise time	A port rise and fall time	5.8	6.3	6.6	7.7	ns
t_{rB}, t_{fB} Input rise time	B port rise and fall time	6.2	4.5	3.5	3.4	ns
$t_{sk(O)}$ Skew(time), output	Channel-to-Channel Skew	0.8	0.7	0.7	0.6	ns
Maximum data rate		50	50	50	50	Mbps

8.9 Switching Characteristics: $V_{CCA}=2.5V \pm 0.2V$

over recommended operating free-air temperature range, $V_{CCA}=2.5V \pm 0.2V$ (unless otherwise noted)

PARAMETER	CONDITIONS	$V_{CCB}=2.5V \pm 0.2V$	$V_{CCB}=3.3V \pm 0.3V$	$V_{CCB}=5V \pm 0.5V$	UNIT
		TYP	TYP	TYP	
t_{PHL} Propagation delay time high-to-low output	A-to-B	6.9	5.3	4	ns
t_{PLH} Propagation delay time low-to-high output	A-to-B	8.1	6.2	4.8	ns
t_{PHL} Propagation delay time high-to-low output	B-to-A	5.5	4.6	4.2	ns
t_{PLH} Propagation delay time low-to-high output	B-to-A	1.9	4.3	4.2	ns
t_{en} Enable time	OE-to-A or B	157	147	138	ns
t_{dis} Disable time	OE-to-A or B	13.1	9.7	8.7	ns
t_{rA}, t_{fA} Input rise time	A port rise and fall time	3.5	2.9	3	ns
t_{rB}, t_{fB} Input rise time	B port rise and fall time	4	2.8	2.5	ns
$t_{sk(O)}$ Skew(time), output	Channel-to-Channel Skew	0.4	0.4	0.3	ns
Maximum data rate		70	80	80	Mbps

8.10 Switching Characteristics: $V_{CCA}=3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CCA}=3.3V \pm 0.3V$ (unless otherwise noted)

PARAMETER	CONDITIONS	$V_{CCB}=3.3V \pm 0.3V$	$V_{CCB}=5V \pm 0.5V$	UNIT	
		TYP	TYP		
t_{PHL}	Propagation delay time high-to-low output	A-to-B	4.8	3.6	ns
t_{PLH}	Propagation delay time low-to-high output	A-to-B	4.9	3.8	ns
t_{PHL}	Propagation delay time high-to-low output	B-to-A	3.5	3.2	ns
t_{PLH}	Propagation delay time low-to-high output	B-to-A	3.9	3.1	ns
t_{en}	Enable time	OE-to-A or B	134	128	ns
t_{dis}	Disable time	OE-to-A or B	9.8	7.7	ns
t_{rA}	Input rise time	A port rise time	1.9	1.9	ns
t_{rB}	Input rise time	B port rise time	1.8	2.3	ns
t_{fA}	Input fall time	A port fall time	2.9	2.6	ns
t_{fB}	Input fall time	B port fall time	1.8	1.6	ns
$t_{sk(O)}$	Skew(time), output	Channel-to-Channel Skew	0.4	0.3	ns
Maximum data rate			80	100	Mbps

9 Operating Characteristics

$T_A=25^\circ C$

PARAMETER	CONDITIONS	V_{CCA}							UNIT
		1.2V	1.2V	1.5V	1.8V	2.5V	2.5V	3.3V	
		V_{CCB}							
		5V	1.8V	1.8V	1.8V	2.5V	5V	3.3V to 5V	
		TYP	TYP	TYP	TYP	TYP	TYP		
C_{pdA}	Power dissipation capacitance $C_L=0$ $f=10MHz$ $t_r=t_f=1ns$	A-port input	9	8	7	8	7	8	pF
		B-port output							
C_{pdB}	Power dissipation capacitance $OE=V_{CCA}$ (outputs enabled)	B-port input	12	11	12	11	11	11	
		A-port output							
C_{pdA}	Power dissipation capacitance $C_L=0$ $f=10MHz$ $t_r=t_f=1ns$	A-port input	35	26	27	27	27	27	pF
		B-port output							
C_{pdB}	Power dissipation capacitance $OE=GND$ (outputs enabled)	B-port input	25	18	19	19	18	19	
		A-port output							
C_{pdA}	Power dissipation capacitance $C_L=0$ $f=10MHz$ $t_r=t_f=1ns$	A-port input	0.01	0.01	0.01	0.01	0.01	0.01	pF
		B-port output							
C_{pdB}	Power dissipation capacitance $OE=GND$ (outputs enabled)	B-port input	0.01	0.01	0.01	0.01	0.01	0.01	
		A-port output							

10 Parameter Measurement Information

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- PRR 10 MHz
- $Z_o = 50 \Omega$
- $dv/dt \geq 1 \text{ V/ns}$

Note: All input pulses are measured one at a time, with one transition per measurement.

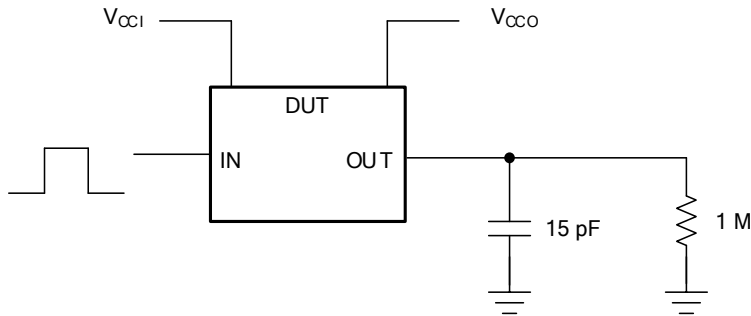


Figure 1. Data Rate, Pulse Duration, Propagation Delay, Output Rise And Fall Time Measurement Using A Push-Pull Driver

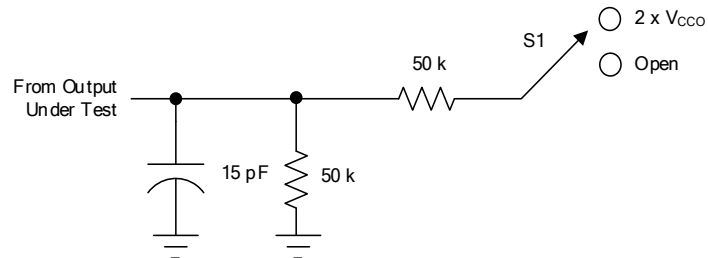


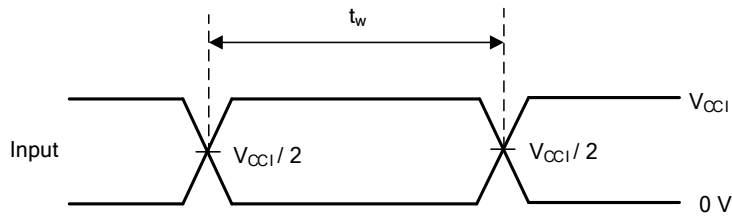
Figure 2. Load Circuit for Enable/Disable Time Measurement

Table 1. Switch Configuration for Enable/Disable Timing

TEST	S1
$t_{PZL}^{(1)}$, $t_{PLZ}^{(2)}$	$2 \times V_{CCO}$
$t_{PHZL}^{(1)}$, $t_{PZH}^{(2)}$	Open

(1) t_{PZL} and t_{PZH} are the same as t_{en} .

(2) t_{PLZ} and t_{PHZ} are the same as t_{dis} .



(1) All input pulses are measured one at a time, with one transition per measurement.

Figure 3. Voltage Waveforms Pulse Duration

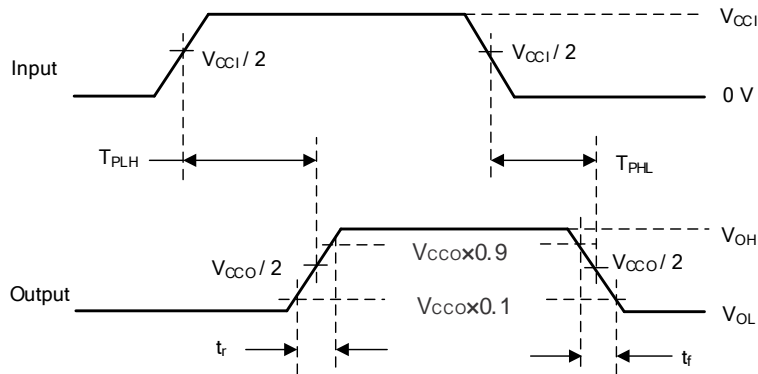
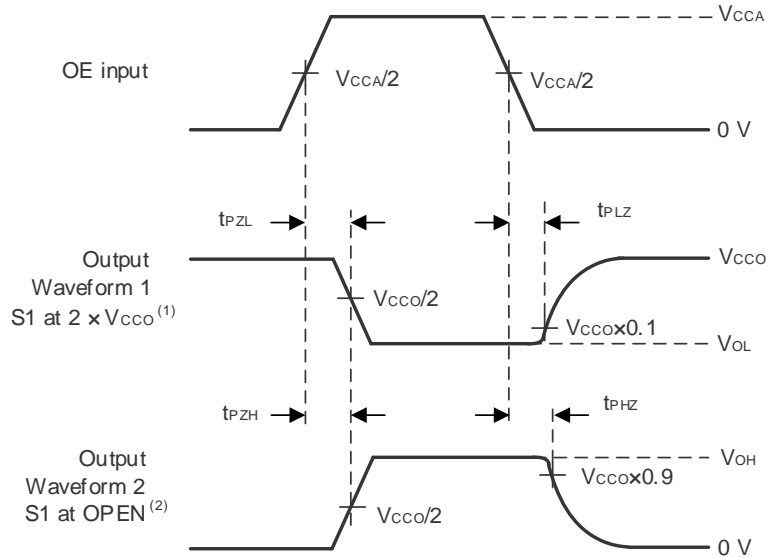


Figure 4. Voltage Waveforms Propagation Delay Times



A. Waveform 1 is for an output with internal such that the output is high, except when OE is high.
 B. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 5. Voltage Waveforms Enable and Disable

11 Detailed Description

11.1 Overview

The RS0204 device is a 4-bit, directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge-rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to RS010X products.

11.2 Architecture

The RS0204 device architecture (see Figure 6) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the device maintain a high or low, but are designed to be weak, so the output drivers can be overdriven by an external driver when data on the bus flows the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at $V_{CCO} = 1.2$ V to 1.8 V, 50 Ω at $V_{CCO} = 1.8$ V to 3.3 V, and 40 Ω at $V_{CCO} = 3.3$ V to 5 V.

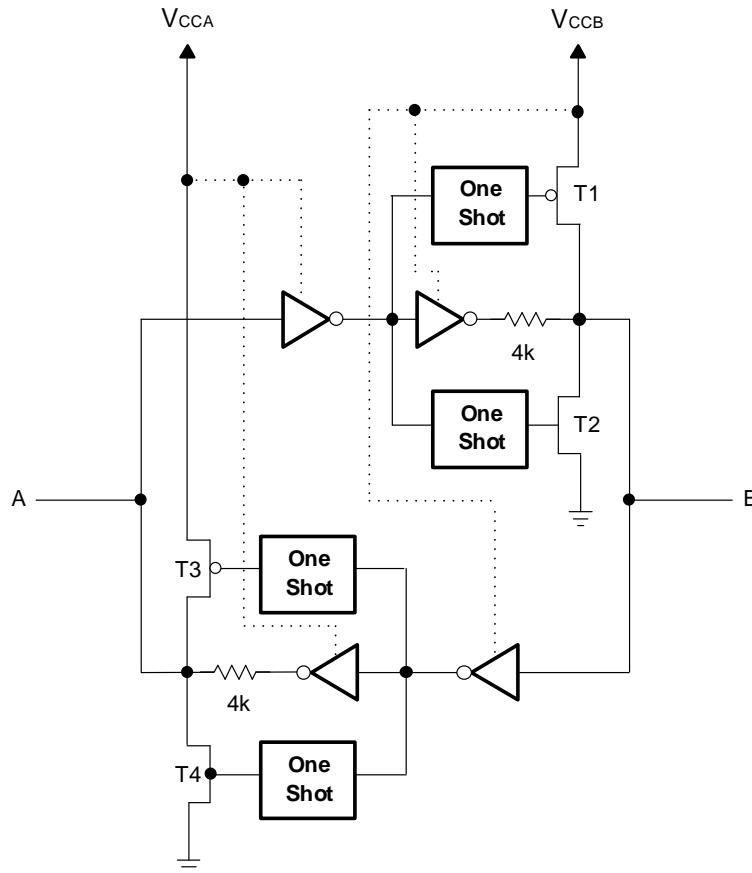
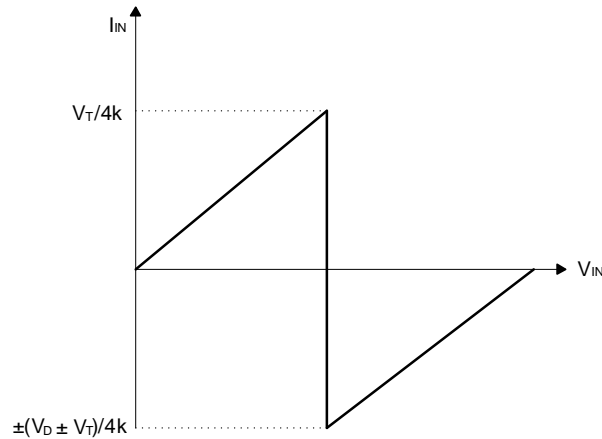


Figure 6. Architecture of RS0204 Device I/O Cell

11.3 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the device are shown in Figure 7. For proper operation, the device driving the data I/Os of the RS0204 device must have driven strength of at least ± 2 mA.



- (1) V_T is the input threshold of the RS0204 device, (typically $V_{CC} / 2$).
- (2) V_D is the supply voltage of the external driver.

Figure 7. Typical I_{IN} vs V_{IN} Curve

11.4 Output Load Considerations

We recommend careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough such that the round-trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic I_{CC} , load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the device output sees, so it is recommended that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

11.5 Enable and Disable

The RS0204 device has an OE input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

11.6 Pullup or Pulldown Resistors on I/O Lines

The device is designed to drive capacitive loads of up to 70 pF. The output drivers of the RS0204 device have low dc drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 k Ω to ensure that they do not contend with the output drivers of the RS0204 device. For the same reason, the RS0204 device must not be used in applications such as I²C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the RS010X series of level translators.

11.7 Device Functional Modes

The device has two functional modes, enabled and disabled. To disable the device, set the OE input to low, which places all I/Os in a high impedance state. Setting the OE input to high will enable the device.

12 Application and Implementation

Information in the following applications sections is not part of the Runic component specification, and Runic does not warrant its accuracy or completeness. Runic's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

12.1 Application Information

The RS0204 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. Any external pulldown or pullup resistors are recommended larger than 50 kΩ.

12.2 Typical Application

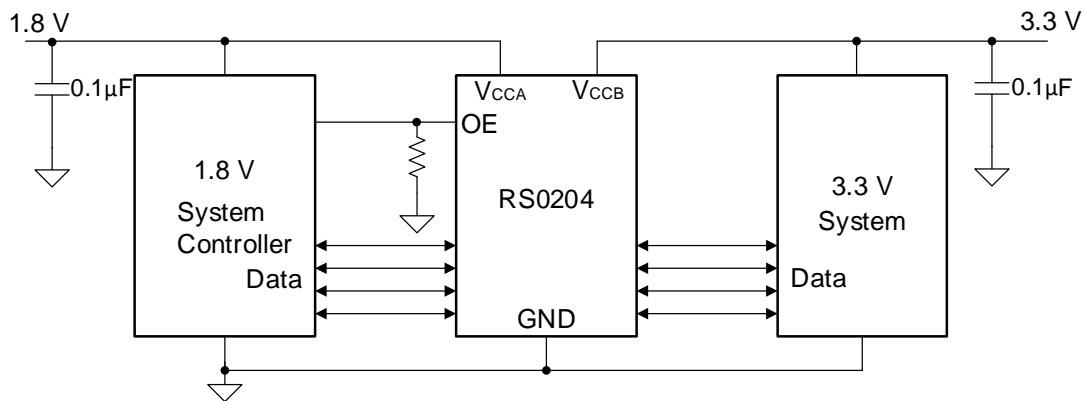
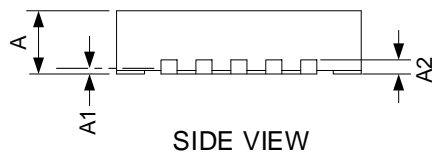
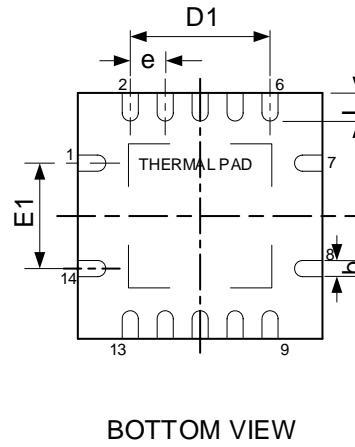
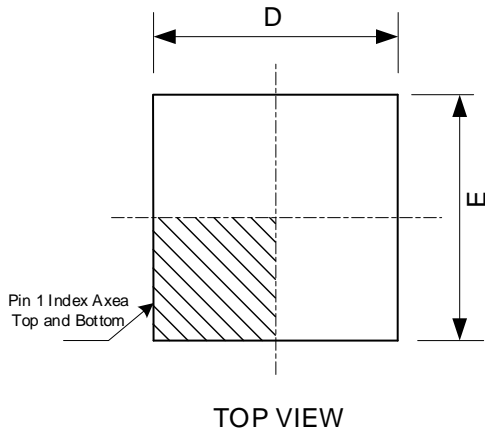


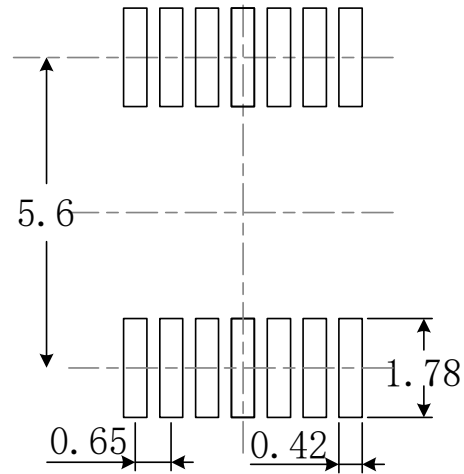
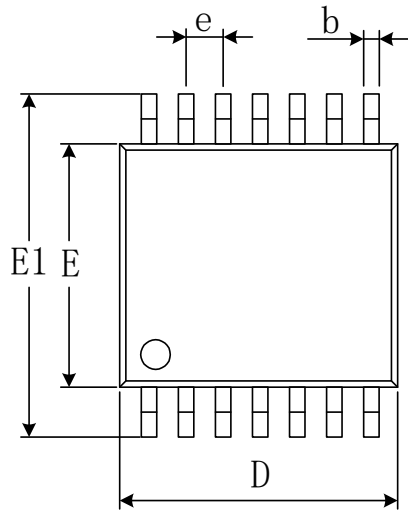
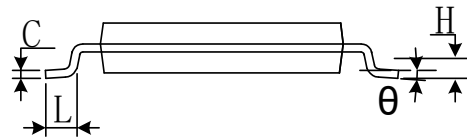
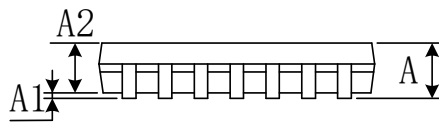
Figure 8. Typical Application Circuit

13 PACKAGE OUTLINE DIMENSIONS

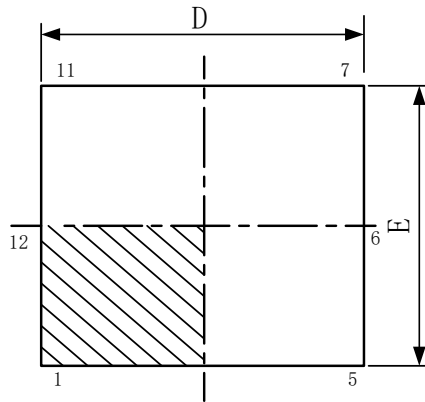
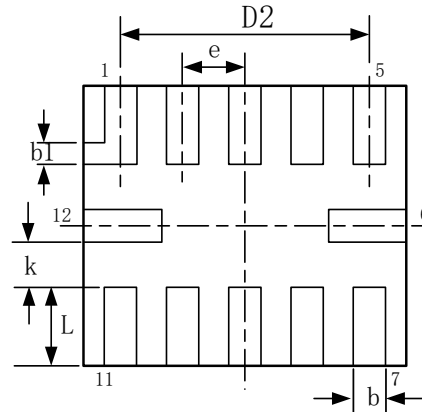
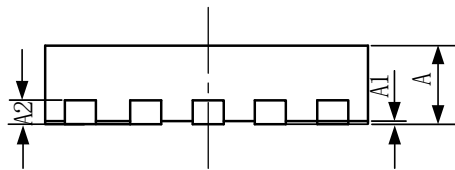
QFN3.5x3.5-14L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A2	0.200 REF		0.008 REF	
b	0.180	0.300	0.007	0.012
D	3.350	3.650	0.132	0.144
D1	2.000 TYP		0.079 TYP	
E	3.350	3.650	0.007	0.012
E1	1.500 TYP		0.059 TYP	
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TSSOP-14

RECOMMENDED LAND PATTERN (Unit: mm)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.250(TYP)		0.010(TYP)	
θ	1°	7°	1°	7°

QFN1.7x2-12L

TOP VIEW

BOTTOM VIEW

SIDE VIEW

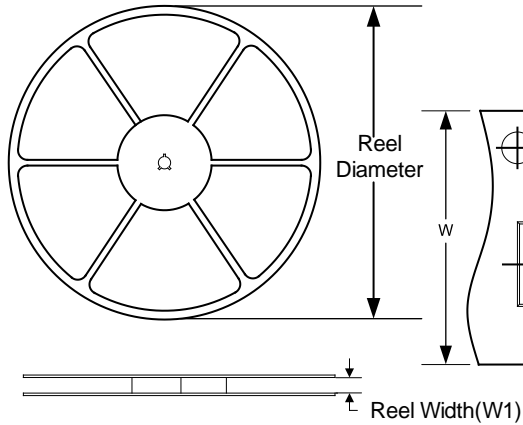
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.450	0.550	0.018	0.022
A1	0.000	0.050	0.000	0.002
A2	0.152 REF		0.006 REF	
D	1.900	2.100	0.075	0.083
E	1.600	1.800	0.063	0.071
D2	1.500	1.700	0.059	0.067
b	0.150	0.250	0.006	0.010
b1	0.150 REF		0.006 REF	
k	0.250 REF		0.010 REF	
e	0.400 BSC		0.016 BSC	
L	0.450	0.550	0.018	0.022

NOTE:

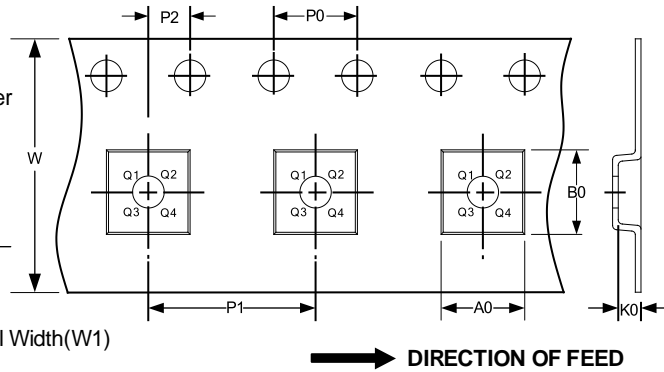
- A. All linear dimension is in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- E. REF: Reference Dimension, usually without tolerance, for information purposes only.

14 TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
QFN3.5x3.5-14L	13"	12.4	4.0	4.0	1.10	4.0	8.0	2.0	12.0	Q1
TSSOP-14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
QFN1.7x2-12L	7"	9.0	1.90	2.30	0.75	4.0	4.0	2.0	8.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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[RS8T245XTSS24-Q1](#) [UM3208QA](#) [UM3208H](#) [UM3212V8](#) [UM3304UE](#) [UM3304](#) [UM3304QT](#) [UM3202H](#) [UM3301DA](#) [UM3308](#)

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