14-Bit, 2 MSPS, Dual-Channel, Differential Analog-to-Digital Converters

1 FEATURES

- **Sample Rate: 2 MSPS**
- **INL 2.5 LSB (max)**
- **Wide Supply Range:**
  - **Analog: 2.7 V to 5.25 V**
  - **Digital: 1.65 V to AVDD**
- **14-Bit No Missing Code Resolution**
- **Auto Power-Down at Lower Speeds**
- **Two Differential Inputs**
- **Operating Temperature Range -40 °C to 125 °C**
- **SPI-Compatible Interface**
- **Package: QFN3x3-16**

2 APPLICATIONS

- **Optical networking**
- **Sensors Measurements**
- **Portable Instrumentation**
- **Medical Instrumentation**
- **Data Acquisition Systems**
- **Battery-Powered Equipment**

3 DESCRIPTIONS

The RS1472 is a 14-bit, 2MSPS analog-to-digital converter (ADC) that offers differential inputs. The device operates at a 2MSPS sample rate with a standard 16 clock data frame. The device includes a two-channel input multiplexer and a low-power successive approximation register (SAR) ADC with an inherent sample-and-hold (S/H) input stage.

The RS1472 supports a wide analog supply range that allows the full-scale input range to extend to ±5Vpp. A simple SPI, with a digital supply that can operate as low as 1.65 V, allows for easy interfacing to a wide variety of digital controllers. Automatic power-down can be enabled when operating at slower speeds to dramatically reduce power consumption.

The RS1472 is offered in a leadless QFN3x3-16 package and is specified over a temperature range of -40°C to +125°C.

Device Information [(1)]

PART NUMBER	PACKAGE	BODY SIZE(NOM)
RS1472	QFN3x3-16	3.00mm x 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

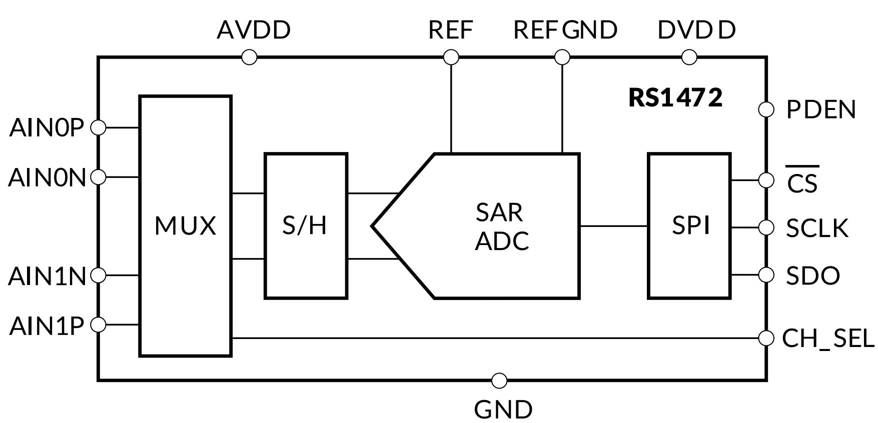

Figure 1. Block Diagram

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4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.0	2023/02/14	Preliminary version completed
A.1	2024/01/31	Initial version completed

5 PACKAGE/ORDERING INFORMATION [1]

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking [2]	MSL[3]	Package Qty
RS1472XTQC16	QFN3x3-16	16	2-Differential	-40°C ~125°C	RS1472	MSL3	Tape and Reel,5000

NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information(data code and vendor code)，the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

6 Pin Configuration and Functions (Top View)

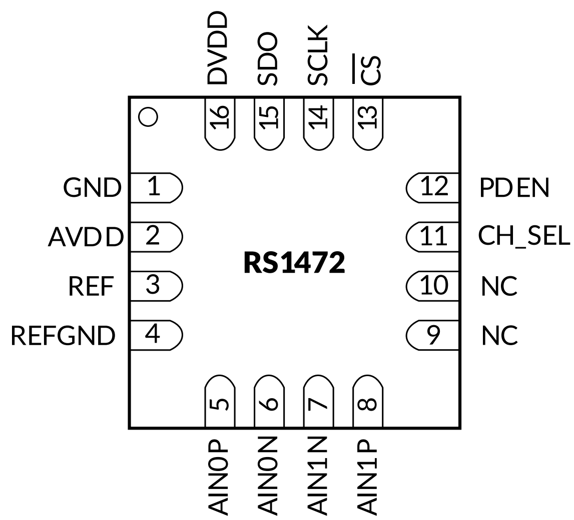


Figure 2. QFN3x3-16

Table 1. PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	GND	Power supply ground
2	AVDD	ADC power supply
3	REF	ADC positive reference input, decouple this pin with REFGND
4	REFGND	Reference return; short to analog ground plane
5	AIN0P	Positive analog input, channel 0
6	AIN0N	Negative analog input, channel 0
7	AIN1N	Negative analog input, channel1
8	AIN1P	Positive analog input, channel1
9	NC	Not connected internally, recommended to short this pin to GND
10	NC	Not connected internally, recommended to short this pin to GND
11	CH_SEL	Selects the analog input channel. Low = Channel 0 High = Channel 1 Recommended to change the channel within a window of one clock, from half a clock after the $\overline{CS}$ falling edge. This change ensures the settling on the multiplexer output before the sample start.
12	PDEN	Enables a power down feature if it is high at the $\overline{CS}$ rising edge
13	$\overline{CS}$	Chip select signal, active low
14	SCLK	Serial SPI clock
15	SDO	Serial data out
16	DVDD	Digital I/O supply

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	AVDD to GND, DVDD to GND (2)		-0.3	6	V
	Digital input voltage to GND		-0.3	DVDD+0.3	
	Digital output pin (3)		-0.3	DVDD+0.3	
Current	Signal input pin		-10	10	mA
θ_{JA}	Package thermal impedance (4)	QFN3×3-16		70	°C/W
Temperature	Operating range, T_A		-40	125	°C
	Junction, T_J (5)		-40	150	
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current-limited to 10mA or less.

(3) Include $\overline{CS}$, SCLK, SDO.

(4) The package thermal impedance is calculated in accordance with JESD-51.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	AVDD to GND	2.7	3.3	5.25	V
	DVDD to GND	1.65	3.3	AVDD	
Full scale input	$V_{IN}=V_{(AINP)} - V_{(AINN)}$	$-V_{REF}$		V_{REF}	V
Operating ambient temperature		-40		125	°C

7.4 ELECTRICAL CHARACTERISTICS

(T_A = –40°C to +125°C, AVDD = 2.7V to 5.25V, DVDD = 1.65V to AVDD, input common mode =$V_{REF}/2$ ±0.2, f_{SAMPLE} = 2MSPS, Typical specifications at T_A = +25°C, AVDD = 5V, DVDD=1.8V, unless otherwise noted.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Full-scale input span (1)	AINxP - AINxN	$-V_{REF}$		V_{REF}	V
Absolute input range	AIN0P, AIN1P	–0.2		AVDD + 0.2	V
	AIN0N, AIN1N	–0.2		AVDD + 0.2	V
Input common-mode range (2)	(AINxP + AINxN)/2		VREF/2 ± 0.2		V
Input capacitance (3)			36		pF
Input leakage current	At +125°C		1		uA
SYSTEM PERFORMANCE					
Resolution			14		Bits
No missing codes		14			Bits
Integral nonlinearity		-2.5	±0.8	2.5	LSB(4)
Differential linearity		-1	±0.6	1.5	LSB
Offset error (5)		-4	±1.5	4	LSB
Gain error		-4	±2	4	LSB
Transition noise			60		μV_{RMS}
Power-supply rejection	With 500 Hz sine wave on AVDD		60		dB
DYNAMIC CHARACTERISTICS					
Total harmonic distortion (THD) (6)	20kHz, V_{REF} = 4.096V		-92		dB
Signal to noise ratio (SNR)	20kHz, V_{REF} = 4.096V	82	84		dB
	100k Hz, V_{REF} = 4.096V		83		dB
Signal to noise and distorion ratio (SINAD)	20kHz, V_{REF} = 4.096V		84		dB
Spurious-free range (SFDR)	20kHz, V_{REF} = 4.096V		94		dB
Full power bandwidth (7)	At -1dB		20		MHz
SAMPLING DYNAMICS					
Conversion time				16	SCLK
Acquisition time		80			ns
Maximum sample rate (throughput rate)	40 MHz SCLK with a 16-clock frame			2	MSPS
Aperture delay (8)			10		ns

NOTE:
(1) Ideal input span; does not include gain or offset error.
(2) Refer to the Input Common-Mode Range section in Application Information.
(3) Refer to Figure 47 for sampling circuit details.
(4) LSB means least significant bit.
(5) In the dynamic characteristics test, input signal complies with PIN=-0.5dBFs
(6) Calculated on the first nine harmonics of the input frequency.
(7) Indicates signal bandwidth for undersampling applications.
(8) Ensured by simulation.

ELECTRICAL CHARACTERISTICS

(T_A = –40°C to +125°C, AVDD = 2.7V to 5.25V, DVDD = 1.65V to AVDD, input common mode =V_{REF}/2 ±0.2, f_{SAMPLE} = 2MSPS, Typical specifications at T_A = +25°C, AVDD = 5V, DVDD=1.8V, unless otherwise noted.)

PARAMETER		CONDITIONS	RS1472			UNITS
			MIN	TYP	MAX	
DIGITAL INPUTS/OUTPUTS						
V_{IH}	High level input voltage		0.7DVDD		DVDD	V
V_{IL}	Low level input voltage		GND		0.3DVDD	V
V_{OH}	High level output voltage	SDO load 20 pF	0.8DVDD			V
V_{OL}	Low level output voltage	SDO load 20 pF			0.2DVDD	V
I_{LEAK}	Input leakage current	0 < VIN < DVDD		±1		µA
External reference			2.5		AVDD	V
POWER SUPPLY						
AVDD	Analog Supply Voltage		2.7	3.3	5.25	V
DVDD	Digital Supply Voltage		1.65	3.3	AVDD	V
I_{AVDD}	Analog supply current	AVDD = 3.3V, f_{SAMPLE} = 2MSPS		3.6	4.2	mA
		AVDD = 5V, f_{SAMPLE} = 2MSPS		4.5	5.5	
		AVDD = 3.3V, SCLK off		2.7		
		AVDD = 5V, SCLK off		3	3.5	
I_{DVDD}	Digital supply current[9]	DVDD =3.3V, f_{SAMPLE} = 2MSPS SDO load 20pF		850		µA
I_{PD}	Power down state AVDD supply current	SCLK = 40 MHz		500		µA
		SCLK off			2.5	µA
P_{ST}	Power up time	From power down state using PDEN pin		0.3[4]	1	µs
T_A	Specified performance		-40		125	°C

NOTE:
(9) DVDD consumes only dynamic current. IDVDD = CLOAD × DVDD × number of 0→1 transitions in SDO × fSAMPLE. This is a load-dependent current and there is no DVDD current when the output is not toggling.

7.5 Timing DIAGRAM:RS1472

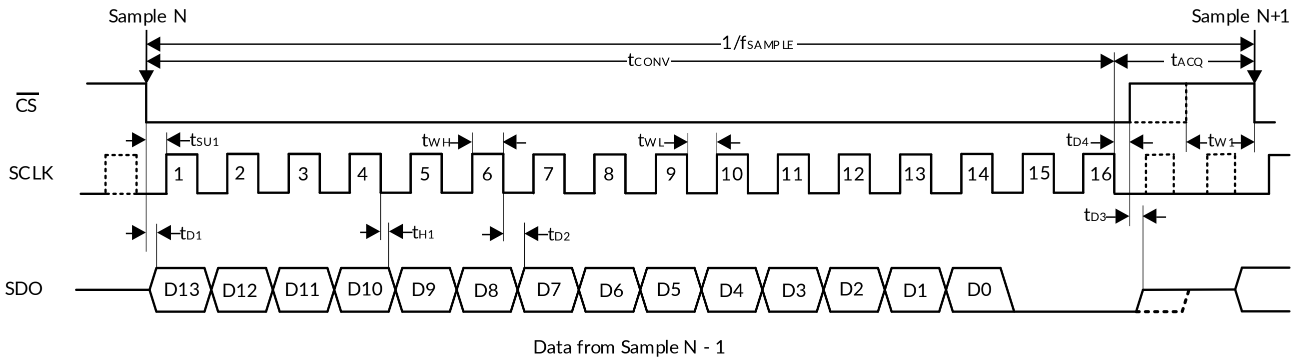


Table2. TIMING REQUIREMENTS:RS1472(1)

PARAMETER		TEST CONSITIONS(2)	MIN	TYP	MAX	UNIT
t_{CONV}	Conversion time				16	SCLK
t_{ACQ}	Acquisition time		80			ns
t_{SAMPLE}	Sample rate (throughput rate)	SCLK=40MHz 16-clock frame			2	MSPS
t_{W1}	Pulse width $\overline{CS}$ high		25			ns
t_{D1}	Delay time, $\overline{CS}$ low to first data (D0~D15) out	DVDD = 1.8V			14.5	ns
		DVDD = 3V			12.5	ns
		DVDD = 5V			8.5	ns
t_{SU1}	Setup time, $\overline{CS}$ low to first rising edge of SCLK	DVDD = 1.8V	3.5			ns
		DVDD = 3V	3.5			ns
		DVDD = 5V	3.5			ns
t_{D2}(3)	Delay time, SCLK falling to SDO	DVDD = 1.8V			11	
		DVDD = 3V			9	
		DVDD = 5V			7.1	
t_{H1}	Hold time, SCLK falling to data valid	DVDD = 1.8V	4			ns
		DVDD = 3V	3			ns
		DVDD = 5V	2			ns
t_{D3}	Delay time, $\overline{CS}$ high to SDO 3-state	DVDD = 1.8V			15	ns
		DVDD = 3V			12.5	ns
		DVDD = 5V			8.5	ns
t_{D4}	Delay time, $\overline{CS}$ rising edge from conversion end		10			ns
t_{WH}	Pulse duration, SCLK high		8			ns
t_{WL}	Pulse duration, SCLK low		8			ns
	SCLK frequency				40	MHz
t_{PDSU}	Setup time, PDEN high to $\overline{CS}$ rising edge		2			ns
t_{PDH}	Hold time, $\overline{CS}$ rising edge to PDEN falling edge		20			ns

(1) All specifications are ensured by simulations at T_A = –40°C to +125°C, and DVDD = 1.65 V to AVDD, unless otherwise noted.
(2) 1.8V specifications apply from 1.65V to 2V; 3V specifications apply form 2.7V to 3.6V; 5V specifications apply from 4.75V to 5.25V.
(3) With 20 pF load.

7.6 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = +25°C, AVDD = 5.0 V, DVDD = 1.8 V, VREF = 2.5 V, f_{SAMPLE} = 2 MSPS, f_{IN} = 20kHz, P_{IN} = -0.5dBFs, f_{SCLK} = 40 MHz, and PDEN = 0 (unless otherwise noted).

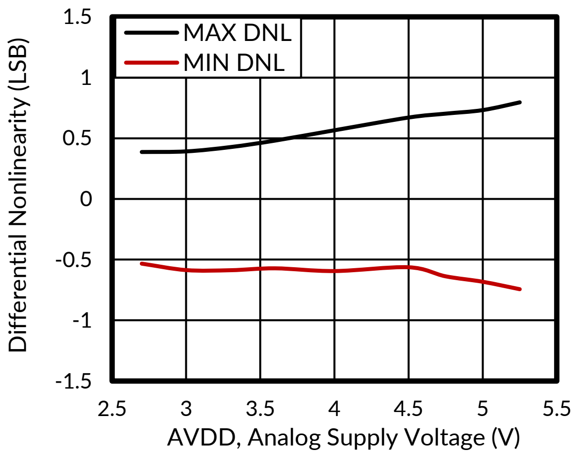


Figure 3. DNL vs ANALOG SUPPLY VOLTAGE

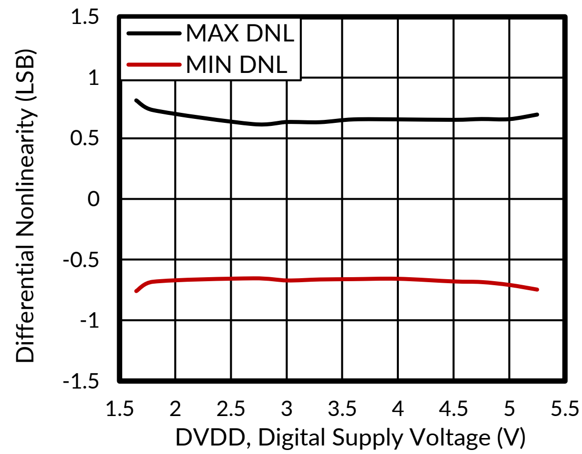


Figure 4. DNL vs DIGITAL SUPPLY VOLTAGE

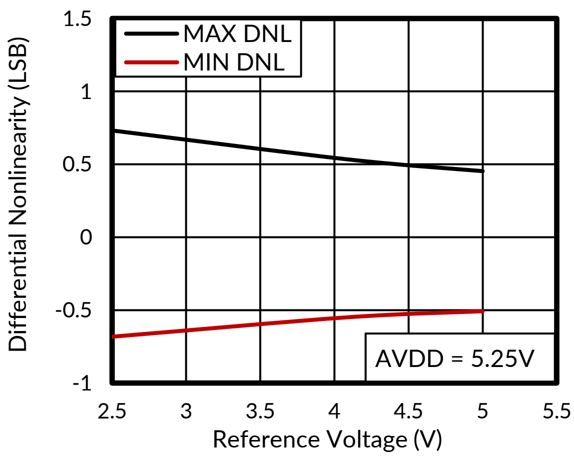


Figure 5. DNL vs REFERENCE VOLTAGE

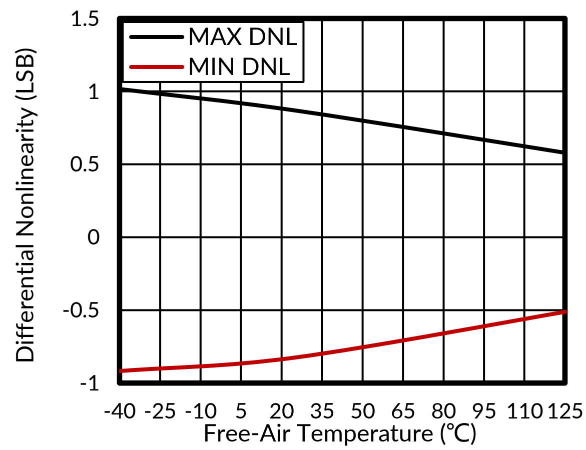


Figure 6. DNL vs FREE-AIR TEMPERATURE

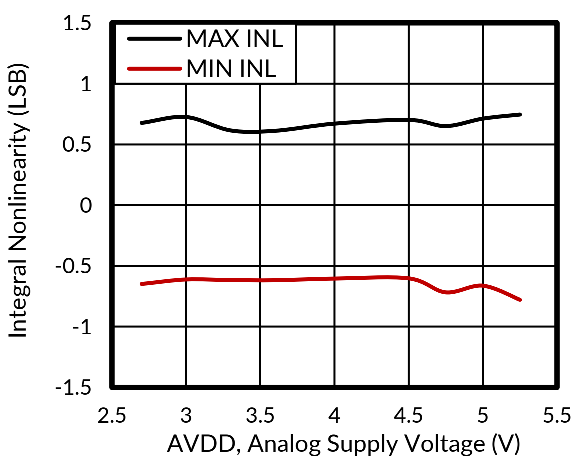


Figure 7. INL vs ANALOG SUPPLY VOLTAGE

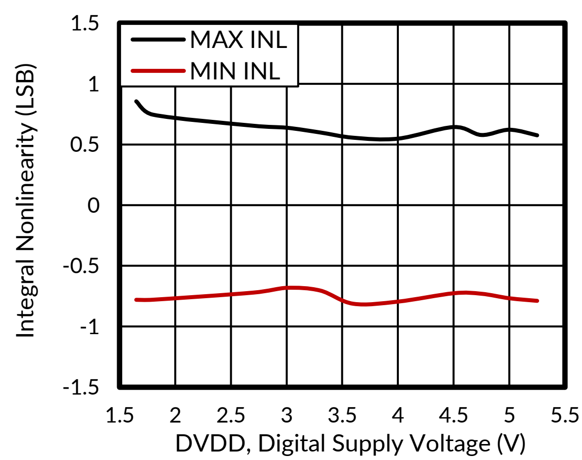


Figure 8. INL vs DIGITAL SUPPLY VOLTAGE

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, AVDD = 5.0 V, DVDD = 1.8 V, VREF = 2.5 V, f_{SAMPLE} = 2 MSPS, f_{IN} = 20kHz, f_{SCLK} = 40 MHz, and PDEN = 0 (unless otherwise noted).

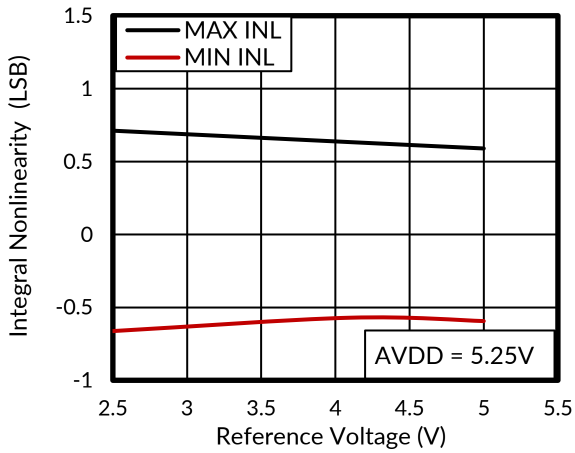


Figure 9. INL vs REFERENCE VOLTAGE

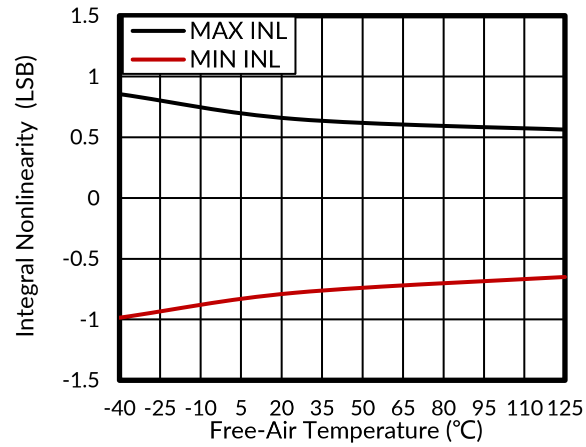


Figure 10. INL vs FREE-AIR TEMPERATURE

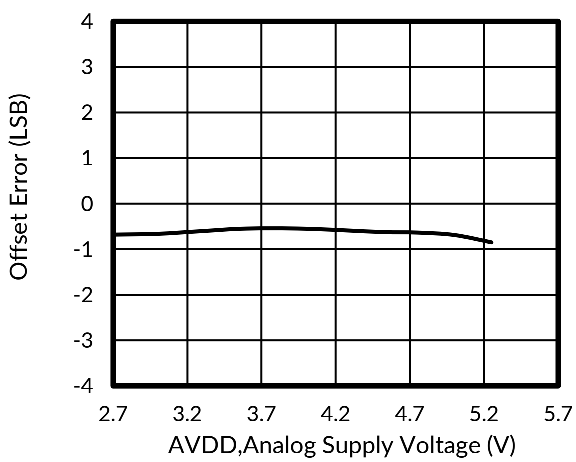


Figure 11. OFFSET ERROR vs ANALOG SUPPLY VOLTAGE

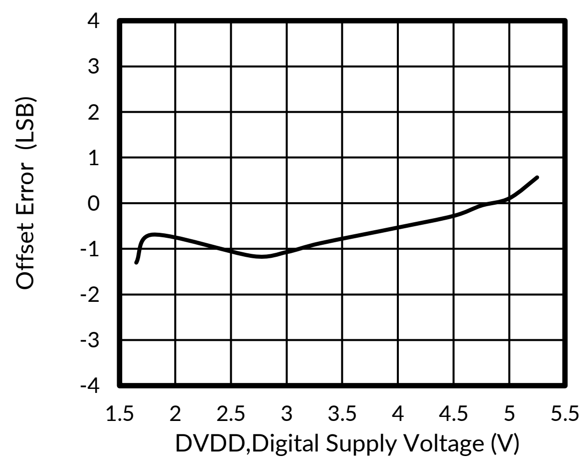


Figure 12. OFFSET ERROR vs DIGITAL SUPPLY VOLTAGE

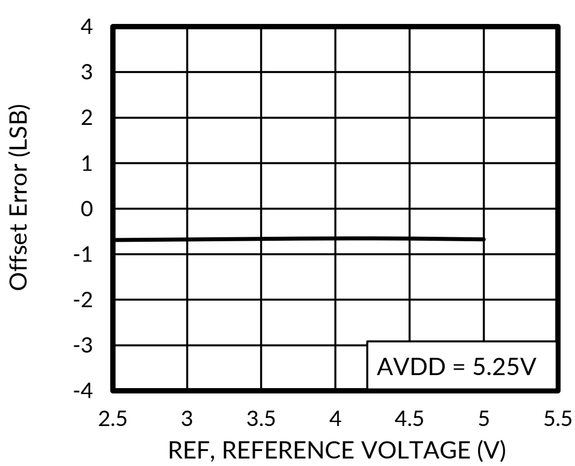


Figure 13. OFFSET ERROR vs REFERENCE VOLTAGE

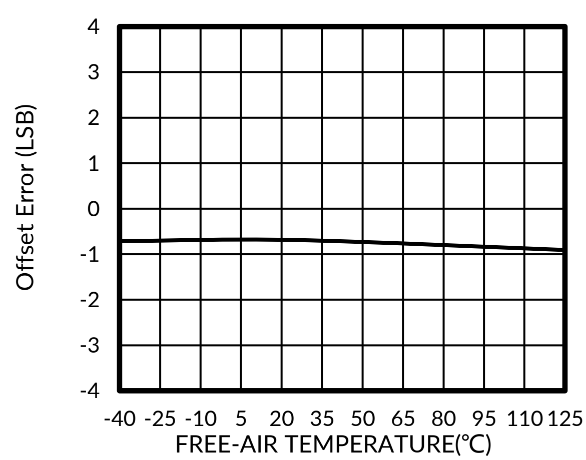


Figure 14. OFFSET ERROR vs FREE-AIR TEMPERATURE

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = +25°C, AVDD = 5.0 V, DVDD = 1.8 V, VREF = 2.5 V, f_{SAMPLE} = 2 MSPS, f_{IN} = 20kHz, f_{SCLK} = 40 MHz, and PDEN = 0 (unless otherwise noted).

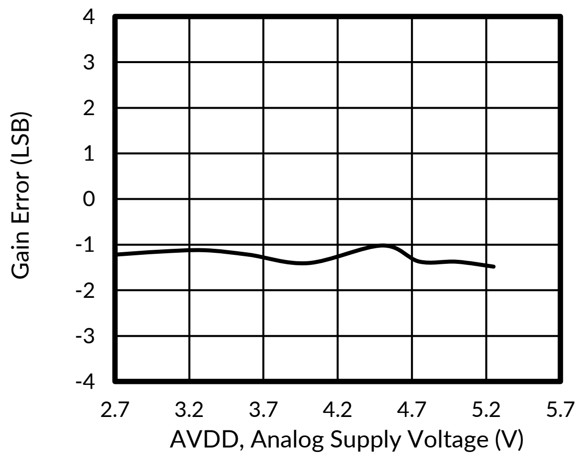


Figure 15. GAIN ERROR vs ANALOG SUPPLY VOLTAGE

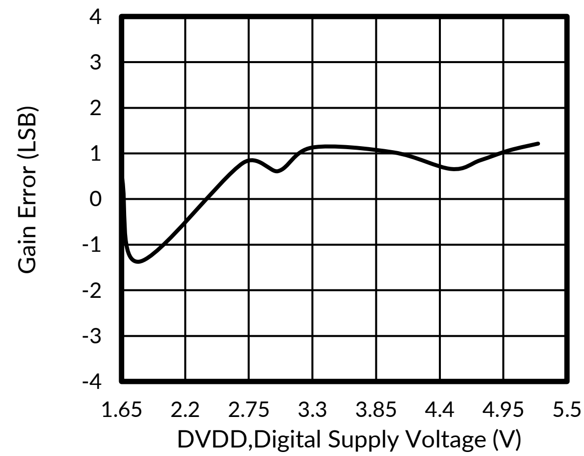


Figure 16. GAIN ERROR vs DIGITAL SUPPLY VOLTAGE

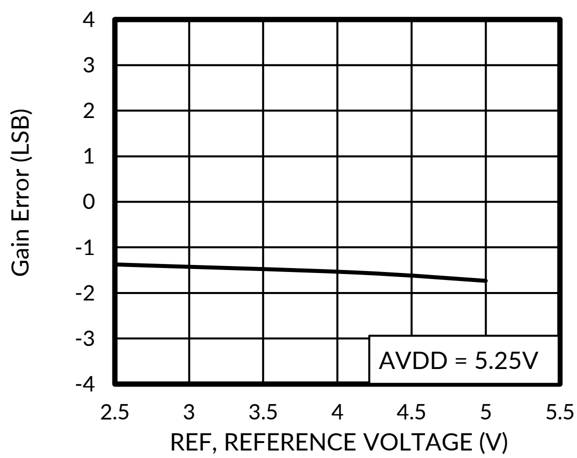


Figure 17. GAIN ERROR vs REFERENCE VOLTAGE

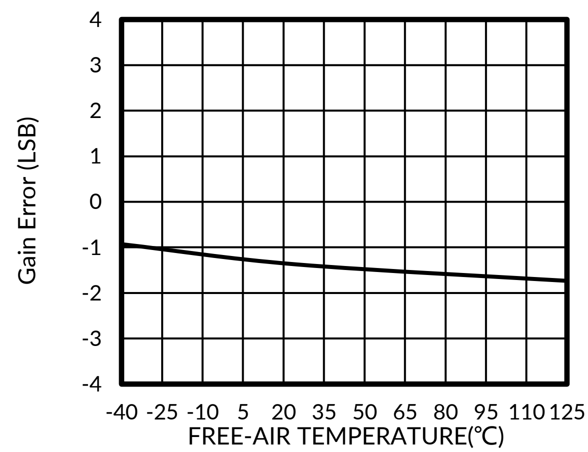


Figure 18. GAIN ERROR vs FREE-AIR TEMPERATURE

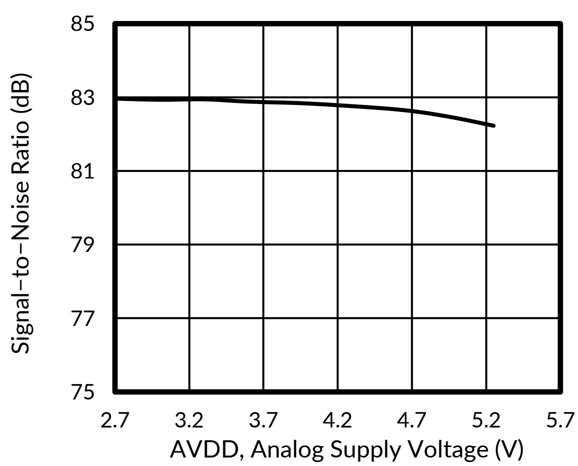


Figure 19. SNR vs ANALOG SUPPLY VOLTAGE

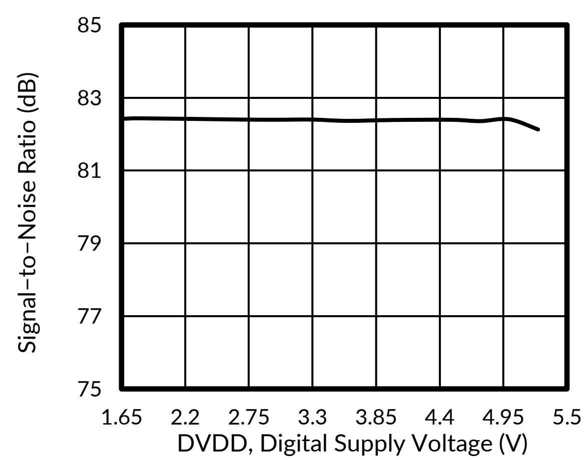


Figure 20. SNR vs DIGITAL SUPPLY VOLTAGE

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, AVDD = 5.0 V, DVDD = 1.8 V, VREF = 2.5 V, f_{SAMPLE} = 2 MSPS, f_{IN} = 20kHz, f_{SCLK} = 40 MHz, and PDEN = 0 (unless otherwise noted).

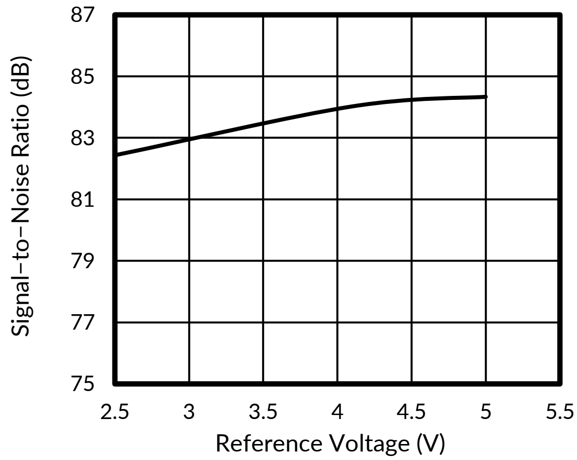


Figure 21. SNR vs REFERENCE VOLTAGE

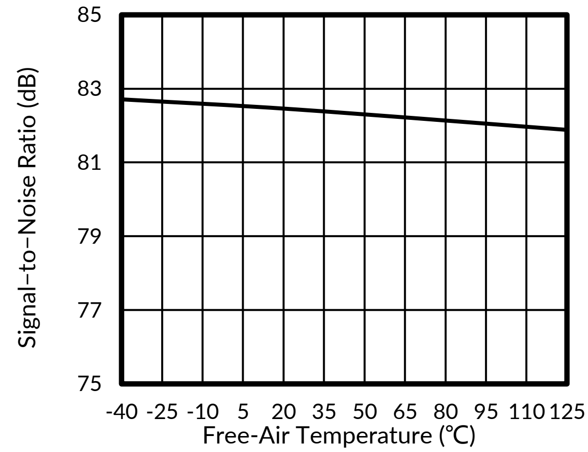


Figure 22. SNR vs FREE-AIR TEMPERATURE

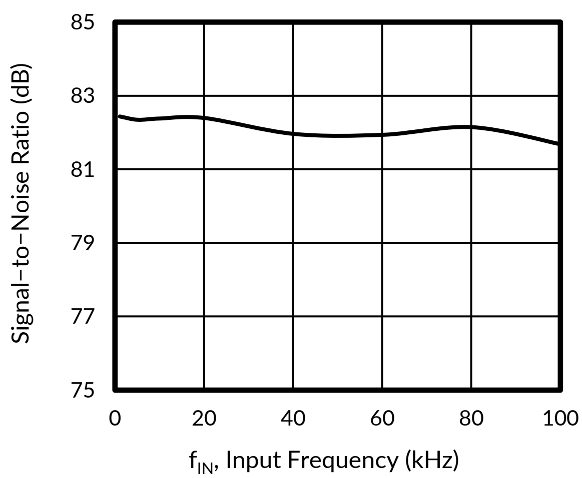


Figure 23. SNR vs INPUT FREQUENCY

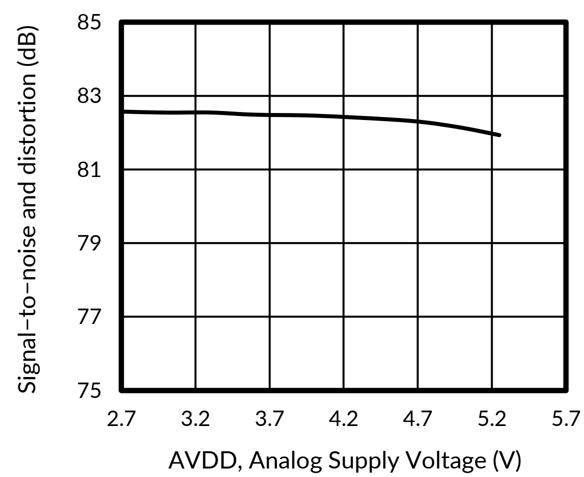


Figure 24. SINAD vs ANALOG SUPPLY VOLTAGE

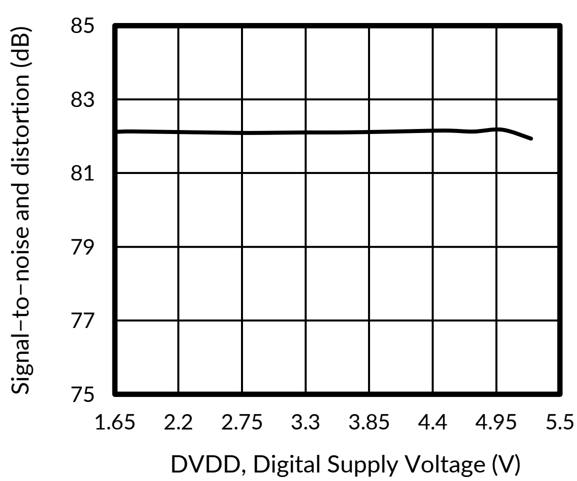


Figure 25. SINAD vs DIGITAL SUPPLY VOLTAGE

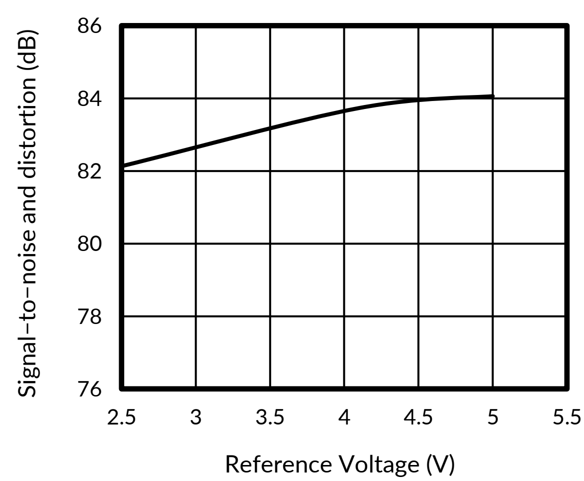


Figure 26. SINAD vs REFERENCE VOLTAGE

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, AVDD = 5.0 V, DVDD = 1.8 V, VREF = 2.5 V, f_{SAMPLE} = 2 MSPS, f_{IN} = 20kHz, f_{SCLK} = 40 MHz, and PDEN = 0 (unless otherwise noted).

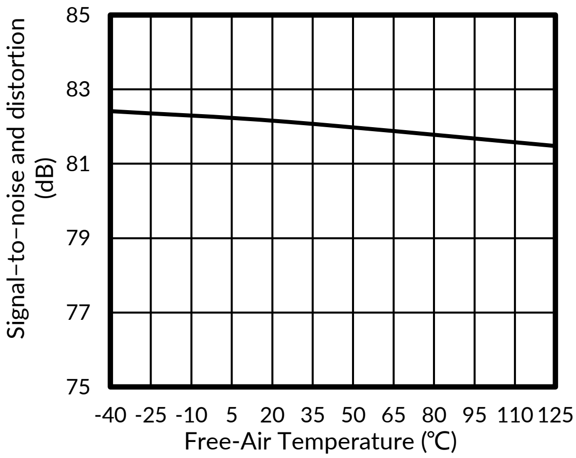


Figure 27. SINAD vs FREE-AIR TEMPERATURE

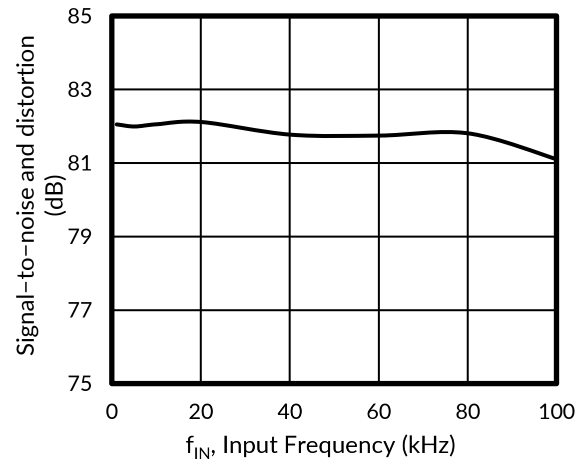


Figure 28. SINAD vs INPUT FREQUENCY

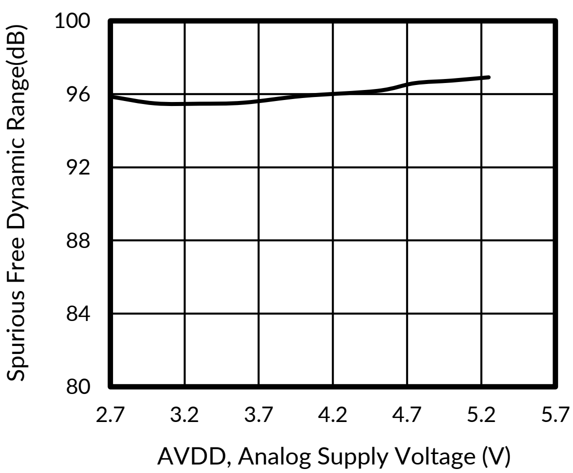


Figure 29. SFDR vs ANALOG SUPPLY VOLTAGE

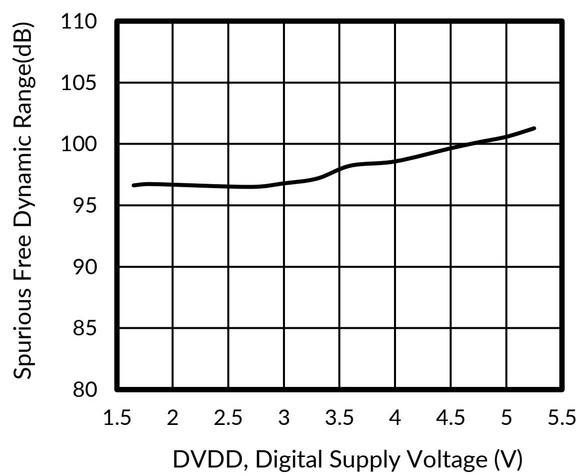


Figure 30. SFDR vs DIGITAL SUPPLY VOLTAGE

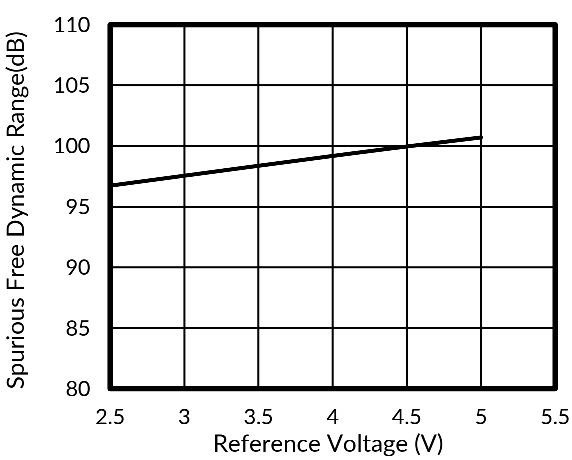


Figure 31. SFDR vs REFERENCE VOLTAGE

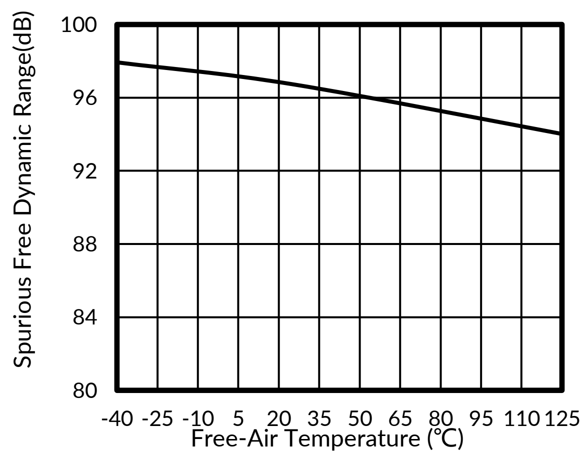


Figure 32. SFDR vs FREE-AIR TEMPERATURE

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, AVDD = 5.0 V, DVDD = 1.8 V, VREF = 2.5 V, f_{SAMPLE} = 2 MSPS, f_{IN} = 20kHz, f_{SCLK} = 40 MHz, and PDEN = 0 (unless otherwise noted).

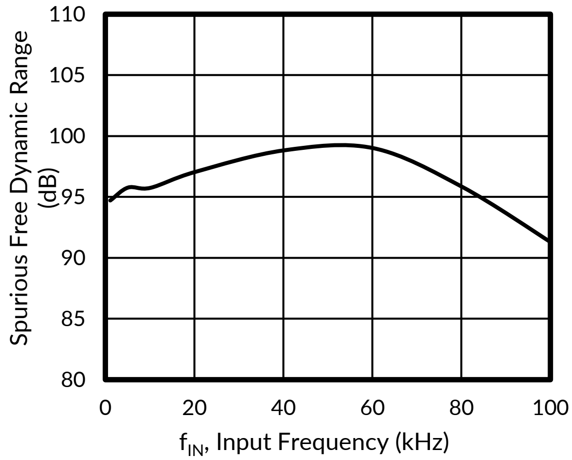


Figure 33. SFDR vs INPUT FREQUENCY

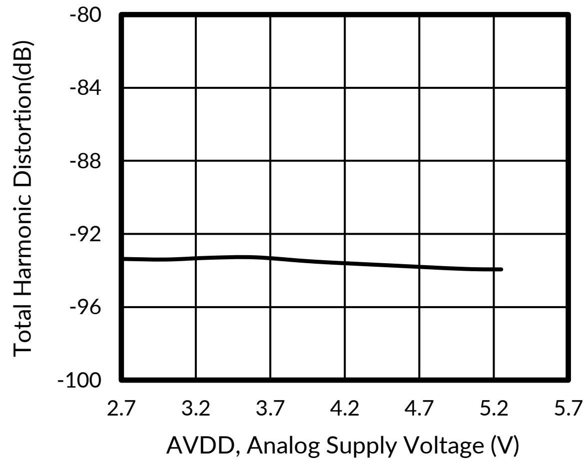


Figure 34. THD vs ANALOG SUPPLY VOLTAGE

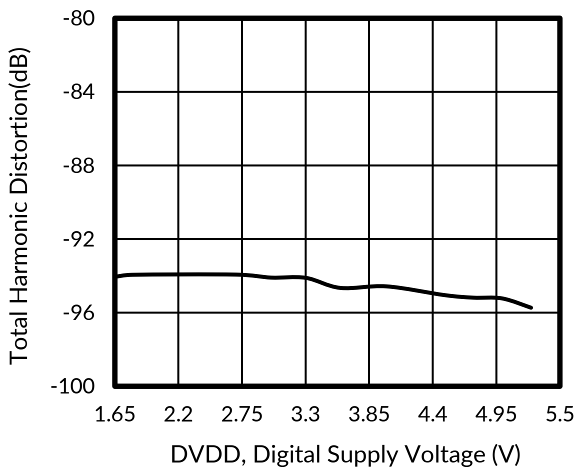


Figure 35. THD vs DIGITAL SUPPLY VOLTAGE

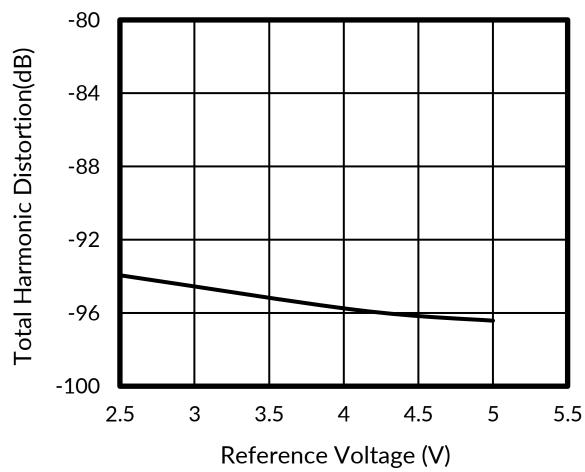


Figure 36. THD vs REFERENCE VOLTAGE

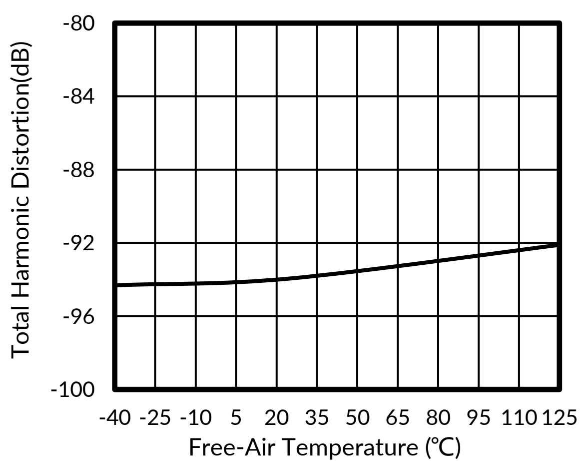


Figure 37. THD vs FREE-AIR TEMPERATURE

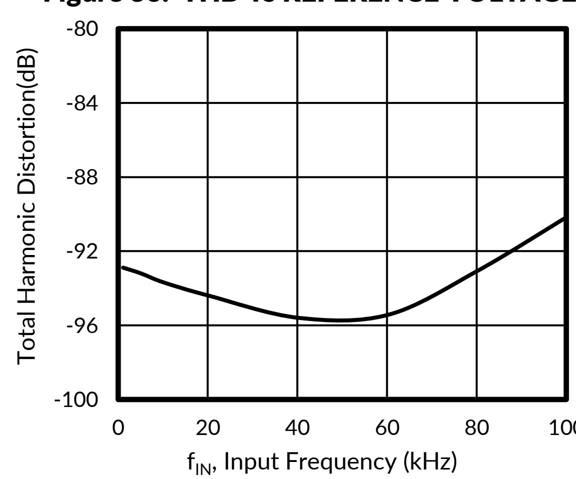


Figure 38. THD vs INPUTFREQUENCY

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.
At T_A = +25°C, AVDD = 5.0 V, DVDD = 1.8 V, VREF = 2.5 V, f_{SAMPLE} = 2 MSPS, f_{IN} = 20kHz, f_{SCLK} = 40 MHz, and PDEN = 0 (unless otherwise noted).

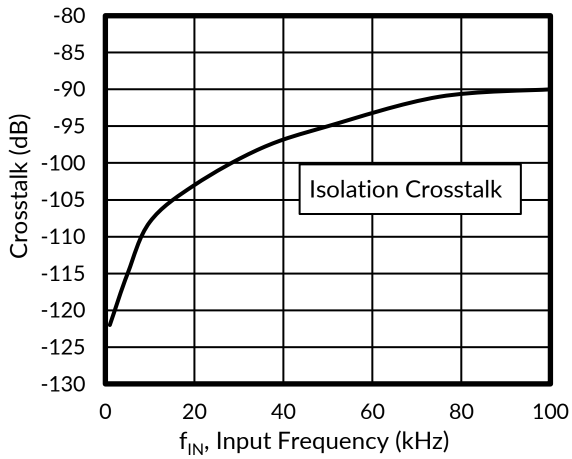


Figure 39. CROSSTALK vs INPUT FREQUENCY

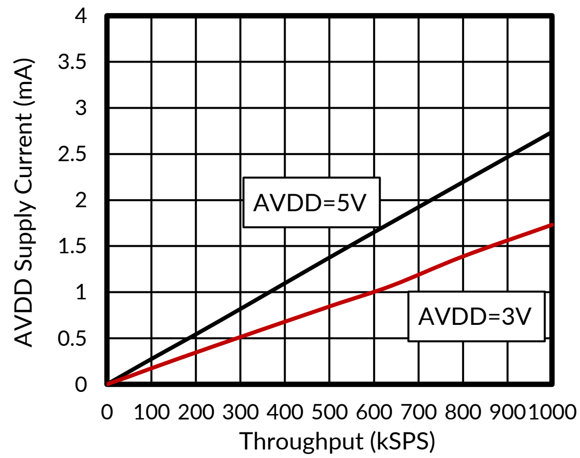


Figure 40. ANALOG SUPPLY CURRENT (Dynamic) vs SAMPLE RATE

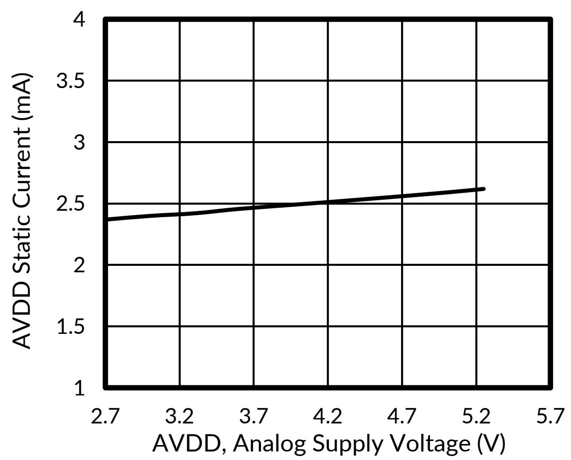


Figure 41. ANALOG SUPPLY CURRENT (Static) vs ANALOG SUPPLY VOLTAGE

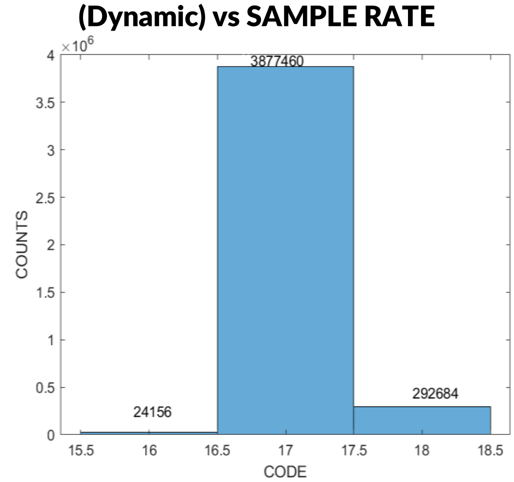


Figure 42. Histogram of a DC Input near Code Center

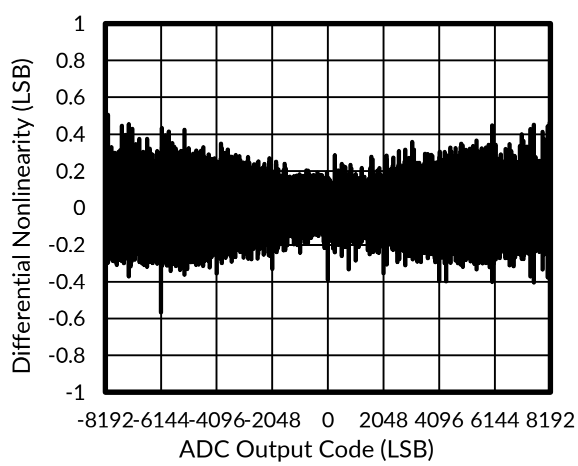


Figure 43. Differential Nonlinearity vs. Code

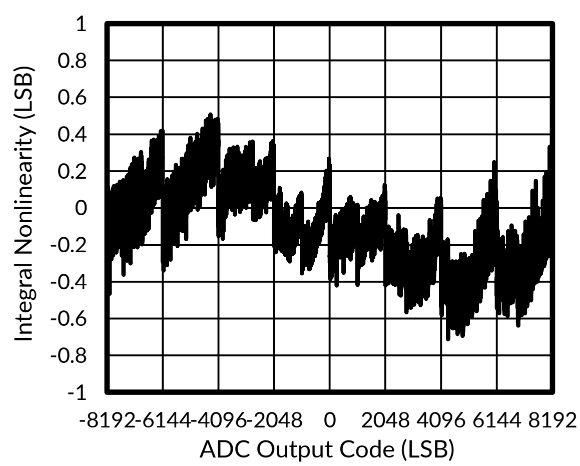


Figure 44. Integral Nonlinearity vs. Code

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25°C, AVDD = 5.0 V, DVDD = 1.8 V, VREF = 2.5 V, f_{SAMPLE} = 2 MSPS, f_{IN} = 20kHz, f_{SCLK} = 40 MHz, and PDEN = 0 (unless otherwise noted).

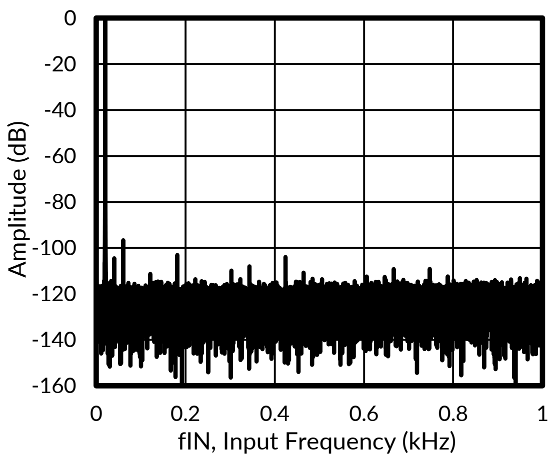


Figure 45. 20 kHz FFT, VREF = 2.5 V

8 OVERVIEW

The RS1472 is a 14-bit, miniature, dual-channel, low-power, differential input SAR ADC. The PDEN pin enables an auto power-down mode that further reduces power consumption at lower speeds.

8.1 MULTIPLEXER AND ADC INPUT

The RS1472 features a differential input with a double-pole, double-throw multiplexer. Each of the positive (AINxP) and negative (AINxN) inputs can swing from $-V_{REF}/2$ to $+V_{REF}/2$ around the common-mode voltage (AINxP + AINxN)/2 so that AINxP and AINxN swing in opposite directions equally from common-mode voltage (differential input swing $V_{AINxP} - V_{AINxN}$ ranges from $-V_{REF}$ to $+V_{REF}$). The ADC converts the difference in voltage: $V_{AINxP} - V_{AINxN}$. This feature allows the devices to reject the common-mode noise in the input signal.

Figure 46 shows the electrostatic discharge (ESD) diodes to supply and ground at every analog input. Make sure that these diodes do not turn on by keeping the supply voltage within the specified input range.

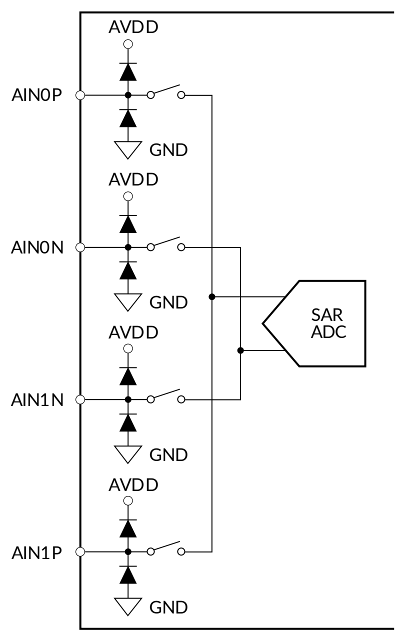


Figure 46. Analog Inputs

Figure 47 shows an equivalent circuit of the multiplexer and ADC sampling stage. See the Application Information section for details on the driving circuit. The positive and negative sense inputs are separately sampled on 36 pF sampling capacitors. The multiplexer and sampling switches are represented by an ideal switch in series with an about 50 Ω resistance. Note that this is dc resistance and can be used for step-settling calculations (do not use the RC values shown in Figure 47 for 3 dB bandwidth calculations for undersampling applications). During sampling, the devices connect the 36pF sampling capacitor to the ADC driver. This connection creates a glitch at the device input. It is recommended to connect a capacitor across the AINxP and AINxN terminals to reduce this glitch. A driving circuit must have sufficient bandwidth to settle this glitch within the acquisition time.

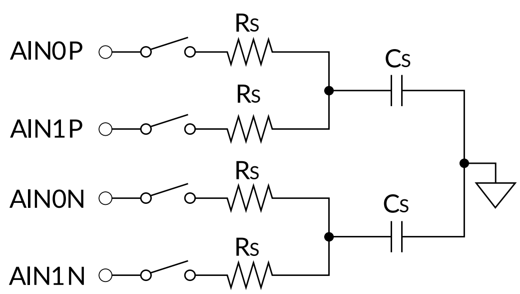


Figure 47. Input Sampling Stage Equivalent Circuit

Figure 48 shows a timing diagram for the ADC analog input channel selection. As shown in Figure 48, the CH_SEL signal selects the analog input channel to the ADC. CH_SEL = 0 selects channel 0 and CH_SEL = 1 selects channel 1. It is recommended not to toggle the CH_SEL signal during an ADC acquisition phase until the device sees the first valid SCLK rising edge after the device samples the analog input. If CH_SEL is toggled during this period, it can cause erroneous output code because the device might see unsettled analog input. CH_SEL can be toggled at any time during the window specified in Figure 48; however, it is recommended to select the desired channel after the first SCLK rising edge and before the second SCLK rising edge. This timing ensures that the multiplexer output is settled before the ADC starts acquisition of the analog input.

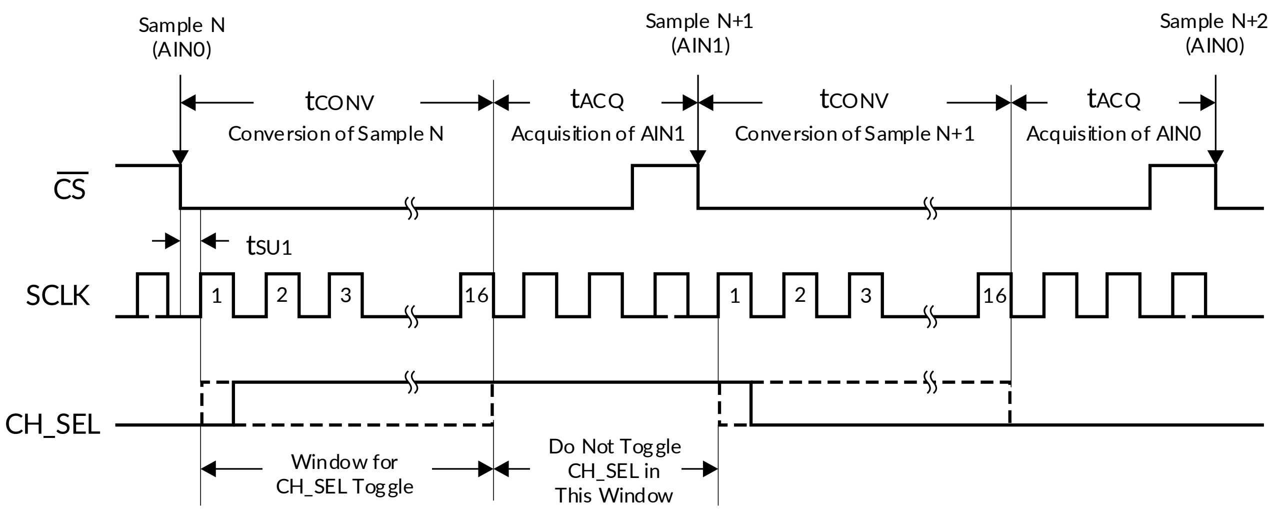


Figure 48. ADC Analog Input Channel Selection

8.2 REFERENCE

The RS1472 uses an external reference voltage during the conversion of a sampled signal. The device switches the capacitors used in the conversion process to the reference terminal during conversion. The switching frequency is the same as the SCLK frequency. It is necessary to decouple the REF terminal to REFGND with a 1µF ceramic capacitor in order to get the best noise performance from the device. The capacitor must be placed closest to these pins. Figure 49 shows a typical reference driving circuit.

Sometimes it is convenient to use AVDD as a reference. The RS1472 allow reference ranges up to AVDD. However, make sure that AVDD is well-bypassed and that there is a separate bypass capacitor between REF and REFGND.

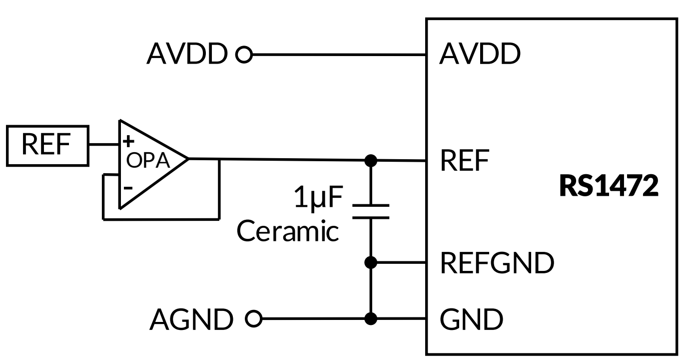


Figure 49. Typical Reference Driving Circuit

8.3 ADC TRANSFER FUNCTION

The RS1472 output is in twos compliment format. Figure 50 shows the ideal transfer characteristics for these devices. Here, full-scale range for the ADC input (AINxP – AINxN) is equal to twice the reference input voltage to the ADC 2 × (VREF). 1 LSB is equal to 2 × (VREF/2^N), where N is the resolution of the ADC (N = 14 for the RS1472). The differential input of the ADC is bipolar around the common-mode voltage (AINxP + AINxN)/2 and has a range of positive FSR (+VREF) to negative FSR (–VREF).

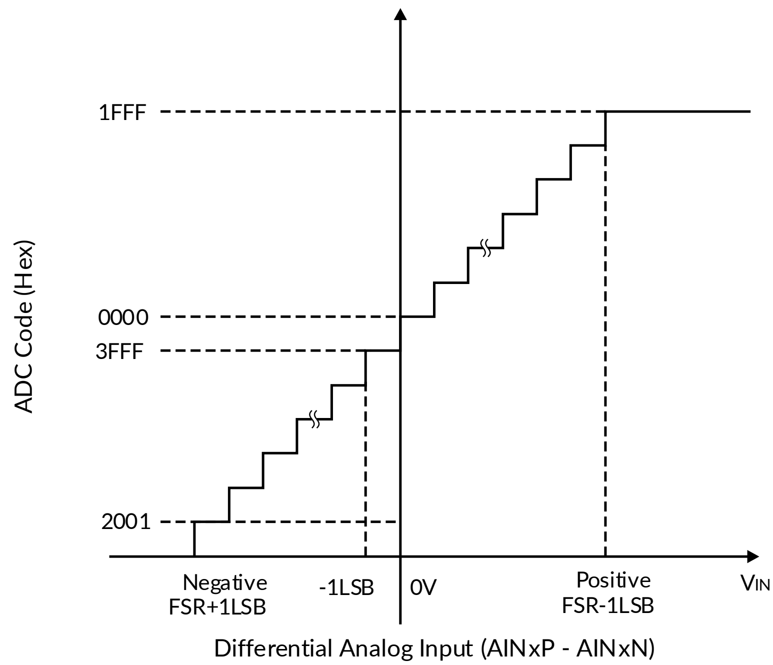


Figure 50. RS1472 Transfer Characteristics

9 DEVICE OPERATION

The RS1472 operate with either a 16-clock frame or 32-clock frame for ease of interfacing with the host processor.

9.1 16-CLOCK FRAME

Figure 51 shows the devices operating in 16-clock mode. This mode is the fastest mode for device operation. In this mode, the devices output data from previous conversions while converting the recently sampled signal.

As shown in Figure 51, the RS1472 start acquisition of the analog input from the 16th falling edge of SCLK. The device samples the input signal on the $\overline{CS}$ falling edge. SDO comes out of 3-state and the device outputs the MSB on the $\overline{CS}$ falling edge. The device outputs the next lower SDO bits on every SCLK falling edge after it has first seen the SCLK rising edge. The data correspond to the sample and conversion completed in the previous frame. During a $\overline{CS}$ low period, the device converts the recently sampled signal. It uses SCLK for conversions. Conversion is complete on the 16th SCLK falling edge. $\overline{CS}$ can be high at any time after the 16th SCLK falling edge (see the Parameter Measurement Information for more details). The $\overline{CS}$ rising edge after the 16th SCLK falling edge and before the 29th SCLK falling edge keeps the device in the 16-clock data frame. The device output goes to 3-state when $\overline{CS}$ is high. It is also permissible to stop SCLK after the device has seen the 16th SCLK falling edge.

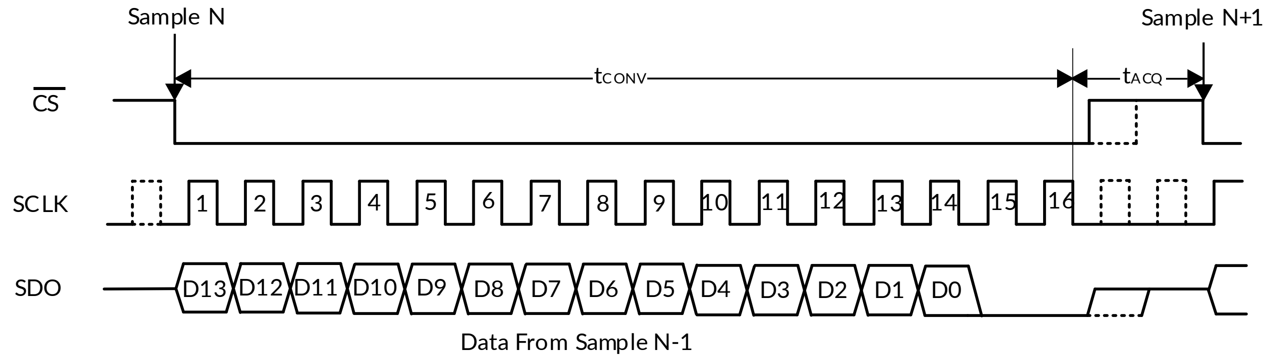


Figure 51. RS1472 Operating in 16-Clock Mode without Power-Down (PDEN = 0)

9.2 32-CLOCK FRAME

Figure 52 shows the devices operating in 32-clock mode. In this mode, the devices convert and output the data from the most recent sample before taking the next sample.

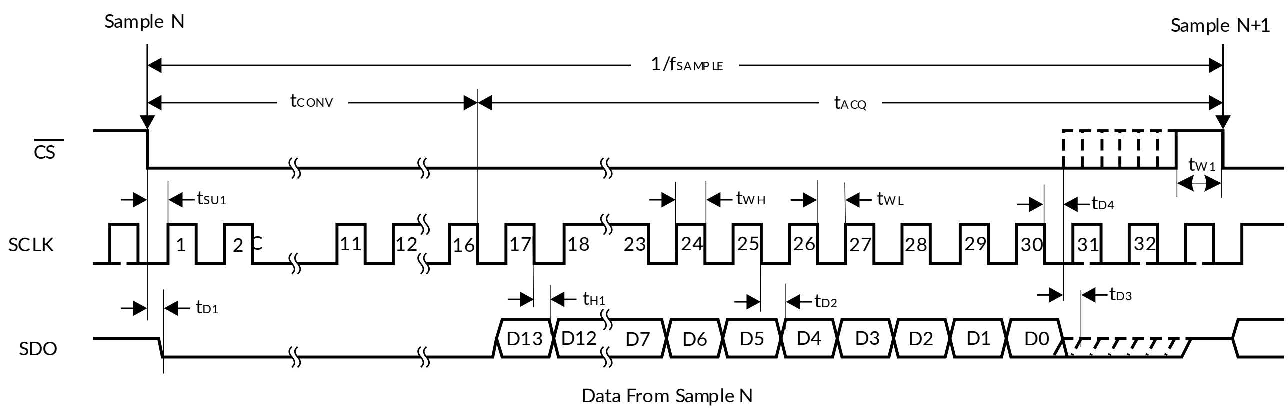


Figure 52. RS1472 Operation in 32-Clock Frame without Power-Down (PDEN = 0)

$\overline{CS}$ can be held low past the 16th falling edge of SCLK. The devices continue to output recently converted data starting with the 16th SCLK falling edge. If $\overline{CS}$ is held low until the 30th SCLK falling edge, then the devices detect 32-clock mode. Note that the device data from recent conversions are already output with no latency before the 30th SCLK falling edge. Once 32-clock mode is detected, the device outputs 16 zeros during the next conversion (in fact, for the first 16 clocks), unlike 16-clock mode where the devices output the previous conversion result. SCLK can be stopped after the devices have seen the 30th falling edge with $\overline{CS}$ low.

9.3 CONVERSION ABORT

For some event triggered applications such as latching position of absolute position sensor on marker or homing pulse, it is essential to abort ongoing conversion on event and quickly start fresh acquisition. RS1472 features conversion abort function. $\overline{CS}$ high during conversion (during first 16 clocks) will abort ongoing conversion and start fresh acquisition. Device will sample acquired signal during $\overline{CS}$ high period on falling edge of $\overline{CS}$ and will start conversion normally, however data on SDO (conversion results from aborted frame) will not be valid.

For example, if conversion is aborted during ‘n^{th}’ frame and (n+1) is first valid frame after conversion abort. SDO data during frame number (n+1) (corresponding to n^{th} conversion) will not be valid. Conversion results for sample and conversion during frame number (n+1) will be available in frame number (n+2).

9.4 POWER-DOWN

The RS1472 offers an easy-to-use power-down feature available through a dedicated PDEN pin (pin 12). A high level on PDEN at the $\overline{CS}$ rising edge enables the power-down mode for that particular cycle. For speeds below approximately 750 kSPS, it is convenient to use 32-clock mode with power-down. This configuration results in considerable power savings.

As shown in Figure 53, PDEN is held at a logic '1' level. Note that the device looks at the PDEN status only at the $\overline{CS}$ rising edge; however, for continuous low-speed operation, it is convenient to continuously hold PDEN = 1. The RS1472 detects power-down mode on the $\overline{CS}$ rising edge with PDEN = 1.

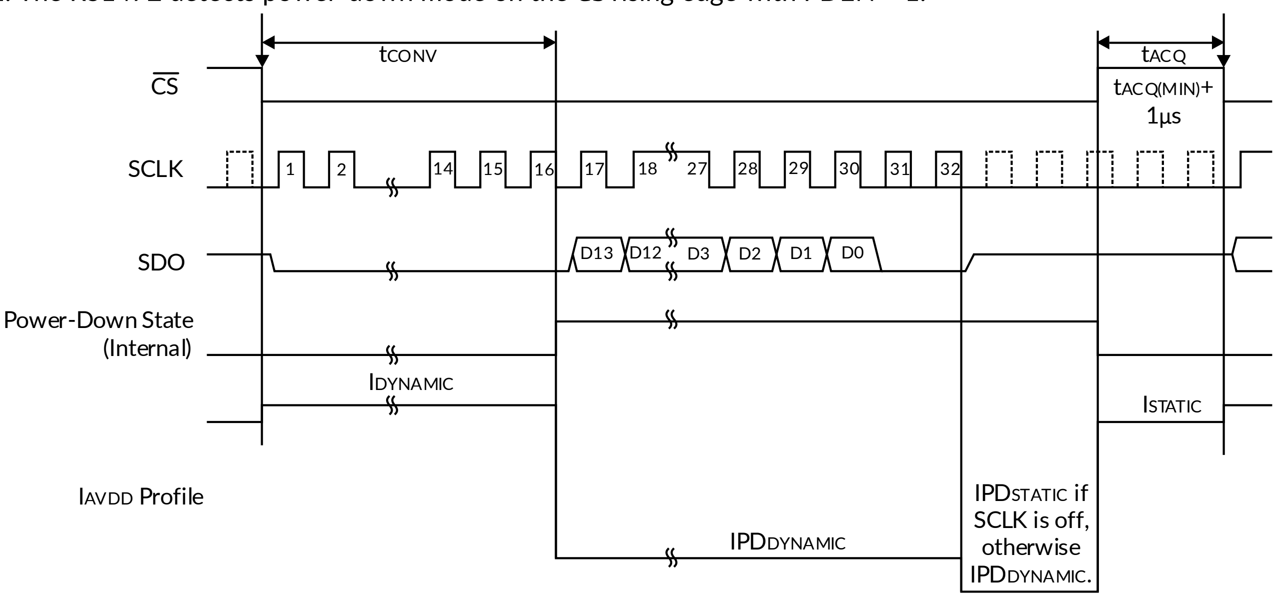


Figure 53. Power-Down Mode (PDEN = 1)

On the $\overline{CS}$ falling edge, the devices start normal operation as previously described. The devices complete conversions on the 16th SCLK falling edge. The devices enter the power-down state immediately after conversions complete. However, the devices can still output data as per the timings described previously. The devices consume dynamic power-down current (IPD-DYNAMIC) during data out operations. It is recommended to stop the clock after the 32nd SCLK falling edge to further save power down to the static power-down current level (IPD-STATIC). The devices power up again on the SCLK rising edge. However, they require an extra 0.5 µs to power up completely. $\overline{CS}$ must be high for the 0.5 µs period.
In some applications, data collection is accomplished in burst mode. The system powers down after data collection. 16-clock mode is convenient for these applications. Figure 54 and Figure 55 detail power saving in 16-clock burst mode.

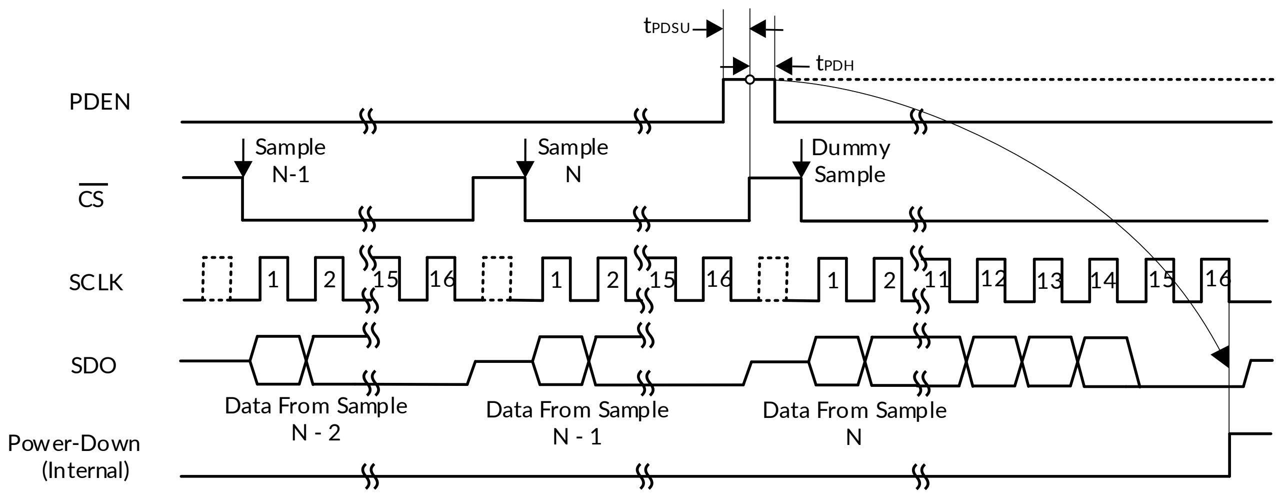


Figure 54. Entry Into Power-Down with 16-Clock Burst Mode

As shown in Figure 54, the two frames capturing the N−1 and Nth samples are normal 16-clock frames. Keeping PDEN = 1 before the $\overline{CS}$ rising edge in the next frame ensures that the devices detect the power-down mode. Data from the Nth sample are read during this frame. It is expected that the Nth sample represents the last data of interest in the burst of conversions. The devices enter the power-down state after the end of conversions. This is the 16th SCLK falling edge. It is recommended to stop the clock after the 16th SCLK falling edge. Note that it is mandatory not to have more than 29 SCLK falling edges during the $\overline{CS}$ low period. This limitation ensures that the devices remain in 16-clock mode.

The devices remain in a power-down state as long as $\overline{CS}$ is low. A $\overline{CS}$ rising edge with PDEN = 0 brings the devices out of the power-down state. It is necessary to ensure that the $\overline{CS}$ high time for the first sample after power up is more than 1 µs + t_{ACQ} (min).

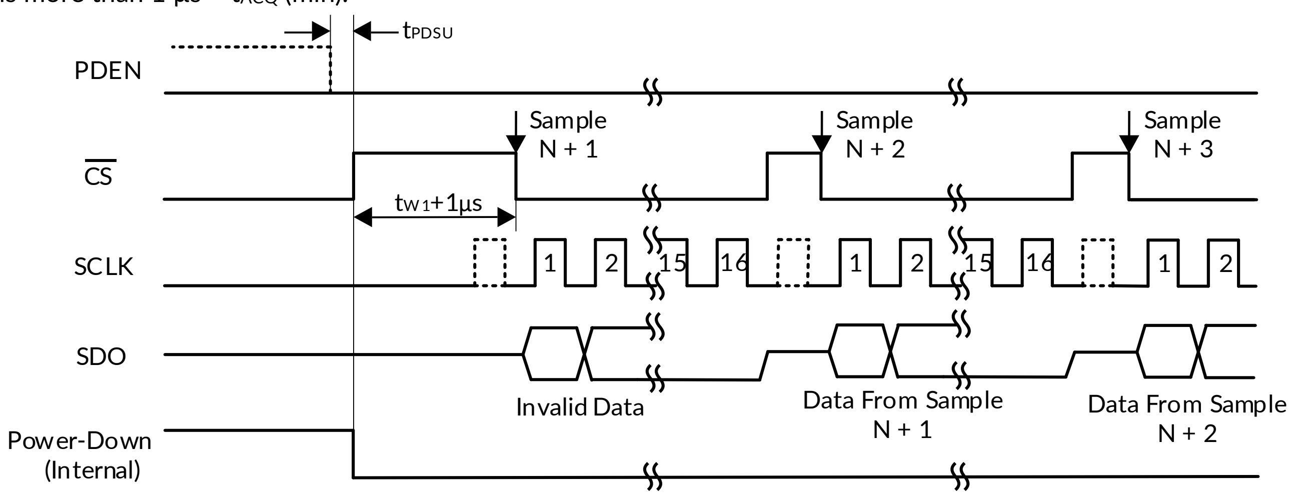


Figure 55. Exit From Power-Down with 16-Clock Burst Mode

9.5 APPLICATION INFORMATION

The RS1472 employs a sample-and-hold stage at the input. The device connects a 32 pF sampling capacitor during sampling. This configuration results in a glitch at the input terminals of the device at the start of the sample. The external circuit must be designed in such a way that the input can settle to the required accuracy during the sampling time chosen. Figure 56 shows a typical driving circuit for the analog inputs.

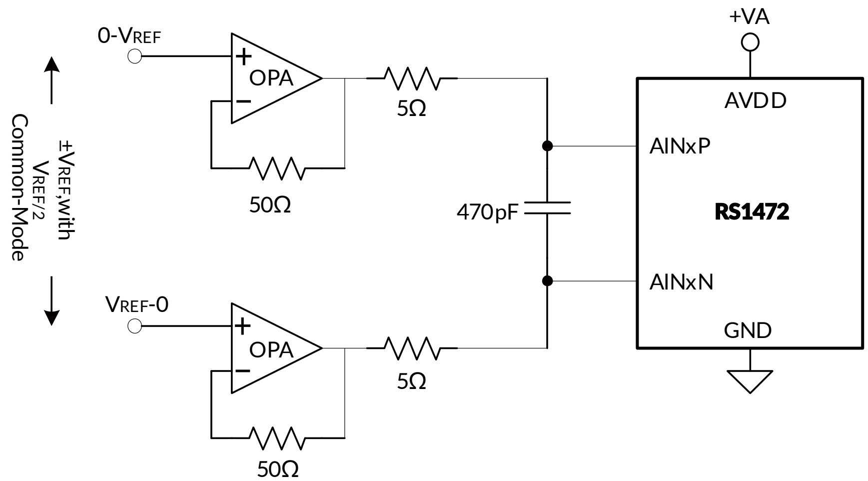


Figure 56. Typical Input Driving Circuit

The 470 pF capacitor across the AINxP and AINxN terminals decouples the driving op amp from the sampling glitch. It is recommended to split the series resistance of the input filter in two equal values as shown in Figure 56. It is recommended that both input terminals see the same impedance from the external circuit. The low-pass filter at the input limits noise bandwidth of the driving op amps. Select the filter bandwidth so that the full-scale step at the input can settle to the required accuracy during the sampling time. Equation 1, Equation 2, and Equation 3 are useful for filter component selection.

$$\text{Filter Time Constant } (t_{AU}) = \frac{\text{Sampling Time}}{\text{Setting Resolution} \times \ln(2)}$$

Where：

Settling resolution is the accuracy in LSB to which the input needs to settle. A typical settling resolution for the 14-bit device is 15 or 16. (1)

$$\text{Filter Time Constant } (t_{AU}) = R \times C \quad (2)$$

$$\text{Fiter Bandwidth} = \frac{1}{2 \times \Pi \times tAU} \quad (3)$$

Also, make sure the driving op amp bandwidth does not limit the signal bandwidth below filter bandwidth. In many applications, signal bandwidth may be much lower than filter bandwidth. In this case, an additional low-pass filter may be used at the input of the driving op amp. This signal filter bandwidth can be selected in accordance with the input signal bandwidth.

9.6 INPUT COMMON-MODE RANGE

The AIN+ and AIN– inputs to the RS1472 should typically vary between 0 V and VREF with a common-mode of VREF/2. The RS1472 offers excellent CMRR which makes it possible to achieve close to the rated performance of the converter even in cases where the common-mode input is not well-controlled. The device can accept a ±200 mV variation in the common-mode voltage at any VDD/VREF combination allowing use of the entire ADC signal range (–VREF to +VREF differentially).

9.7 DRIVING AN ADC WITHOUT A DRIVING OP AMP

For some low input signal bandwidth applications, such as battery power monitoring or mains monitoring, it is not required to operate an ADC at high sampling rates. In fact, it is desirable to avoid using a driving op amp from a cost perspective. In these cases, the ADC input sees the impedance of the signal source (such as a battery or mains transformer). This section elaborates the effects of source impedance on sampling frequency.

Equation 1 can be rewritten as Equation 4:

Sampling Time = Filter Time Constant × Settling Resolution × ln(2) (4)

As shown in Figure 57, it is recommended to use a bypass capacitor across the positive and negative ADC input terminals.

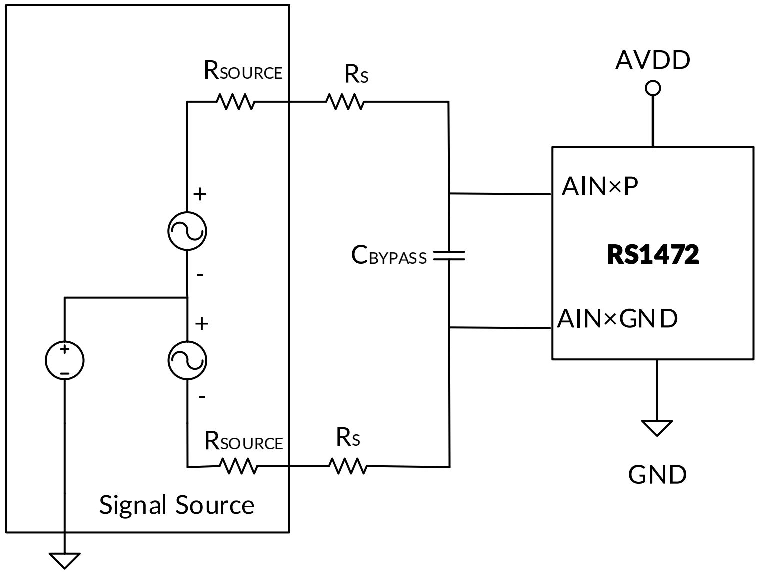


Figure 57. Driving an RS1472 ADC Without a Driving Op Amp

Source impedance ($2 \times R_{SOURCE} + 2 \times R_S$) with ($C_{BYPASS} + C_{SAMPLE}$) acts as a low-pass filter with Equation 5:

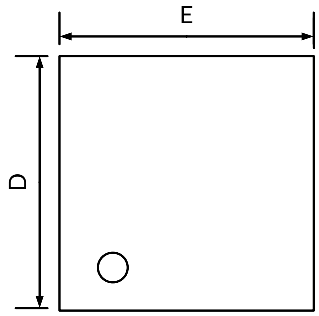
$$\text{Filter Time Constant} = 2 \times (R_{SOURCE} + R_S) \times (C_{BYPASS} + C_{SAMPLE}) \quad (5)$$

where:

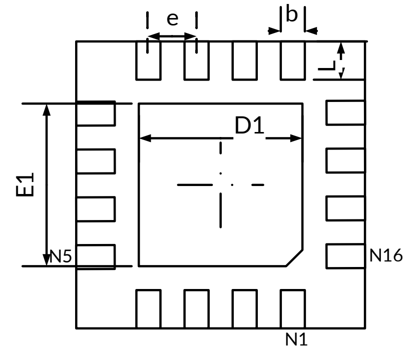
C_{SAMPLE} is the internal sampling capacitance of the ADC (equal to 36 pF).

10 PACKAGE OUTLINE DIMENSIONS

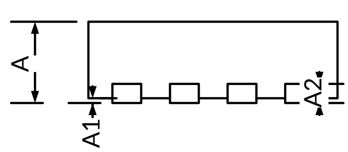
QFN3x3-16 (2)



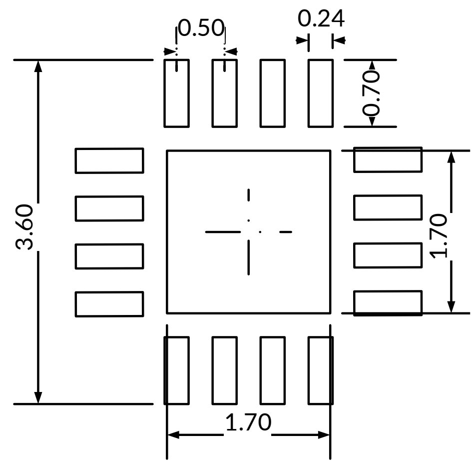
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

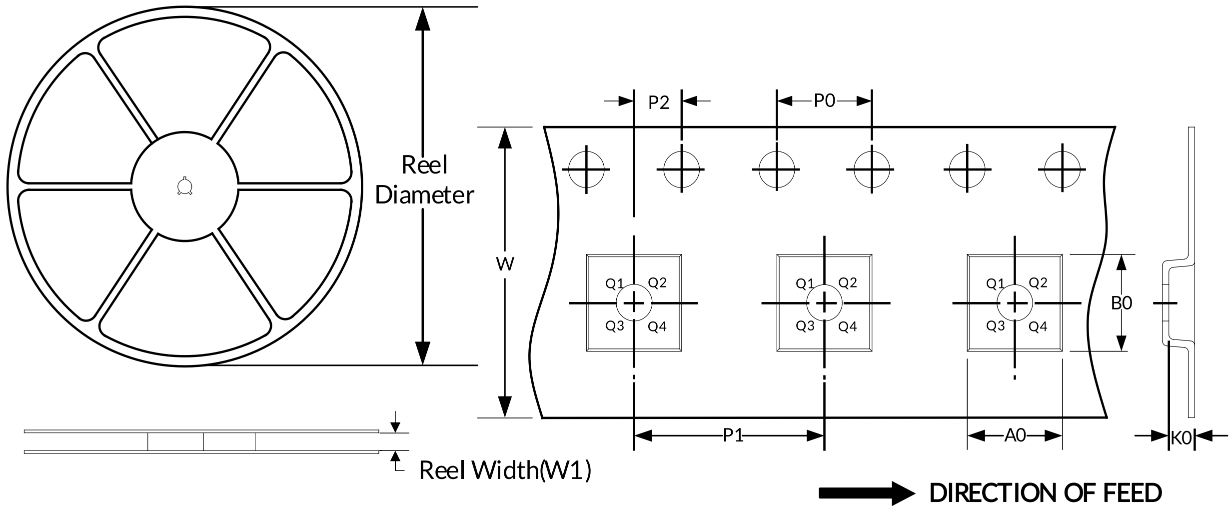
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203		0.008	
b	0.180	0.300	0.007	0.012
D (1)	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E (1)	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

NOTE:

1. Plastic or metal protrusions of 0.075mm maximum per side are not included.
2. This drawing is subject to change without notice.

11 TAPE AND REEL INFORMATION

REEL DIMENSIONS　　　TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
QFN3x3-16	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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