Octal Edge-Triggered D-Type Flip-Flops With 3-State Outputs

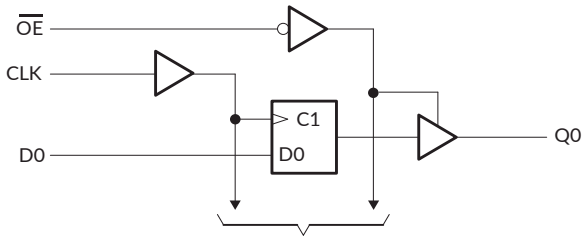
1 FEATURES

- **Operating Voltage Range: 2V to 5.5V**
- **Low Power Consumption: 40μA (Max)**
- **Operating Temperature Range: -40°C to +125°C**
- **3-State Outputs Drive Bus Lines Directly**
- **Micro SIZE PACKAGES: TSSOP-20, SOIC-20(SOP20)**

2 APPLICATIONS

- **Power Sub-station controls**
- **Industrial**
- **Personal electronics**
- **Test and Measurement Solutions**
- **Patient Monitoring**

Simplified Schematic



3 DESCRIPTIONS

The RS574 is high-speed octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A clock (CLK) and an output enable ($\overline{OE}$) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold times requirements on the low-to-high CLK transition. When $\overline{OE}$ is low the contents of the 8 flip-flops are available at the outputs. When $\overline{OE}$ is high, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

This device available in Green TSSOP-20, SOIC-20(SOP20) packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS574	TSSOP-20(20)	6.50mm×4.40mm
	SOIC-20 (SOP20)(20)	12.80mm×7.50mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.1	2023/08/23	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS574	RS574XS20	-40°C ~+125°C	SOIC-20 (SOP20)	RS574	MSL3	Tape and Reel,1500
	RS574XTSS20	-40°C ~+125°C	TSSOP-20	RS574	MSL3	Tape and Reel,4000

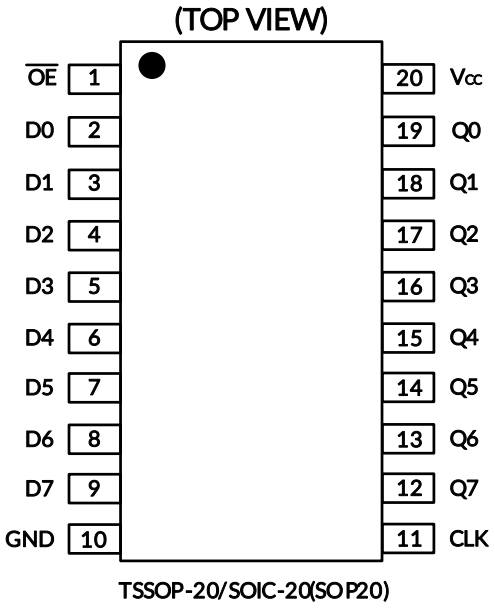
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

6 PIN CONFIGURATIONS



TSSOP-20/SOIC-20(SOP20)

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
TSSOP-20/SOIC-20(SOP20)			
1	$\overline{OE}$	I	3-State output enable input
2	D0	I	Data input
3	D1	I	Data input
4	D2	I	Data input
5	D3	I	Data input
6	D4	I	Data input
7	D5	I	Data input
8	D6	I	Data input
9	D7	I	Data input
10	GND	G	Ground.
11	CLK	I	Clock input
12	Q7	O	Data output
13	Q6	O	Data output
14	Q5	O	Data output
15	Q4	O	Data output
16	Q3	O	Data output
17	Q2	O	Data output
18	Q1	O	Data output
19	Q0	O	Data output
20	V_{CC}	P	Supply voltage

(1) I=input, O=output, P=power.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings (1)

over operating free-air temperature range (unless otherwise noted) (1) (2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range (2)		-0.5	6.5	V
Vo	Output Voltage range (2)		-0.5	V_{CC}+0.5	V
I_{IK}	Input clamp current	V_I<0		-20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
θ_{JA}	Package thermal impedance (3)	SOIC-20(SOP20)		40	°C/W
		TSSOP-20		40	
T_J	Junction temperature (4)		-65	150	°C
Tstg	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD-51.

(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	
		Machine Model (MM), JESD22-A115C (2010)	±200	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8 ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at T_A = +25°C, Full=-40°C to 125°C, unless otherwise noted.) (1)

8.1 Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}		2	5.5	V
High-level input voltage	V_{IH}	V_{CC}=2V	1.5		V
		V_{CC}=3V	2.1		
		V_{CC}=5.5V	3.85		
Low-level input voltage	V_{IL}	V_{CC}=2V		0.5	V
		V_{CC}=3V		0.9	
		V_{CC}=5.5V		1.65	
Input voltage	V_I		0	5.5	V
Output voltage	V_O		0	V_{CC}	V
High-level output current	I_{OH}	V_{CC}=2V		-50	μA
		V_{CC}=3V to 3.6V		-8	mA
		V_{CC}=4.5V to 5.5V		-16	
Low-level output current	I_{OL}	V_{CC}=2V		50	μA
		V_{CC}=3V to 3.6V		8	mA
		V_{CC}=4.5V to 5.5V		16	
Input transition rise or fall rate	Δt / Δv	V_{CC}=3V to 3.6V		100	ns/V
		V_{CC}=4.5V to 5.5V		20	
Operating temperature	T_A		-40	+125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

8.2 DC Characteristics

PARAMETER	TEST CONDITIONS	V_{CC}	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OH}	I_{OH} = -50μA	2V to 5.5V	Full	V_{CC}-0.1			V
	I_{OH} = -4mA	3V		2.8			
	I_{OH} = -8mA	4.5V		4.15			
	I_{OH} = -16mA	5.5V		5.1			
V_{OL}	I_{OL} = 50μA	2V to 5.5V	Full			0.1	V
	I_{OL} = 4mA	3V				0.2	
	I_{OL} = 8mA	4.5V				0.2	
	I_{OL} = 16mA	5.5V				0.5	
I_I	V_I=5.5V or GND	0V to 5.5V	+25°C			±1	μA
			Full			±2	
I_{OZ} (4)	V_O=V_{CC} or GND	5.5	+25°C			±1	μA
			Full			±2.5	
I_{CC}	V_I= V_{CC} or GND, I_O=0	5.5V	+25°C			4	μA
			Full			40	
C_i (Input Capacitance)	V_I = V_{CC} or GND	5V	+25°C		6		pF
C_O (Output Capacitance)	V_O = V_{CC} or GND	5V	+25°C		6		pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) For input and output pins, I_{OZ} includes the input leakage current.

8.3 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER	TEMP	V_{CC}=3.3V ± 0.3V		V_{CC}=5V ± 0.5V		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration, CLK high or low	25°C	7		7		ns
		Full	7.5		7.5		
t_{su}	Setup time, data before CLKt	25°C	-4		-4		ns
		Full	-4.5		-4.5		
t_h	Hold time, data after CLKt	25°C	6		5		ns
		Full	6.5		5.5		

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.4 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TEMP	V_{CC}=3.3V ± 0.3V			V_{CC}=5V ± 0.5V			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CLK	Q	C_L= 15 pF	25°C		11			10		ns
				Full	5.5		20	5		18	
t_{PHL}	CLK	Q	C_L= 15 pF	25°C		11			10		ns
				Full	5.5		20	5		18	
t_{PZH}	$\overline{OE}$	Q	C_L= 15 pF	25°C		11			7		ns
				Full	5.5		20	3.5		14	
t_{PZL}	$\overline{OE}$	Q	C_L= 15 pF	25°C		8			6		ns
				Full	4		16	3		12	
t_{PHZ}	$\overline{OE}$	Q	C_L= 15 pF	25°C		12			8		ns
				Full	6		22	4		16	
t_{PLZ}	$\overline{OE}$	Q	C_L= 15 pF	25°C		11			7		ns
				Full	5.5		20	3.5		14	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

8.5 Operating Characteristics

T_A = +25°C

PARAMETER	TEST CONDITIONS	V_{CC} = 5V	UNIT
		TYP	
C_{pd} Power dissipation capacitance	No load, f = 1 MHz	20	pF

8.6 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At T_A = +25℃, unless otherwise noted.

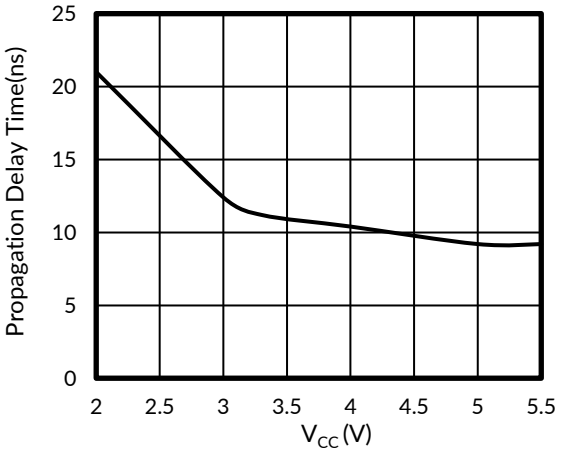


Figure 1. TPD vs V_{CC}

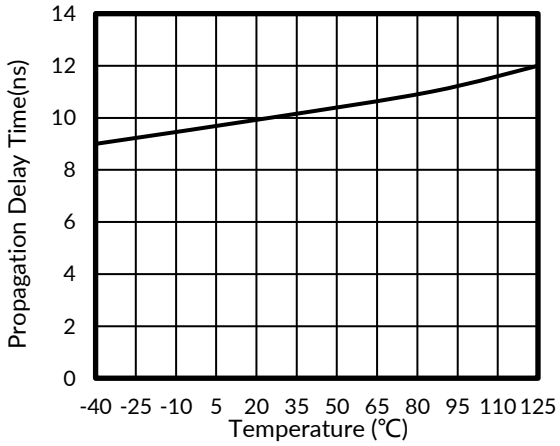
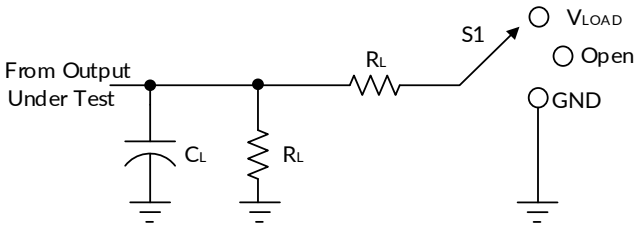
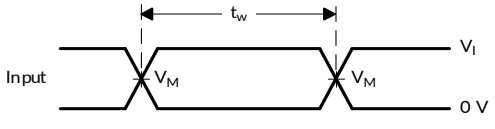


Figure 2. TPD vs Temperature

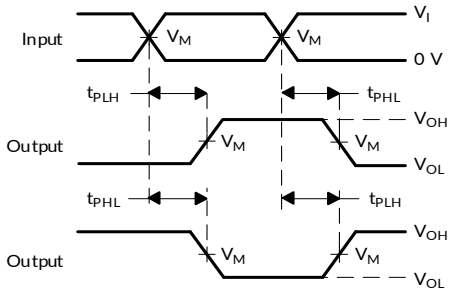
9 Parameter Measurement Information



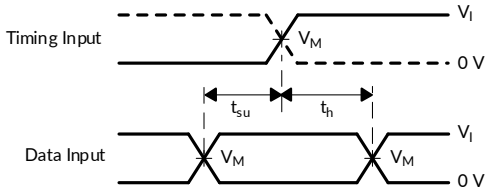
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND



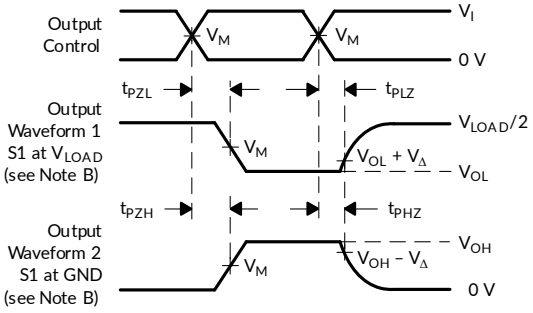
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY
TIMES INVERTION AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES
LOW-AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

10 Detailed Description

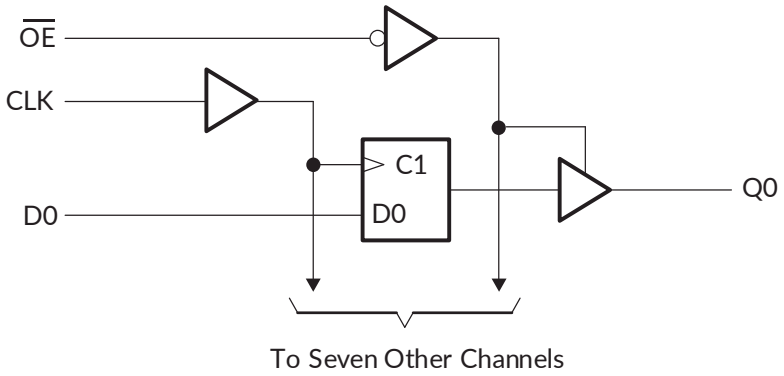
10.1 Overview

The RS574 devices are octal edge-triggered D-type flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels of the data (D) inputs. The states of the Q outputs are not predictable until the first valid clock.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pull-up components.

10.2 Functional Block Diagram



10.3 Feature Description

- 5.5V tolerant input allows for 5 V to 3.3 V voltage translation
- Slow edges reduce output ringing

10.4 Device Functional Modes

Table 1. Function Table (Each Flip-Flop)

INPUT			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

11 Application and Implementation

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

RS574 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid VCC making it Ideal for down translation.

11.2 Typical Application

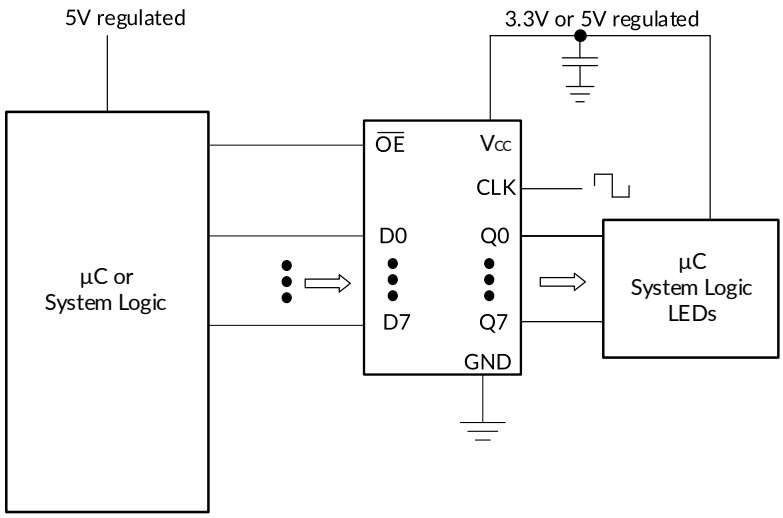


Figure 4. Typical Application Schematic

11.3 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

12 Power Supply Recommendations

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1uF capacitor is recommended and if there are multiple V_{CC} terminals then 0.01uF or 0.022uF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

13 Layout

13.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Figure 5 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/O_S so they also cannot float when disabled.

13.2 Layout Example

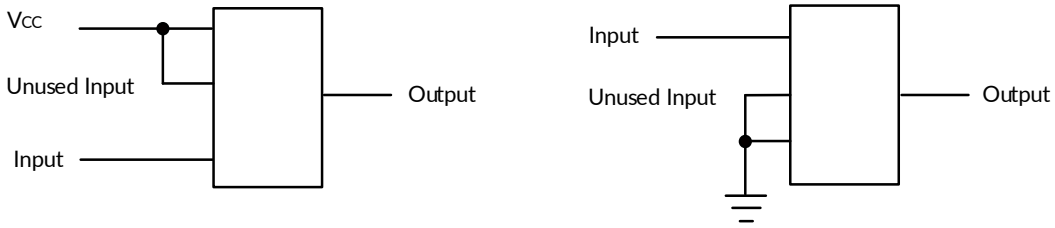
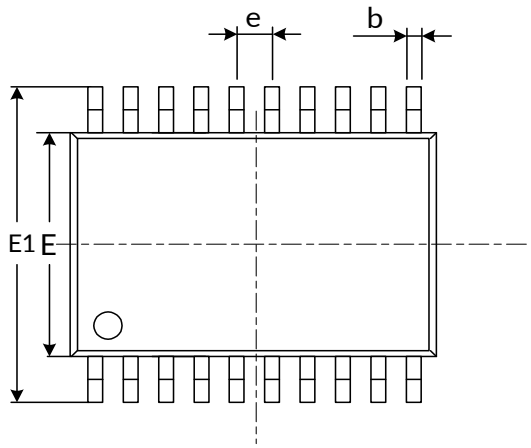
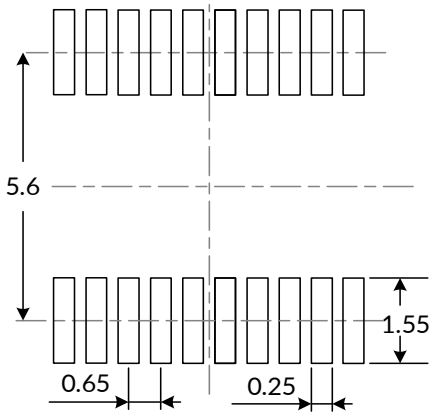


Figure 5. Layout Diagram

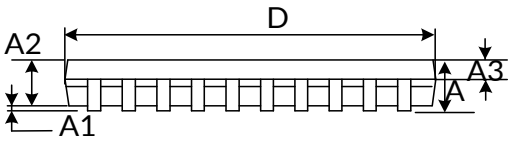
14 PACKAGE OUTLINE DIMENSIONS

TSSOP-20 (4)





RECOMMENDED LAND PATTERN (Unit: mm)

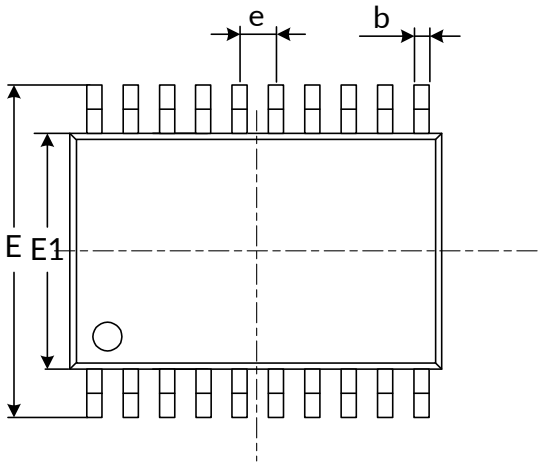


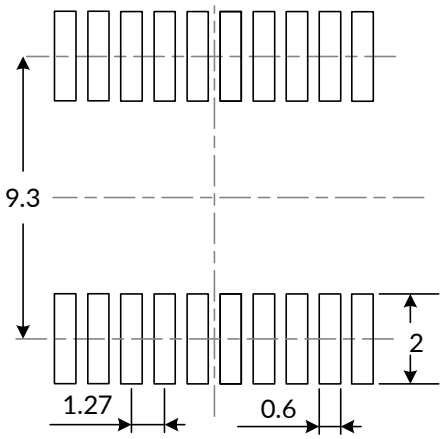
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
A3	0.390	0.490	0.015	0.020
b	0.200	0.290	0.008	0.011
c	0.130	0.170	0.005	0.007
D (1)	6.400	6.600	0.252	0.260
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.450	0.750	0.018	0.030
H	0.250(TYP)		0.010(TYP)	
θ	0°	8°	0°	8°
L1	1.00(REF) (3)		0.039(REF) (3)	

NOTE:

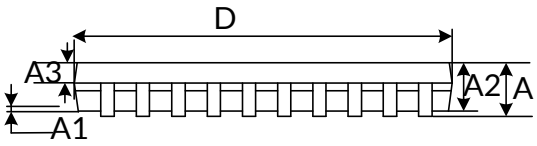
1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

SOIC-20(SOP20) (4)





RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		2.650		0.104
A1	0.100	0.300	0.004	0.012
A2	2.250	2.350	0.089	0.093
A3	0.970	1.070	0.038	0.042
b	0.390	0.470	0.015	0.019
c	0.250	0.290	0.010	0.011
D (1)	12.700	12.900	0.500	0.508
E	10.100	10.500	0.398	0.413
E1 (1)	7.400	7.600	0.291	0.299
e	1.270(BSC) (2)		0.050(BSC) (2)	
L	0.700	1.000	0.028	0.039
H	0.250(TYP)		0.010(TYP)	
θ	0°	8°	0°	8°
L1	1.400(REF) (3)		0.055(REF) (3)	

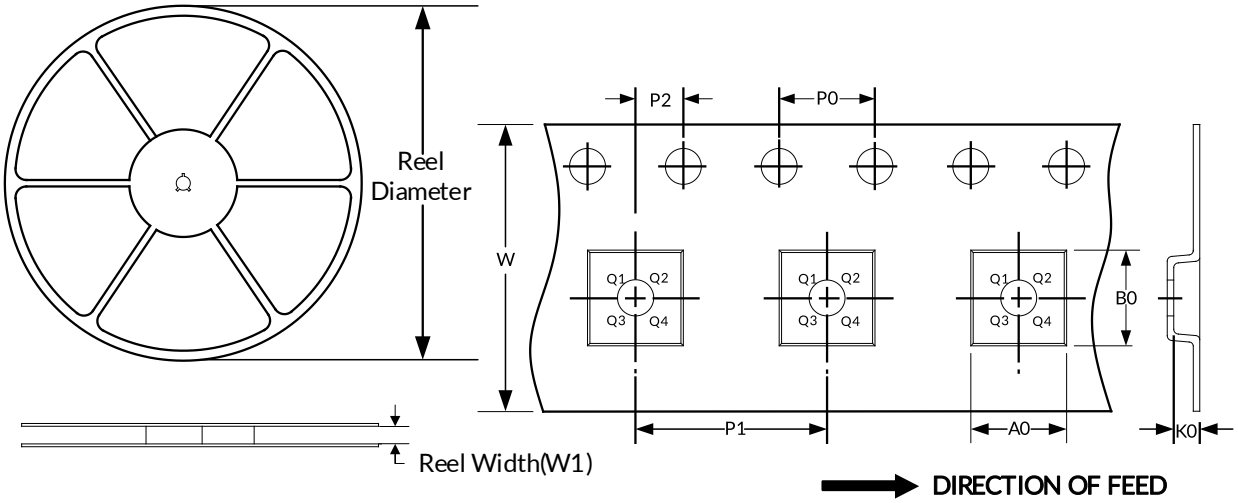
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

15 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-20	13”	12.4	6.75	6.95	1.20	4.0	8.0	2.0	12.0	Q1
SOIC-20(SOP20)	13”	24.4	10.75	13.55	2.65	4.0	12.0	2.0	24.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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