

13MHz, Rail-to-Rail I/O CMOS Operational Amplifier

1 FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Grade 1
- HIGH GAIN BANDWIDTH: 13MHz
- RAIL-TO-RAIL INPUT AND OUTPUT
±0.5mV Typical Vos
- INPUT VOLTAGE RANGE: -0.1V to +5.6V
with $V_S = 5.5V$
- SUPPLY RANGE: +2.5V to +5.5V
- SPECIFIED UP TO +125°C
- Micro SIZE PACKAGES: SOT23-5, SOIC-8

2 APPLICATIONS

- SENSORS
- PHOTODIODE AMPLIFICATION
- ACTIVE FILTERS
- TEST EQUIPMENT
- DRIVING A/D CONVERTERS

3 DESCRIPTIONS

The RS72XP-Q1 families of products offer low voltage operation and rail-to-rail input and output, as well as excellent speed/power consumption ratio, providing an excellent bandwidth (13MHz) and slew rate of 8V/us. The op-amps are unity gain stable and feature an ultra-low input bias current.

The devices are ideal for sensor interfaces, active filters and portable applications. The RS72XP-Q1 families of operational amplifiers are specified at the full temperature range of -40°C to +125°C under single or dual power supplies of 2.5V to 5.5V.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS721P-Q1	SOT23-5	2.92mm×1.62mm
RS722P-Q1	SOIC-8(SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm
RS724P-Q1	SOIC-14 (SOP14)	8.65mm×3.90mm
	TSSOP-14	5.00mm×4.40mm
	QFN3x3-16L	3.00mm×3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Note: Page numbers for previous revisions may differ from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2022/07/26	Initial version completed

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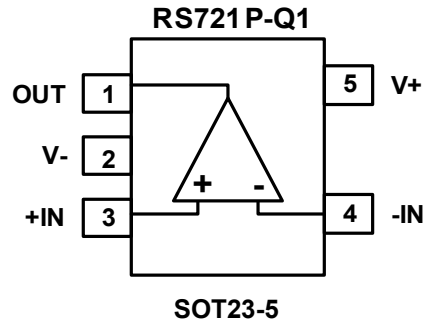
5 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Pin	Channel	Lead finish/Ball material (2)	MSL Peak Temp (3)	Op Temp(°C)	Device Marking (4)	Package Qty
RS721PXF-Q1	SOT23-5	5	1	NIPDAUAG	MSL1-260°-Unlimited	-40°C ~125°C	721P	Tape and Reel,3000
RS722P XK-Q1	SOIC-8 (SOP8)	8	2	NIPDAUAG	MSL1-260°-Unlimited	-40°C ~125°C	RS722P	Tape and Reel,4000
RS722PXM-Q1	MSOP-8	8	2	NIPDAUAG	MSL1-260°-Unlimited	-40°C ~125°C	RS722P	Tape and Reel,4000
RS724PXP-Q1	SOIC-14 (SOP14)	14	4	NIPDAUAG	MSL1-260°-Unlimited	-40°C ~125°C	RS724P	Tape and Reel,4000
RS724PXQ-Q1	TSSOP-14	14	4	NIPDAUAG	MSL1-260°-Unlimited	-40°C ~125°C	RS724P	Tape and Reel,4000
RS724PXT QC16-Q1	QFN3x3-16L	16	4	NIPDAUAG	MSL1-260°-Unlimited	-40°C ~125°C	RS724P	Tape and Reel,5000

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.
- (2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (3) MSL Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

6 Pin Configuration and Functions (Top View)

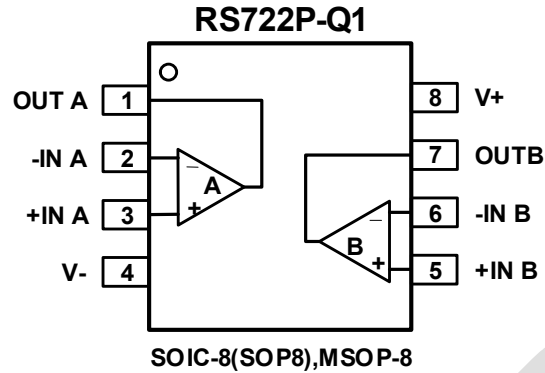


Pin Description

NAME	PIN		I/O ⁽¹⁾	DESCRIPTION
	RS721P-Q1			
	SOT23-5			
-IN	4	I	Negative (inverting) input	
+IN	3	I	Positive (noninverting) input	
OUT	1	O	Output	
V-	2	-	Negative (lowest) power supply	
V+	5	-	Positive (highest) power supply	

(1) I = Input, O = Output, P = Power.

Pin Configuration and Functions (Top View)

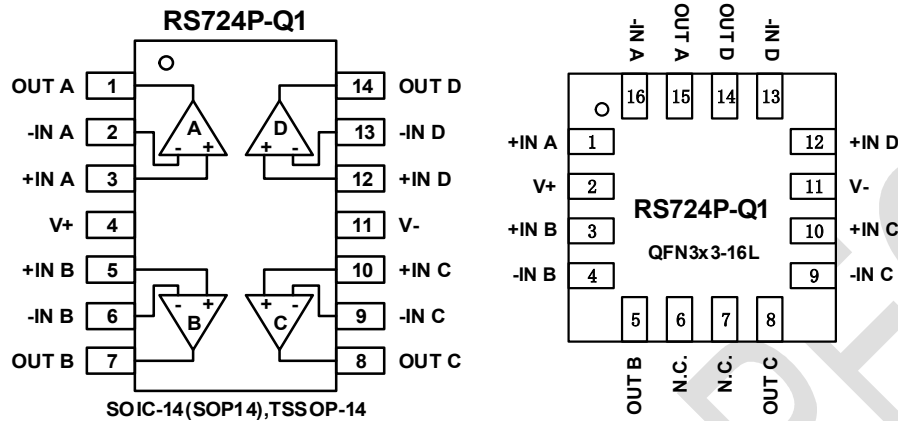


Pin Description

NAME	PIN		I/O ⁽¹⁾	DESCRIPTION
	RS722P-Q1			
	SOIC-8(SOP8)/MSOP-8			
-INA	2	I	Inverting input, channel A	
+INA	3	I	Noninverting input, channel A	
-INB	6	I	Inverting input, channel B	
+INB	5	I	Noninverting input, channel B	
OUTA	1	O	Output, channel A	
OUTB	7	O	Output, channel B	
V-	4	-	Negative (lowest) power supply	
V+	8	-	Positive (highest) power supply	

(1) I = Input, O = Output, P = Power.

Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN		I/O ⁽¹⁾	DESCRIPTION
	SOIC-14(SOP14)/TSSOP-14	QFN3x3-16L		
-INA	2	16	I	Inverting input, channel A
+INA	3	1	I	Noninverting input, channel A
-INB	6	4	I	Inverting input, channel B
+INB	5	3	I	Noninverting input, channel B
-INC	9	9	I	Inverting input, channel C
+INC	10	10	I	Noninverting input, channel C
-IND	13	13	I	Inverting input, channel D
+IND	12	12	I	Noninverting input, channel D
OUTA	1	15	O	Output, channel A
OUTB	7	5	O	Output, channel B
OUTC	8	8	O	Output, channel C
OUTD	14	14	O	Output, channel D
V-	11	11	-	Negative (lowest) power supply
V+	4	2	-	Positive (highest) power supply

(1) I = Input, O = Output, P = Power.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
Voltage	Supply, $V_S=(V+) - (V-)$		7	V
	Signal input pin ⁽²⁾	(V-)-0.5	(V+) +0.5	
	Signal output pin ⁽³⁾	(V-)-0.5	(V+) +0.5	
Current	Signal input pin ⁽²⁾	-10	10	mA
	Signal output pin ⁽³⁾	-200	200	mA
	Output short-circuits ⁽⁴⁾	Continuous		
Temperature	Operating range, T_A	-40	125	°C
	Junction, T_J ⁽⁵⁾	-40	150	
	Storage, T_{stg}	-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ± 200 mA or less.

(4) Short-circuit to ground, one amplifier per package.

(5) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), per AEC Q100-002 ⁽¹⁾	± 2000	V
		Charged-Device Model (CDM), per AEC Q100-011	± 500	
		Latch-Up (LU), per AEC Q100-004	± 100	mA

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.



ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Supply voltage, $V_S=(V+) - (V-)$	Single-supply	2.5		5.5	V
	Dual-supply	± 1.25		± 2.75	

7.4 Thermal Information: RS721P-Q1

THERMAL METRIC ⁽¹⁾		RS721P-Q1		UNIT
		5PINS		
		SOT23-5		
R _{θJA}	Junction-to-ambient thermal resistance	273.8		°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	126.8		°C/W
R _{θJB}	Junction-to-board thermal resistance	85.9		°C/W
Ψ _{JT}	Junction-to-top characterization parameter	10.9		°C/W
Ψ _{JB}	Junction-to-board characterization parameter	84.9		°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A		°C/W

(1) Thermal resistance varies with operating conditions.

7.5 Thermal Information: RS722P-Q1

THERMAL METRIC ⁽¹⁾		RS722P-Q1		UNIT
		8PINS		
		SOIC-8(SOP8)	MSOP-8	
R _{θJA}	Junction-to-ambient thermal resistance	116	165	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	60	53	°C/W
R _{θJB}	Junction-to-board thermal resistance	56	87	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	12.8	4.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	98.3	85	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) Thermal resistance varies with operating conditions.

7.6 Thermal Information: RS724P-Q1

THERMAL METRIC ⁽¹⁾		RS724P-Q1			UNIT
		14PINS		16PINS	
		SOIC-14 (SOP14)	TSSOP-14	QFN3×3-16L	
R _{θJA}	Junction-to-ambient thermal resistance	83.8	120.8	68.5	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	70.7	34.3	70.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	59.5	62.8	42.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	11.6	1	5.3	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	37.7	56.5	40.9	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) Thermal resistance varies with operating conditions.

7.7 ELECTRICAL CHARACTERISTICS

(At $T_A = +25^\circ\text{C}$, $V_S = 2.5\text{V}$ to 5.5V , $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, Full ⁽⁹⁾ = -40°C to $+125^\circ\text{C}$, unless otherwise noted.) ⁽¹⁾

PARAMETER	CONDITIONS	T_J	RS72XP-Q1				
			MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT	
POWER SUPPLY							
V_S	Operating Voltage Range	25°C	2.5		5.5		V
IQ	Quiescent Current/Amplifier	$V_S = \pm 2.5\text{V}$, $I_o = 0\text{mA}$	25°C		1.15	1.35	mA
			Full			1.85	
PSRR	Power-Supply Rejection Ratio	$V_S = 2.7\text{V}$ to 5.5V	25°C	75	93		dB
			Full	70	90		
INPUT							
V_{OS}	Input Offset Voltage	$V_{CM} = V_S/2$	25°C	-2.5	± 0.5	2.5	mV
$V_{OS} T_C$	Input Offset Voltage Average Drift		Full		± 2.6		$\mu\text{V}/^\circ\text{C}$
IB	Input Bias Current ⁽⁴⁾	$V_{CM} = 0\text{V}$	25°C		± 1	± 10	pA
			Full		0.5		nA
$I_{OS}^{(5)}$	Input Offset Current	$V_{CM} = 0\text{V}$	25°C		± 1	± 10	pA
V_{CM}	Common-Mode Voltage Range	$V_S = 5.5\text{V}$	25°C	-0.1		5.6	V
CMRR	Common-Mode Rejection Ratio	$V_S = 5.5\text{V}$, $V_{CM} = -0.1\text{V}$ to 3.5V	25°C	73	90		dB
			Full	70	85		
			25°C	60	77		
			Full	59	75		
OUTPUT							
A _{OL}	Open-Loop Voltage Gain	$R_L = 10\text{k}\Omega$, $V_o = (V_-) + 0.1\text{V}$ to $(V_+) - 0.1\text{V}$	25°C	110	127		dB
			Full	94	120		
	Output Swing from Rail	$V_S = \pm 2.5\text{V}$, $R_L = 10\text{k}\Omega$	25°C		10	20	mV
I_{OUT}	Output Short-Circuit Current ⁽⁶⁾⁽⁷⁾	$V_S = \pm 2.5\text{V}$, $V_o = 0\text{V}$	25°C	80	150		mA
C_{LOAD}	Capacitive Load Drive		25°C		100		pF
FREQUENCY RESPONSE							
SR	Slew Rate ⁽⁸⁾	$G = +1$, $C_L = 100\text{pF}$	25°C		8		V/ μs
GBP	Gain-Bandwidth Product		25°C		13		MHz
t_S	Setting Time, 0.1%	$V_S = \pm 2.5\text{V}$, $G = +1$, $C_L = 100\text{pF}$, Step = 2V	25°C		0.8		μs
t_{OR}	Overload Recovery Time	$V_{IN} \cdot \text{Gain} \geq V_S$, $G = -10$	25°C		0.4		μs
NOISE							
E_n	Input Voltage Noise	$f = 0.1\text{Hz}$ to 10Hz , $V_S = \pm 2.5\text{V}$	25°C		5		μV_{PP}

NOTE:

- (1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
- (2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
- (4) Positive current corresponds to current flowing into the device.
- (5) This parameter is ensured by design and/or characterization and is not tested in production.
- (6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A . The maximum allowable power dissipation at any ambient temperature is $PD = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
- (7) Short circuit test is a momentary test.
- (8) Number specified is the slower of positive and negative slew rates.
- (9) Specified by characterization only.

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7.8 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, $V_{OUT} = V_S/2$, unless otherwise noted.

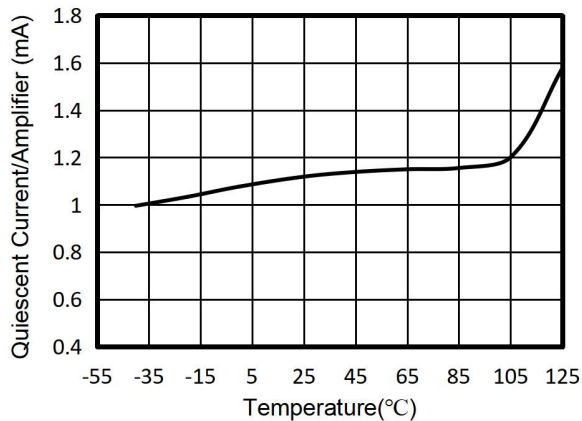


Figure 1. Quiescent Current vs Temperature

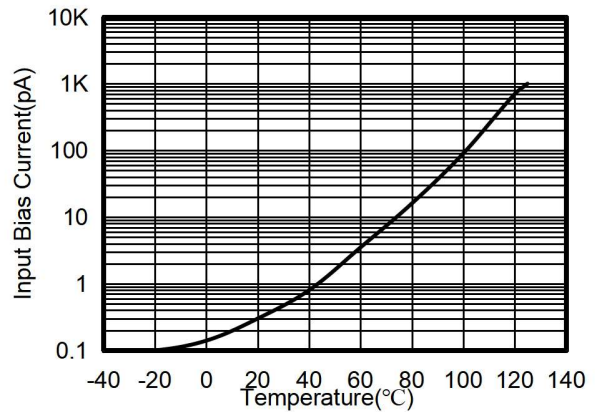


Figure 2. Input Bias Current vs Temperature

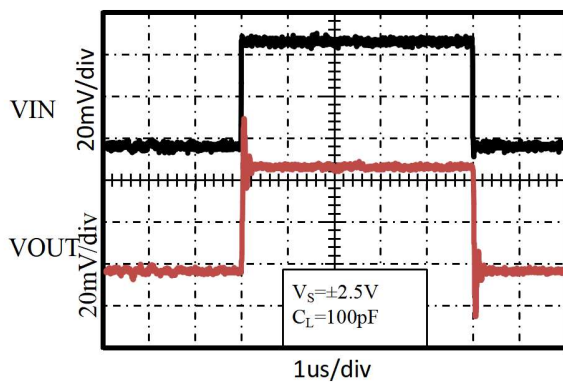


Figure 3. Small-Signal Step Response

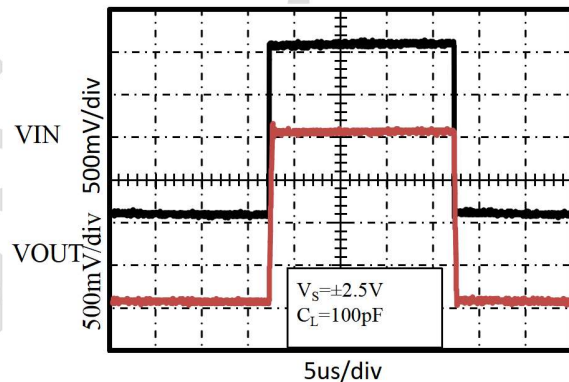


Figure 4. Large-Signal Step Response

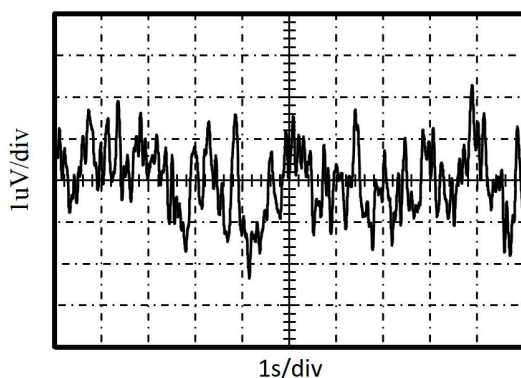


Figure 5. 0.1Hz to 10Hz Input Voltage Noise

8 Detailed Description

8.1 Overview

The RS721P-Q1, RS722P-Q1, RS724P-Q1 are high precision, rail-to-rail operational amplifiers that can be run from a single-supply voltage 2.5V to 5.5V ($\pm 1.25V$ to $\pm 2.75V$). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Good layout practice mandates use of a 0.1 μF capacitor place closely across the supply pins.

8.2 Phase Reversal Protection

The RS72XP-Q1 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the RS72XP-Q1 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in figure 6.

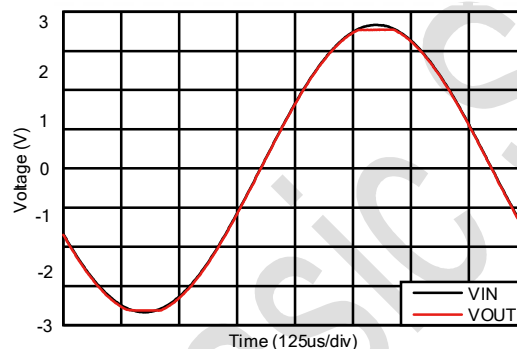


Figure 6. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

8.3 EMIRR IN+ Test Configuration

Figure 7 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input pin using a transmission line. The operational amplifier is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that can interfere with multimeter accuracy.

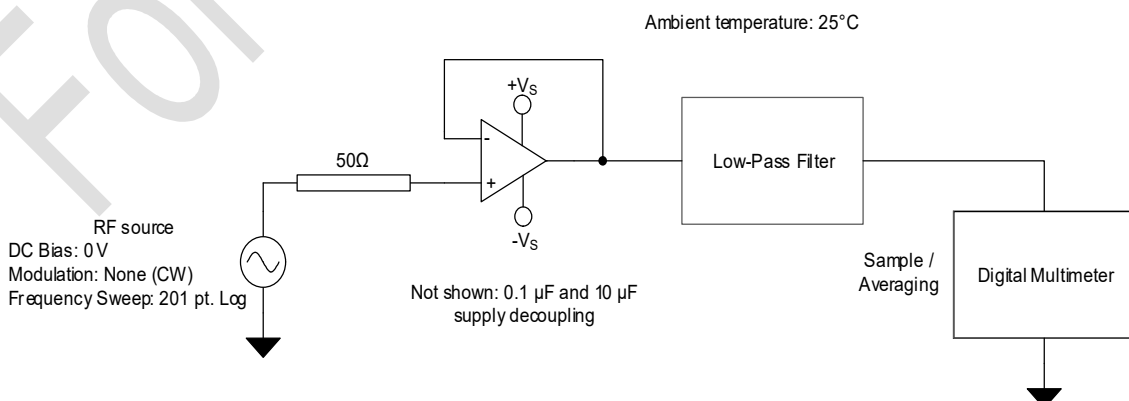


Figure 7. EMIRR IN+ Test Configuration Schematic

9 Application and Implementation

Information in the following applications sections is not part of the Runic component specification, and Runic does not warrant its accuracy or completeness. Runic's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 APPLICATION NOTE

The RS72XP-Q1 are high precision, rail-to-rail operational amplifiers that can be run from a single-supply voltage 2.5V to 5.5V ($\pm 1.25V$ to $\pm 2.75V$). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. Good layout practice mandates use of a 0.1 μ F capacitor placed closely across the supply pins.

Typical Applications

9.2 25-kHz Low-pass Filter

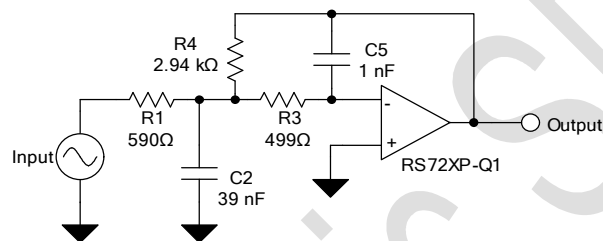


Figure 8. 25-kHz Low-Pass Filter

9.3 Design Requirements

Low-pass filters are commonly employed in signal processing applications to reduce noise and prevent aliasing. The RS72XP-Q1 devices are ideally suited to construct high-speed, high-precision active filters. Figure 8 shows a second-order, low-pass filter commonly encountered in signal processing applications.

Use the following parameters for this design example:

- Gain = 5 V/V (inverting gain)
- Low-pass cutoff frequency = 25 kHz
- Second-order Chebyshev filter response with 3-dB gain peaking in the passband.

9.4 Detailed Design Procedure

The infinite-gain multiple-feedback circuit for a low-pass network function is shown in Figure 8. Use Equation 1 to calculate the voltage transfer function.

$$\frac{\text{Output}}{\text{Input}}(s) = \frac{-1/R_1 R_3 C_2 C_5}{s^2 + (s/C_2)(1/R_1 + 1/R_3 + 1/R_4) + 1/R_3 R_4 C_2 C_5} \quad (1)$$

This circuit produces a signal inversion. For this circuit, the gain at dc and the low-pass cutoff frequency are calculated by Equation 2:

$$\text{Gain} = \frac{R_4}{R_1}$$

$$f_c = \frac{1}{2\pi} \sqrt{(1/R_3 R_4 C_2 C_5)} \quad (2)$$

9.5 Application Curve

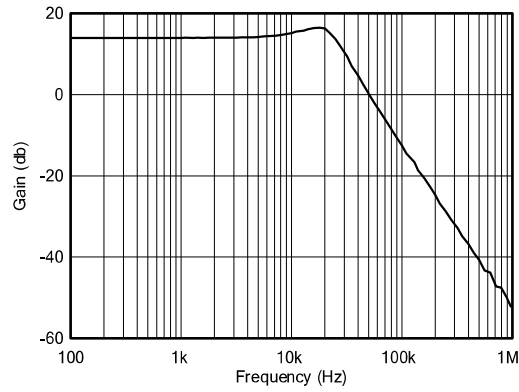


Figure 9. Low-pass filter transfer function

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10 LAYOUTS

10.1 Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1 μ F capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the EMI susceptibility.

10.2 Layout Example

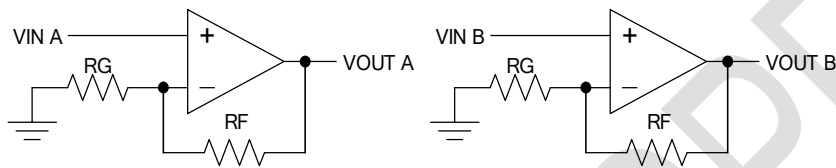


Figure 10. Schematic Representation

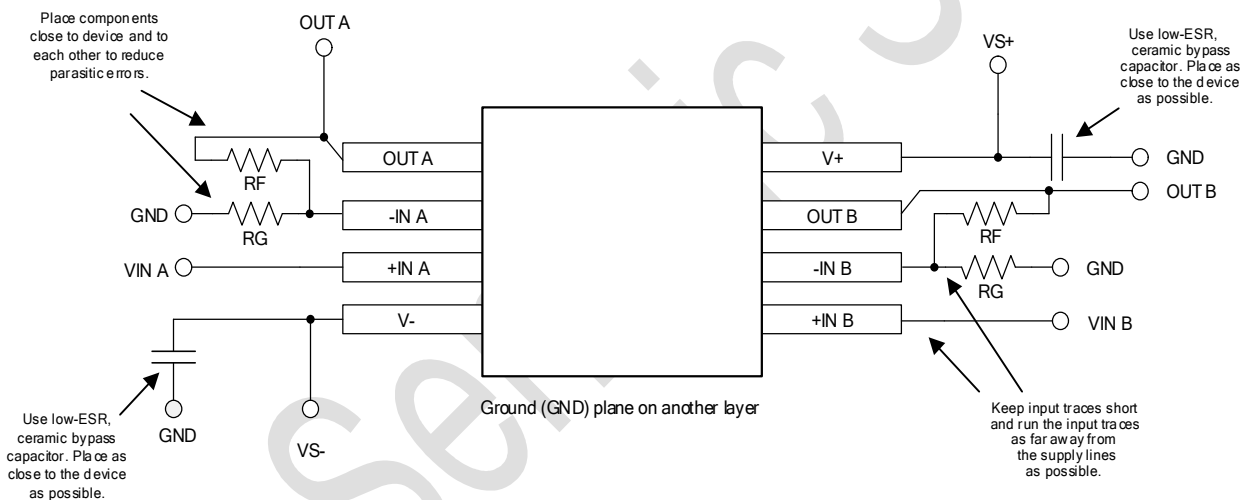
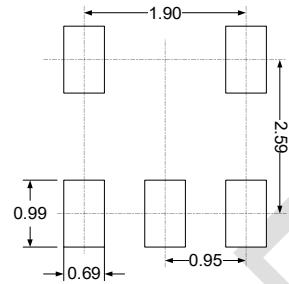
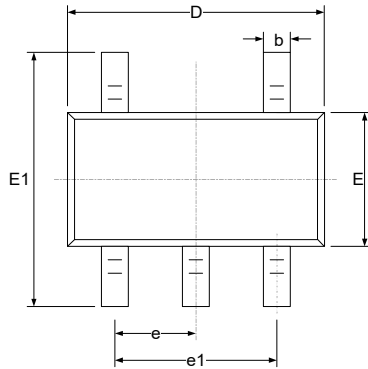
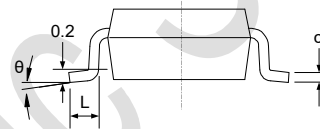
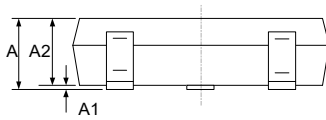
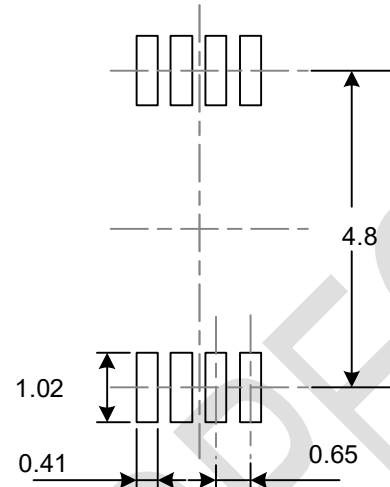
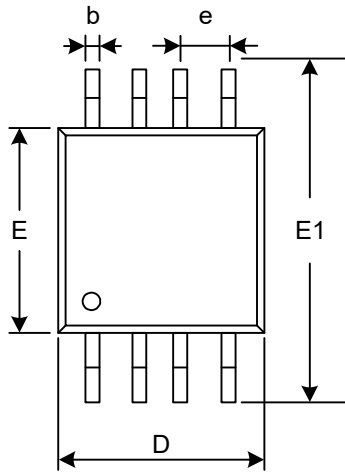
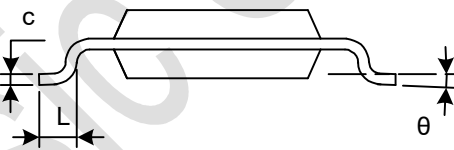
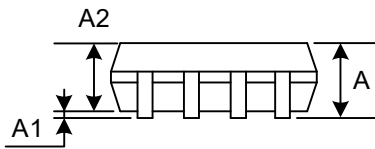


Figure 11. Layout Example

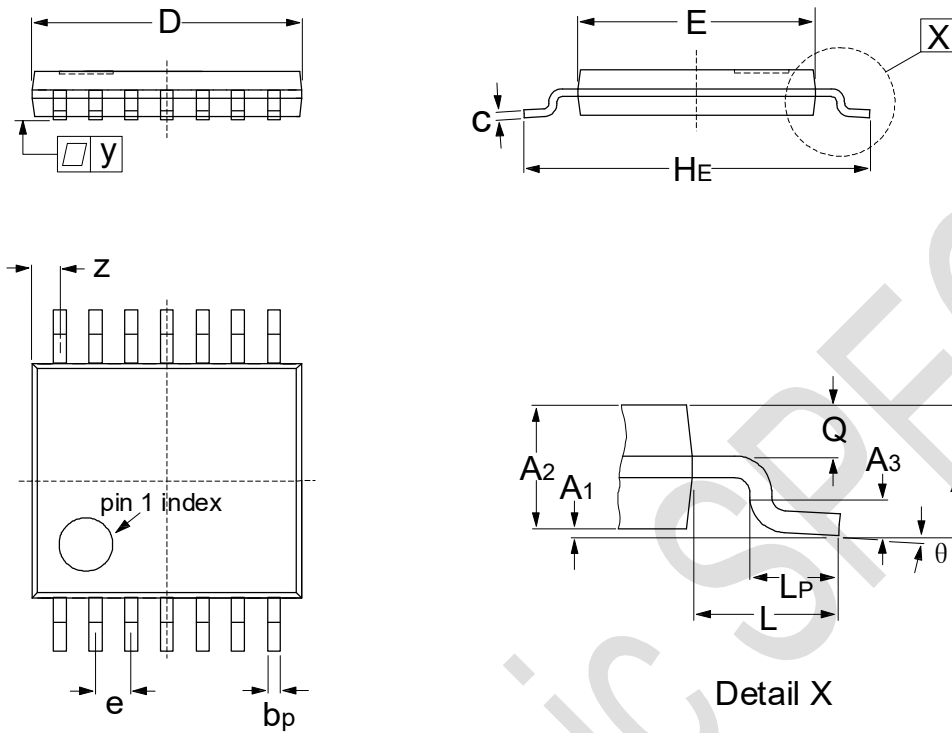
NOTE: Layout Recommendations have been shown for dual op-amp only, follow similar precautions for Single and four.

11 PACKAGE OUTLINE DIMENSIONS
SOT23-5

RECOMMENDED LAND PATTERN (Unit: mm)


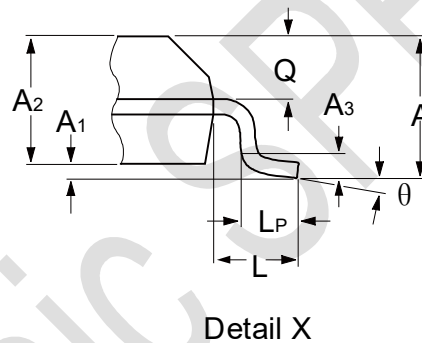
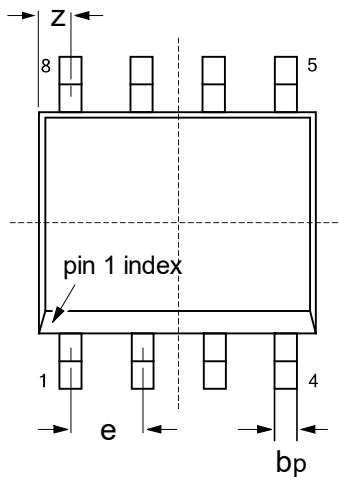
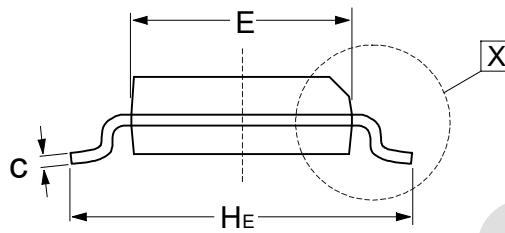
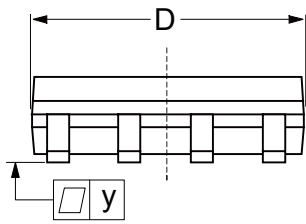
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.250		0.049
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.360	0.500	0.014	0.020
c	0.100	0.200	0.004	0.008
D	2.826	3.026	0.111	0.119
E	1.526	1.726	0.060	0.068
E1	2.600	3.000	0.102	0.118
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.350	0.600	0.014	0.024
θ	0°	8°	0°	8°

MSOP-8

RECOMMENDED LAND PATTERN (Unit: mm)


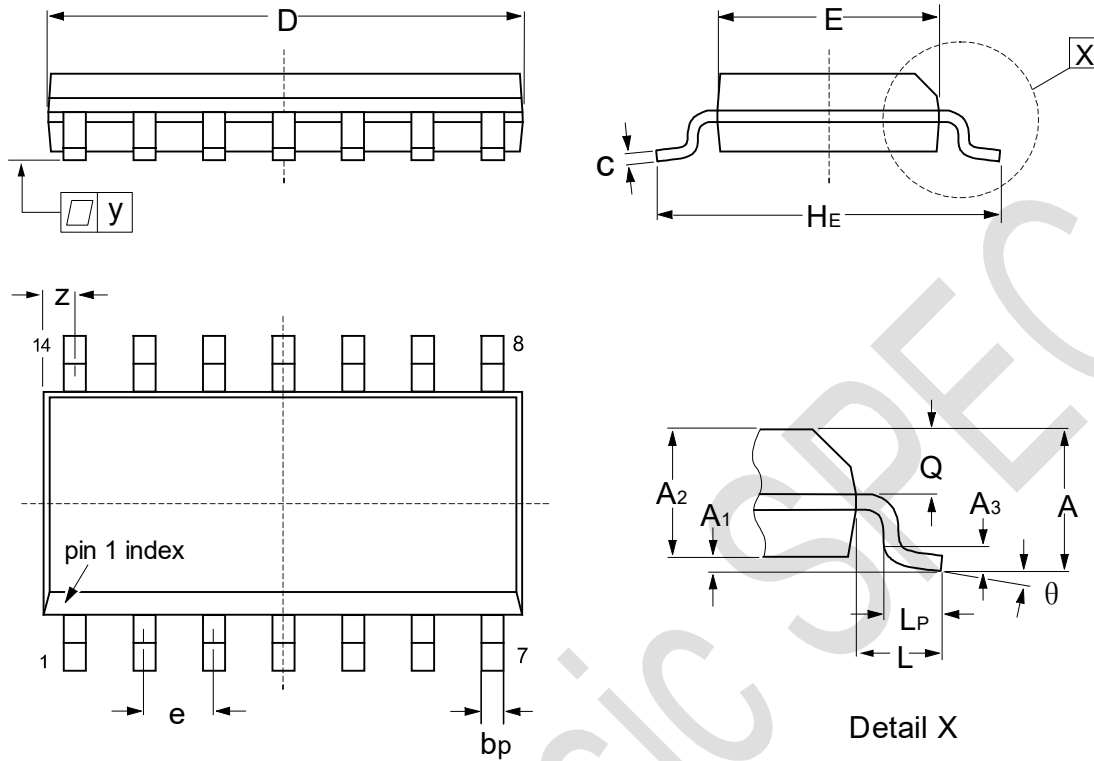
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

TSSOP-14


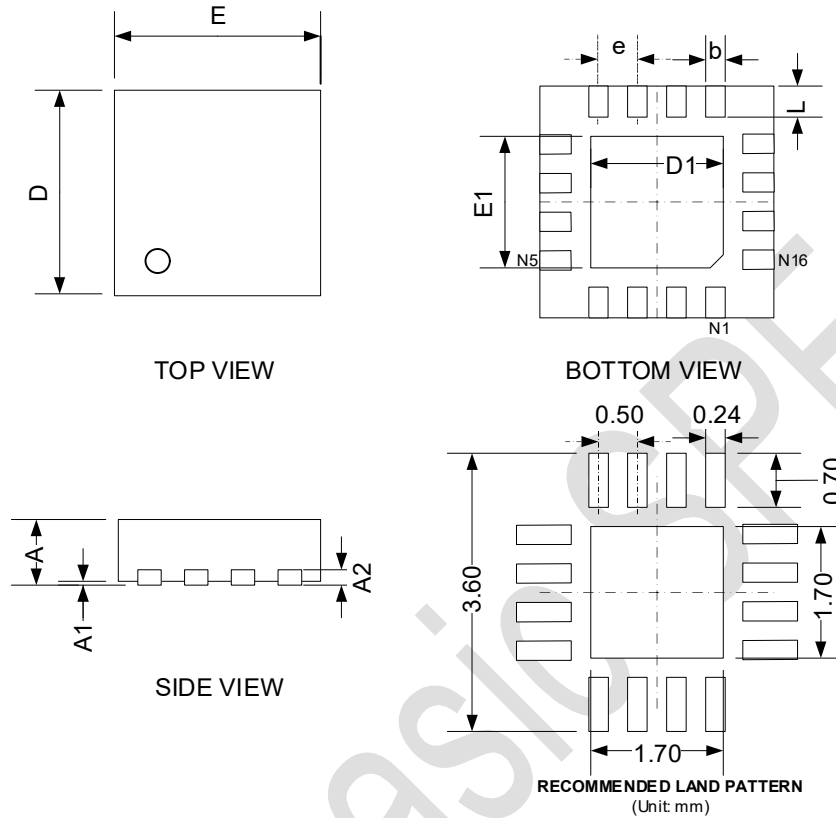
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.100		0.043
A ₁	0.050	0.150	0.002	0.006
A ₂	0.800	0.950	0.031	0.037
A ₃	0.25		0.010	
b _p	0.190	0.300	0.007	0.012
c	0.100	0.200	0.004	0.008
D ^(A)	4.900	5.100	0.193	0.201
E ^(B)	4.300	4.500	0.169	0.177
H _E	6.200	6.600	0.244	0.260
e	0.650		0.026	
L	1		0.039	
L _P	0.500	0.750	0.020	0.030
Q	0.300	0.400	0.012	0.016
Z ^(A)	0.380	0.720	0.015	0.028
y	0.1		0.004	
θ	0°	8°	0°	8°

SOIC-8(SOP8)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.750		0.069
A ₁	0.100	0.250	0.004	0.010
A ₂	1.250	1.450	0.049	0.057
A ₃	0.25		0.010	
b _p	0.360	0.490	0.014	0.019
c	0.190	0.250	0.007	0.010
D ^(A)	4.800	5.000	0.190	0.200
E ^(B)	3.800	4.000	0.150	0.160
H _E	5.800	6.200	0.228	0.244
e	1.270		0.050	
L	1.05		0.041	
L _P	0.400	1.000	0.016	0.039
Q	0.600	0.700	0.024	0.028
Z ^(A)	0.300	0.700	0.012	0.028
y	0.1		0.004	
θ	0°	8°	0°	8°

SOIC-14(SOP14)


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.750		0.069
A ₁	0.100	0.250	0.004	0.010
A ₂	1.250	1.450	0.049	0.057
A ₃	0.25		0.010	
b _p	0.360	0.490	0.014	0.019
c	0.190	0.250	0.007	0.010
D ^(A)	8.550	8.750	0.340	0.350
E ^(A)	3.800	4.000	0.150	0.160
H _E	5.800	6.200	0.228	0.244
e	1.270		0.050	
L	1.05		0.041	
L _P	0.400	1.000	0.016	0.039
Q	0.600	0.700	0.024	0.028
Z ^(A)	0.300	0.700	0.012	0.028
y	0.1		0.004	
θ	0°	8°	0°	8°

QFN-3x3-16L


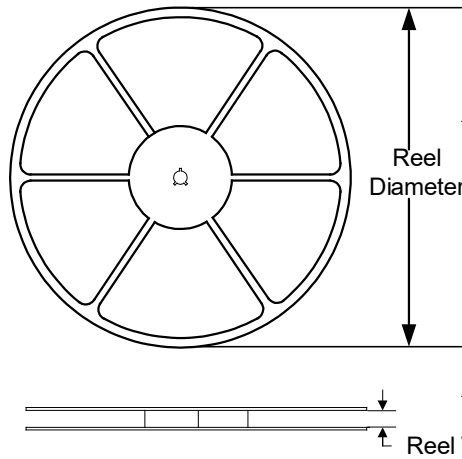
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A2	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D1	1.650	1.750	0.065	0.069
E	2.950	3.050	0.116	0.120
E1	1.650	1.750	0.065	0.069
e	0.500 TYP		0.020 TYP	
L	0.350	0.450	0.014	0.018

NOTE:

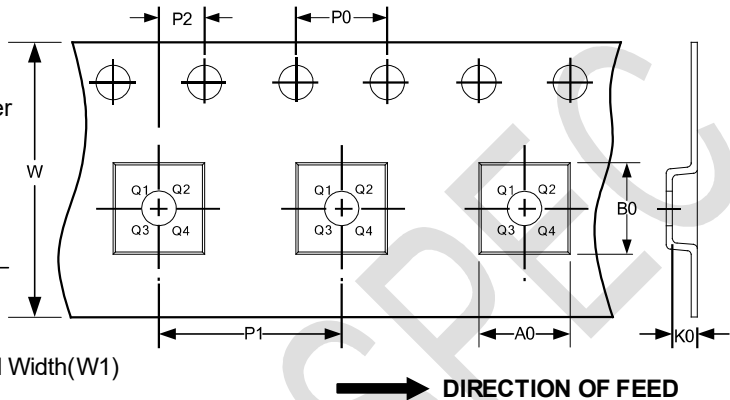
- A. Plastic or metal protrusions of 0.15mm maximum per side are not included.
- B. Plastic interlead protrusions of 0.25mm maximum per side are not included.
- C. All linear dimension is in millimeters.
- D. This drawing is subject to change without notice.
- E. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- F. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

12 TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOIC-8(SOP8)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
MSOP-8	13"	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
SOIC-14(SOP14)	13"	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
TSSOP-14	13"	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
QFN3x3-16L	13"	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

NOTE:

1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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[UPC4742GR-9LG-E1-A](#) [UPC4742G2-E1-A](#) [UPC832G2-E2-A](#) [UPC842G2-E1-A](#) [UPC802G2-E1-A](#) [UPC4741G2-E2-A](#) [UPC4572G2-E2-A](#)
[UPC844GR-9LG-E2-A](#) [UPC259G2-E1-A](#) [UPC4741G2-E1-A](#) [UPC4558G2-E1-A](#) [UPC4574GR-9LG-E1-A](#) [UPC1251GR-9LG-E1-A](#)
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