# 32V, 8MHz Rail-to-Rail Output CMOS Operational Amplifier

## 1 FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Qualified with the Grade 1**
- **HIGH GAIN BANDWIDTH:8MHz**
- **INPUT OFFSET VOLTAGE: ±0.8mV (Typical)**
- **QUIESCENT CURRENT:2.75mA/Amp**
- **Rail to Rail Output**
- **Supply Range: +5V to +32V**
- **SPECIFIED UP TO +125°C**
- **Micro SIZE PACKAGES: SOIC-8(SOP8)**

## 2 APPLICATIONS

- **SENSORS**
- **PHOTODIODE AMPLIFICATION**
- **ACTIVE FILTERS**
- **TEST EQUIPMENT**
- **DRIVING A/D CONVERTERS**

## 3 DESCRIPTIONS

The RS845X-Q1 families of products offer high voltage (32V) operation and rail-to-rail output, as well as excellent speed/power consumption ratio, providing an excellent bandwidth (8MHz) and slew rate of 5V/us. The op-amps are unity gain stable and feature an ultra-low input bias current.

The input can operate normally within the negative power rail to 2V below of the positive power rail. The RS845X-Q1 families of operational amplifiers are specified at the full temperature range of −40°C to +125°C under single power supplies of 5V to 32V or dual power supplies of ±2.5V to ±16V.

**Device Information (1)**

| PART NUMBER | PACKAGE | BODY SIZE(NOM) |
|---|---|---|
| RS8452-Q1 | SOIC-8(SOP8) | 4.90mm x 3.90mm |
| | MSOP-8 | 3.00mm x 3.00mm |
| RS8454-Q1 | SOIC-14(SOP14) | 8.65mm x 3.90mm |
| | TSSOP-14 | 5.00mm x 4.40mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

# Table of Contents

# 4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

| VERSION | Change Date | Change Item |
|---|---|---|
| A.1 | 2023/02/15 | Initial version completed |

# 5 PACKAGE/ORDERING INFORMATION (1)

| Orderable Device | Package Type | Pin | Channel | Lead finish/Ball material (2) | MSL Peak Temp (3) | Op Temp(°C) | Device Marking (4) | Package Qty |
|---|---|---|---|---|---|---|---|---|
| RS8452XK-Q1 | SOIC-8 (SOP8) | 8 | 2 | NIPDAUAG | MSL1-260°-Unlimited | -40°C ~125°C | RS8452 | Tape and Reel,4000 |
| RS8452XM-Q1 | MSOP-8 | 8 | 2 | NIPDAUAG | MSL1-260°-Unlimited | -40°C ~125°C | RS8452 | Tape and Reel,4000 |
| RS8454XP-Q1 | SOIC-14 (SOP14) | 14 | 4 | NIPDAUAG | MSL1-260°-Unlimited | -40°C ~125°C | RS8454 | Tape and Reel,4000 |
| RS8454XQ-Q1 | TSSOP-14 | 14 | 4 | NIPDAUAG | MSL1-260°-Unlimited | -40°C ~125°C | RS8454 | Tape and Reel,4000 |

NOTE:

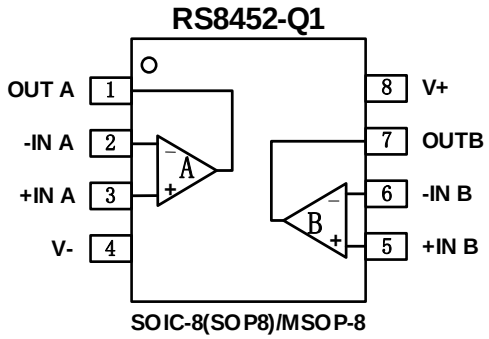
(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) Lead finish/Ball material. Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(3) MSL Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

# 6 Pin Configuration and Functions (Top View)

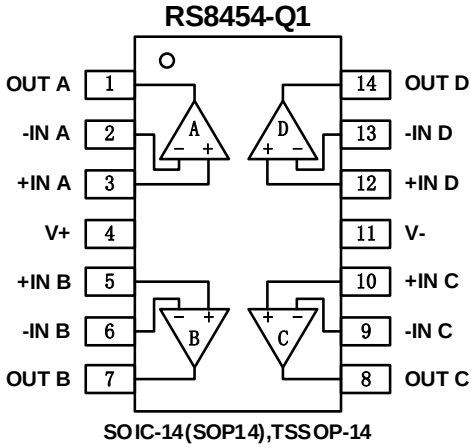



## Pin Description

| NAME | PIN | I/O (1) | DESCRIPTION |
|---|---|---|---|
| | SOIC-8(SOP8)/MSOP-8 | | |
| -INA | 2 | I | Inverting input, channel A |
| +INA | 3 | I | Noninverting input, channel A |
| -INB | 6 | I | Inverting input, channel B |
| +INB | 5 | I | Noninverting input, channel B |
| OUTA | 1 | O | Output, channel A |
| OUTB | 7 | O | Output, channel B |
| V- | 4 | - | Negative (lowest) power supply or ground (for single supply operation) |
| V+ | 8 | - | Positive (highest) power supply |

(1) I = Input, O = Output.

## Pin Configuration and Functions (Top View)




## Pin Description

| NAME | PIN | I/O (1) | DESCRIPTION |
|---|---|---|---|
| | SOIC-14(SOP14)/TSSOP-14 | | |
| -INA | 2 | I | Inverting input, channel A |
| +INA | 3 | I | Noninverting input, channel A |
| -INB | 6 | I | Inverting input, channel B |
| +INB | 5 | I | Noninverting input, channel B |
| -INC | 9 | I | Inverting input, channel C |
| +INC | 10 | I | Noninverting input, channel C |
| -IND | 13 | I | Inverting input, channel D |
| +IND | 12 | I | Noninverting input, channel D |
| OUTA | 1 | O | Output, channel A |
| OUTB | 7 | O | Output, channel B |
| OUTC | 8 | O | Output, channel C |
| OUTD | 14 | O | Output, channel D |
| V- | 11 | - | Negative (lowest) power supply or ground (for single supply operation) |
| V+ | 4 | - | Positive (highest) power supply |

(1) I = Input, O = Output.

# 7 SPECIFICATIONS

## 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Voltage | Supply, Vs=(V+) - (V-) | | -0.7 | 36 | V |
| | Signal input pin (2) | | (V-)-0.2 | (V+) +0.2 | |
| | Signal output pin (3) | | (V-)-0.2 | (V+) +0.2 | |
| Current | Signal input pin (2) | | -10 | 10 | mA |
| | Signal output pin (3) | | -100 | 100 | mA |
| | Output short-circuits (4) | | Continuous | | |
| $\theta_{JA}$ | Package thermal impedance (5) | SOIC-8(SOP8) | | 110.88 | °C/W |
| | | MSOP-8 | | 165.7 | |
| | | SOIC-14(SOP14) | | 104.5 | |
| | | TSSOP14 | | 89.21 | |
| Temperature | Operating range, $T_A$ | | -40 | 125 | °C |
| | Junction, $T_J$ (6) | | -40 | 150 | |
| | Storage, $T_{stg}$ | | -55 | 150 | |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.2V beyond the supply rails should be current-limited to 10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.2V beyond the supply rails should be current-limited to ±100mA or less.
(4) Short-circuit to ground, one amplifier per package.
(5) The package thermal impedance is calculated in accordance with JESD-51.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

## 7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-Body Model (HBM), per AEC Q100-002 (1) | ±2000 | V |
| | | Charged-Device Model (CDM), per AEC Q100-011 | ±500 | |
| | | Latch-Up (LU), per AEC Q100-004 | ±100 | mA |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

**ESD SENSITIVITY CAUTION**

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage，Vs= (V+) - (V-) | Single-supply | 5 | | 32 | V |
| | Dual-supply | ±2.5 | | ±16 | |
| Operating range, $T_A$ | | -40 | | 125 | °C |

## 7.4 ELECTRICAL CHARACTERISTICS

(At $T_A$ = +25°C, $V_S$=5V to 32V, $R_L$ = 10kΩ connected to $V_S$/2, and $V_{OUT}$ = $V_S$/2, Full [9] = -40°C to +125°C, unless otherwise noted.) [1]

| PARAMETER | | CONDITIONS | $T_J$ | RS845X-Q1 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN[2] | TYP[3] | MAX[2] | |
| **POWER SUPPLY** | | | | | | | |
| $V_S$ | Operating Voltage Range | | 25°C | 5 | | 32 | V |
| $I_Q$ | Quiescent Current/Amplifier | $V_S$=±2.5V, $I_O$=0mA | 25°C | | 2.75 | 4.75 | mA |
| | | | Full | | | 5.25 | |
| | | $V_S$=±16V, $I_O$=0mA | 25°C | | 3.0 | 5.75 | |
| | | | Full | | | 6.25 | |
| PSRR | Power-Supply Rejection Ratio | $V_S$=5V to 32V | 25°C | 93 | 110 | | dB |
| | | | Full | 88 | | | |
| **INPUT** | | | | | | | |
| Vos | Input Offset Voltage | $V_{CM}$= $V_S$/2 | 25°C | -2.3 | ±0.8 | 2.3 | mV |
| | | | Full | -3.5 | | 3.5 | |
| Vos Tc | Input Offset Voltage Average Drift | | Full | | ±5 | | uV/°C |
| IB | Input Bias Current [4] [5] | $V_{CM}$= $V_S$/2 | 25°C | | ±10 | | pA |
| $I_{OS}$ | Input Offset Current [4] | $V_{CM}$= $V_S$/2 | 25°C | | ±10 | | pA |
| $V_{CM}$ | Common-Mode Voltage Range | $V_S$= ±16V | Full | (V-)+0.5 | | (V+)-2 | V |
| CMRR | Common-Mode Rejection Ratio | $V_S$= ±16V<br>$V_{CM}$=(V-)+0.5 to (V+)-2V | 25°C | 87 | 110 | | dB |
| | | | Full | 84 | | | |
| **OUTPUT** | | | | | | | |
| $A_{OL}$ | Open-Loop Voltage Gain | $R_L$=10KΩ, $V_O$=(V-)+0.6V to (V+)-0.6V | 25°C | 84 | 100 | | dB |
| | | | Full | 70 | | | |
| $V_{OH}$ | Output Swing | $V_S$=±16V, $R_L$=10KΩ | Full | 15.7 | | | V |
| $V_{OL}$ | | | | | | -15.7 | V |
| $I_{SC}$ | Short-Circuit Current [6] [7] | | 25°C | ±55 | ±150 | | mA |
| | | | Full | ±30 | | | |
| $C_{LOAD}$ | Capacitive Load Drive | | 25°C | | 70 | | pF |
| **FREQUENCY RESPONSE** | | | | | | | |
| SR | Slew Rate [8] | G=+1, $C_L$=70pF | 25°C | | 5 | | V/us |
| GBW | Gain-Bandwidth Product | | 25°C | | 8 | | MHz |
| $t_S$ | Settling Time,0.01% | $V_S$=±2.5V, G=+1, $C_L$=70pF, Step=2V | 25°C | | 1.0 | | us |
| $t_{OR}$ | Overload Recovery Time | $V_{IN}$·Gain≥$V_S$, G=11 | 25°C | | 1.0 | | us |
| $t_{ON}$ | Turn On Time | | 25°C | | 10 | | us |
| **NOISE** | | | | | | | |
| En | Input Voltage Noise | f = 0.1Hz to 10Hz, $V_S$=±2.5V | 25°C | | 7 | | uVpp |
| en | Input Voltage Noise Density [4] | f = 1KHz | 25°C | | 35 | | nV/$\sqrt{\text{Hz}}$ |

NOTE:
(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Positive current corresponds to current flowing into the device.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and $T_A$. The maximum allowable power dissipation at any ambient temperature is PD = ($T_{J(MAX)}$ - $T_A$) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.
(7) Short circuit test is a momentary test.
(8) Number specified is the slower of positive and negative slew rates.
(9) Specified by characterization only.

## 7.5 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At $T_A$ = +25°C, $V_S$=±16V, $R_L$ = 10kΩ connected to $V_S$/2, $V_{OUT}$ = $V_S$/2, unless otherwise noted.

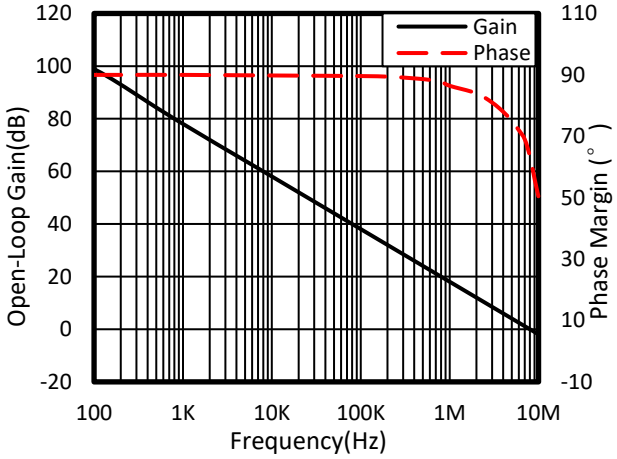



**Figure 1. OPEN-LOOP GAIN AND PHASE vs FREQUENCY**

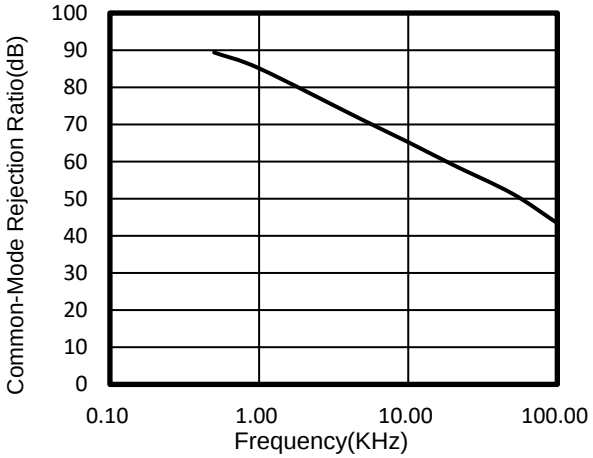



**Figure 2. Common-Mode Rejection Ratio vs FREQUENCY**

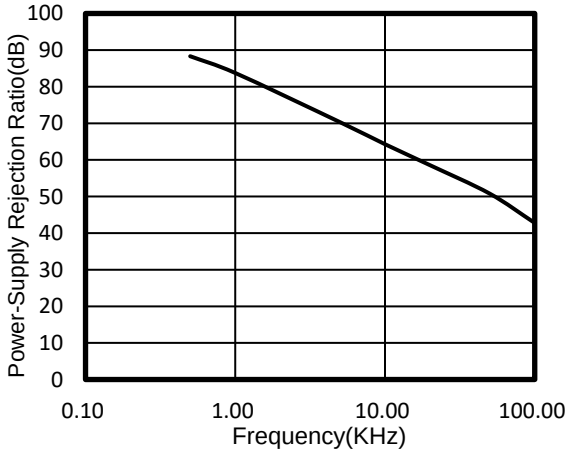



**Figure 3. Power-Supply Rejection Ratio+ vs FREQUENCY**

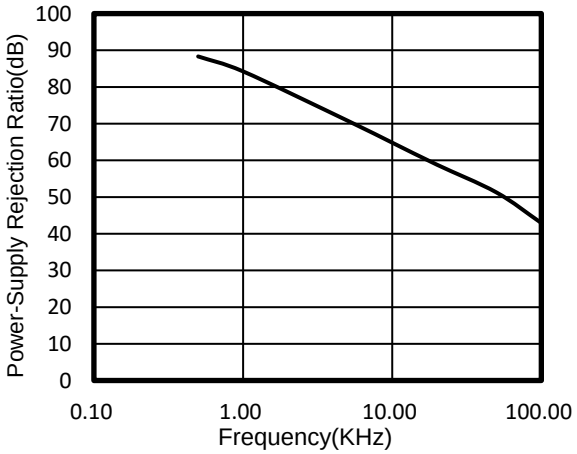



**Figure 4. Power-Supply Rejection Ratio- vs FREQUENCY**

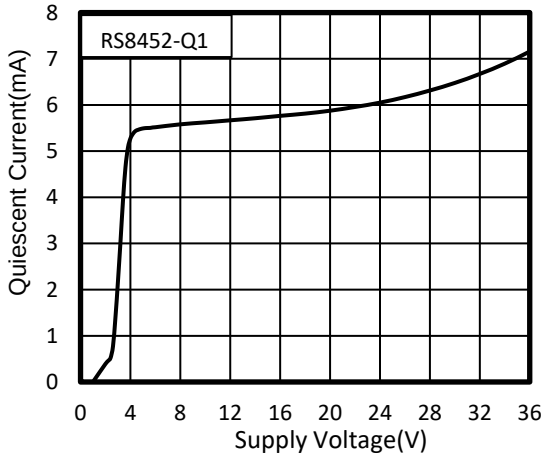



**Figure 5. SUPPLY VOLTAGE vs QUIESCENT CURRENT**

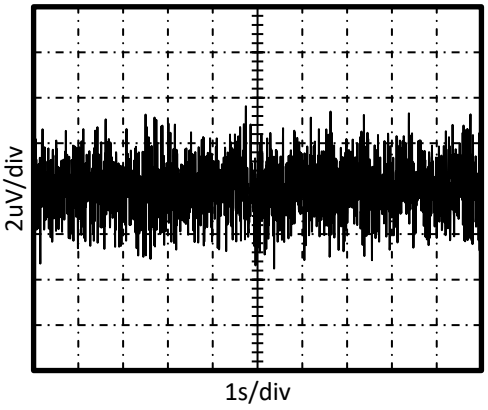



**Figure 6. 0.1Hz TO 10Hz NOISE at Vs=5V**

## TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At $T_A$ = +25°C, $V_S$=±16V, $R_L$ = 10kΩ connected to $V_S$/2, $V_{OUT}$ = $V_S$/2, unless otherwise noted.

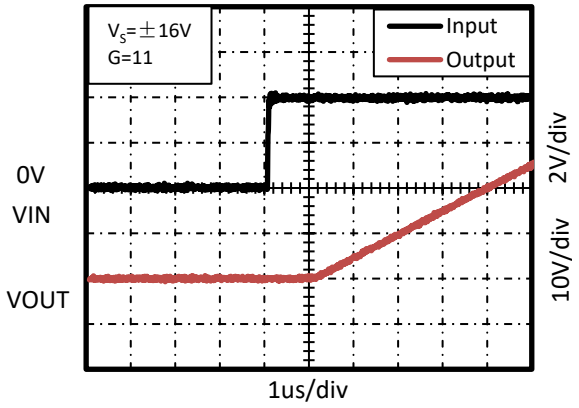



**Figure 7. POSITIVE OVERVOLTAGE RECOVERY**

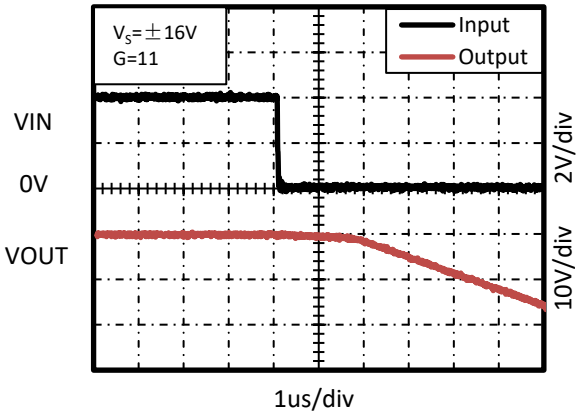



**Figure 8. NEGATIVE OVERVOLTAGE RECOVERY**

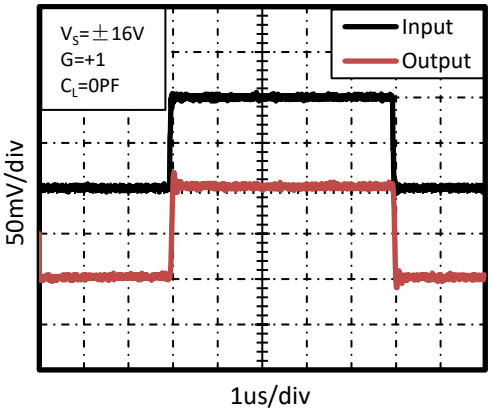



**Figure 9. SMALL SIGNAL STEP RESPONSE**

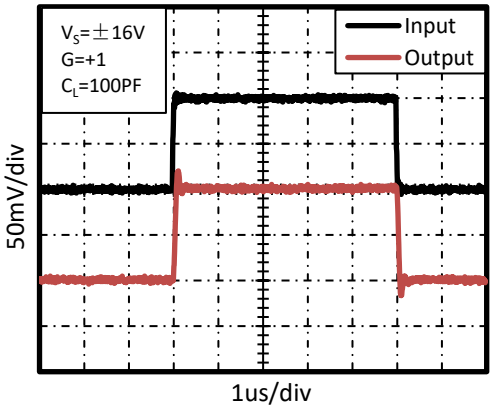



**Figure 10. SMALL SIGNAL STEP RESPONSE**

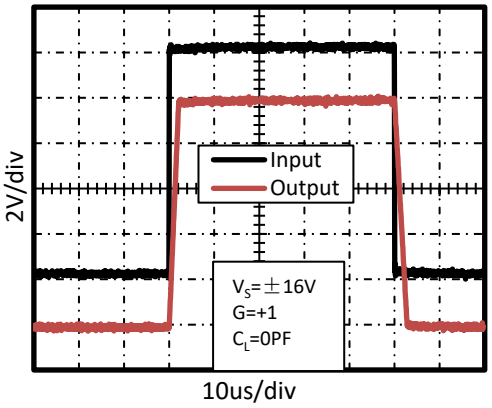



**Figure 11. LARGE SIGNAL STEP RESPONSE**

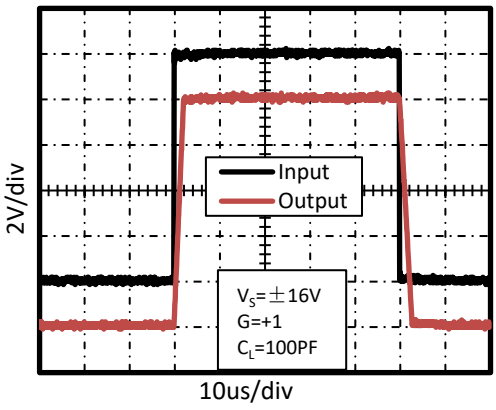



**Figure 12. LARGE SIGNAL STEP RESPONSE**

# TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

At $T_A$ = +25°C, $V_S$=±16V, $R_L$ = 10kΩ connected to $V_S$/2, $V_{OUT}$ = $V_S$/2, unless otherwise noted.

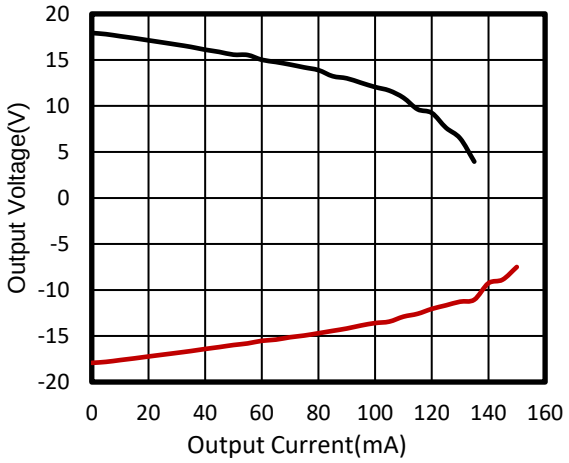



**Figure 13. Output Voltage Swing vs Output Current**

# 8 Detailed Description

## 8.1 Overview

The RS845X-Q1 operational amplifier provides high overall performance, making these devices designed for many general-purpose applications. The excellent offset drift of only 5 μV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and $A_{OL}$.

## 8.2 Operating Characteristics

The RS845X-Q1 amplifier is specified for operation from 5 V to 32 V (±2.5 V to ±16 V). Many of the specifications apply from –40°C to +125°C.

## 8.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits for protection from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 14 shows the ESD circuits contained in the RS845X-Q1. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

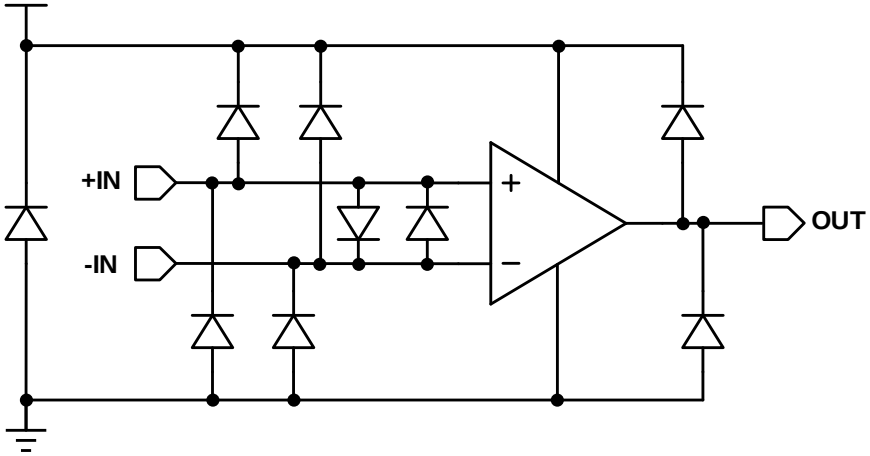



**Figure 14. ESD block diagram**

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the RS845X-Q1 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit, as shown in Figure 11, the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances can arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 11 shows a specific example where the input voltage ($V_{IN}$) exceeds the positive supply voltage (V+) by

500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, then one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher $V_{IN}$. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, $V_{IN}$ can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

The input pins of the RS845X-Q1 are protected from excessive differential voltage with back-to-back diodes; see Figure 11. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, then limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can limit the input signal current. This input series resistor degrades the low-noise performance of the RS845X-Q1. Figure 11 shows an example configuration that implements a current-limiting feedback resistor.

# 9 Application and Implementation

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 APPLICATION NOTE

The RS845X-Q1 operational amplifier provides high overall performance in a large number of general-purpose applications. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1μF capacitors are adequate. Follow the additional recommendations in the Layout Guidelines section to achieve the maximum performance from this device. Many applications introduce capacitive loading to the output of the amplifier (which potentially causes instability). To stabilize the amplifier, add an isolation resistor between the amplifier output and the capacitive load.

## 9.2 Typical Applications

This circuit can drive capacitive loads (such as cable shields, reference buffers, MOSFET gates, and diodes). The circuit uses an isolation resistor ($R_{ISO}$) to stabilize the output of an operational amplifier. $R_{ISO}$ modifies the open-loop gain of the system to ensure that the circuit has sufficient phase margin.

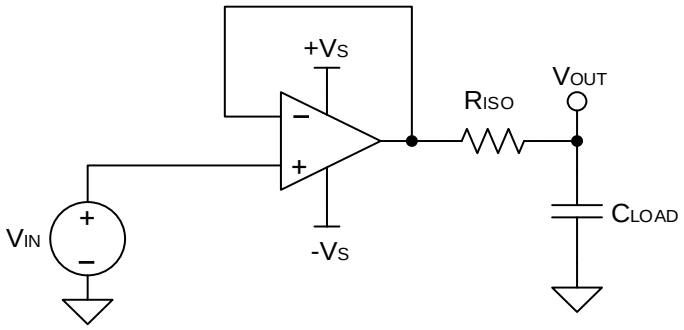



**Figure 15. Unity-Gain Buffer with $R_{ISO}$ Stability Compensation**

## 9.3 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01μF, 0.1μF, and 1μF
- Phase margin: 45° and 60°

## 9.4 Detailed Design Procedure

Figure 15 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 15. Figure 15 does not show the open-loop output resistance of the operational amplifier ($R_O$).

$$T(s) = \frac{1+C_{LOAD}\times R_{ISO}\times S}{1+(R_0+R_{ISO})\times C_{LOAD}\times S} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole ($f_p$) is determined by ($R_O$ +$R_{ISO}$) and $C_{LOAD}$. The $R_{ISO}$ and $C_{LOAD}$ components determine the frequency of the zero ($f_z$). A stable system is obtained by selecting $R_{ISO}$ so that the rate of closure (ROC) between the open-loop gain ($A_{OL}$) and 1/β is 20 dB per decade.

# 10 Layout

## 10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  —Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 17, keeping $R_F$ and $R_G$ close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 10.2 Layout Example

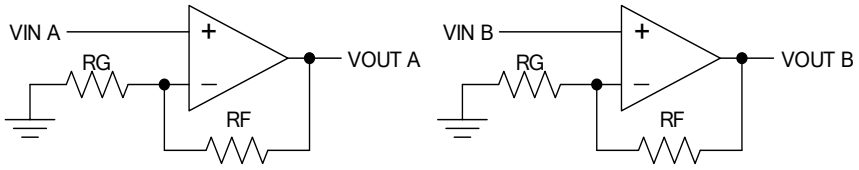



**Figure 16. Schematic Representation**

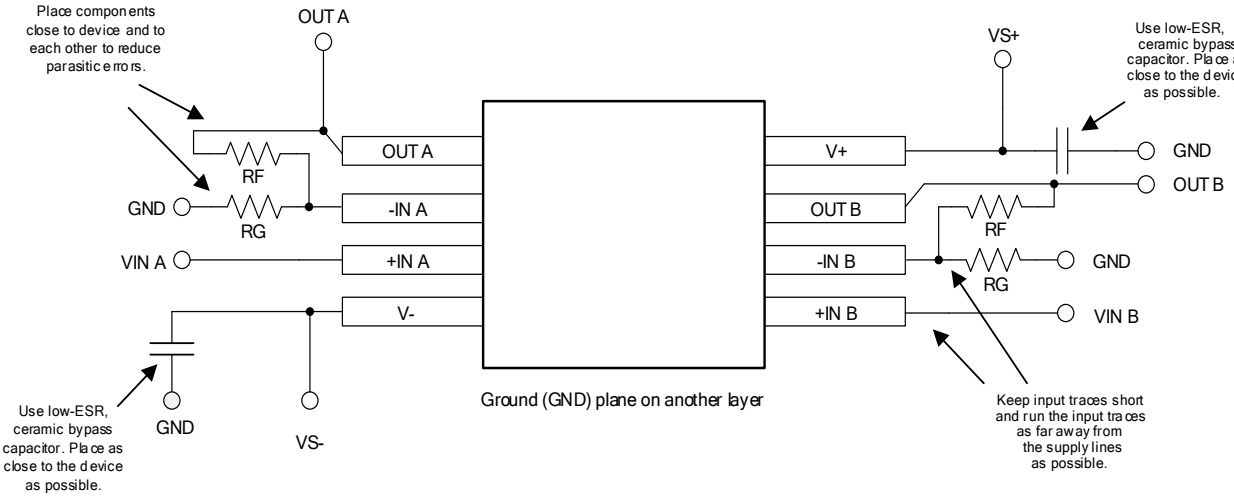
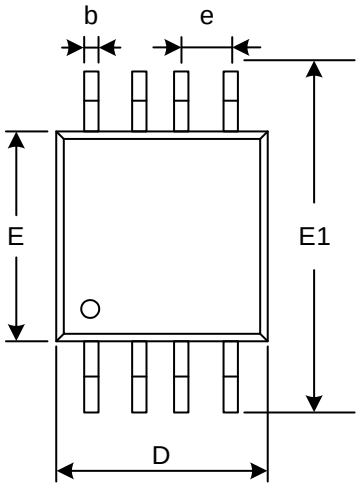


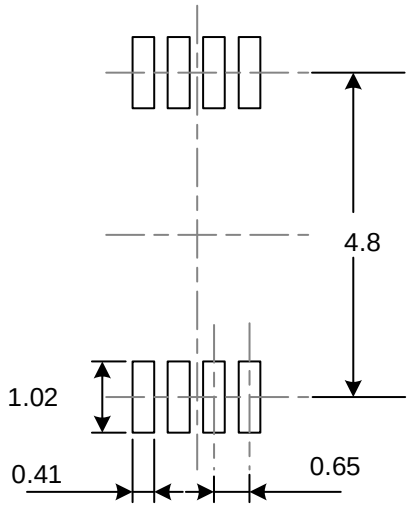

**Figure 17. Layout Example**

NOTE: Layout Recommendations have been shown for dual op-amp only, follow similar precautions for Single and four.

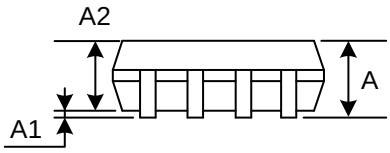
# 11 PACKAGE OUTLINE DIMENSIONS

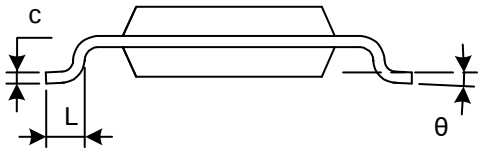
## MSOP-8



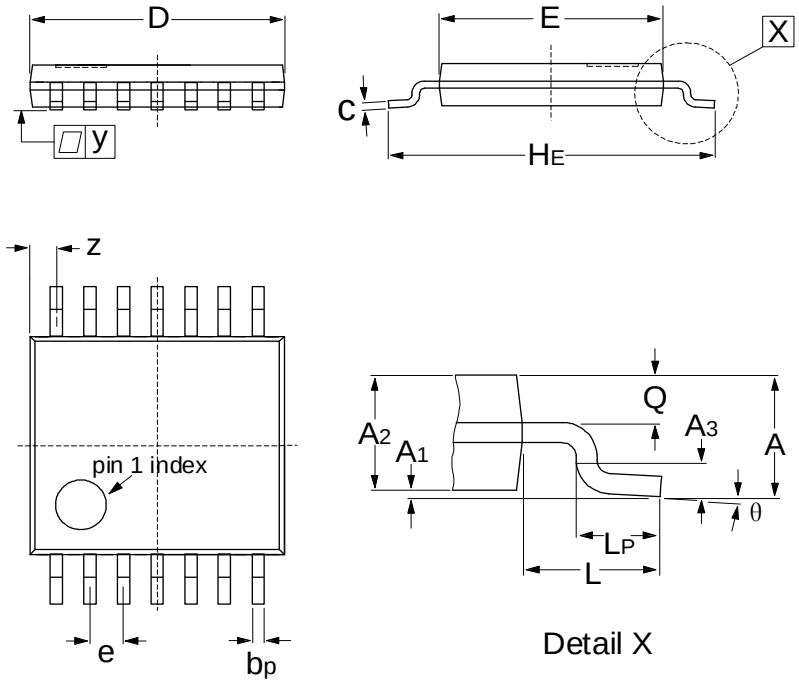

**RECOMMENDED LAND PATTERN** (Unit: mm)

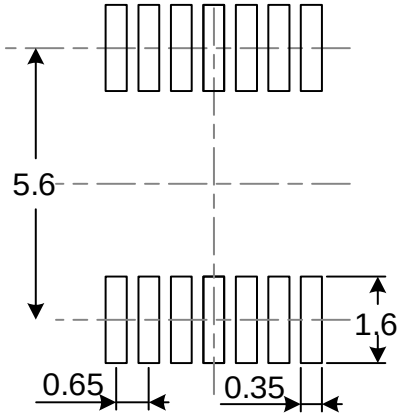



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.820 | 1.100 | 0.032 | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.250 | 0.380 | 0.010 | 0.015 |
| c | 0.090 | 0.230 | 0.004 | 0.009 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| e | 0.650(BSC) | | 0.026(BSC) | |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 4.750 | 5.050 | 0.187 | 0.199 |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0° | 6° | 0° | 6° |

## TSSOP-14

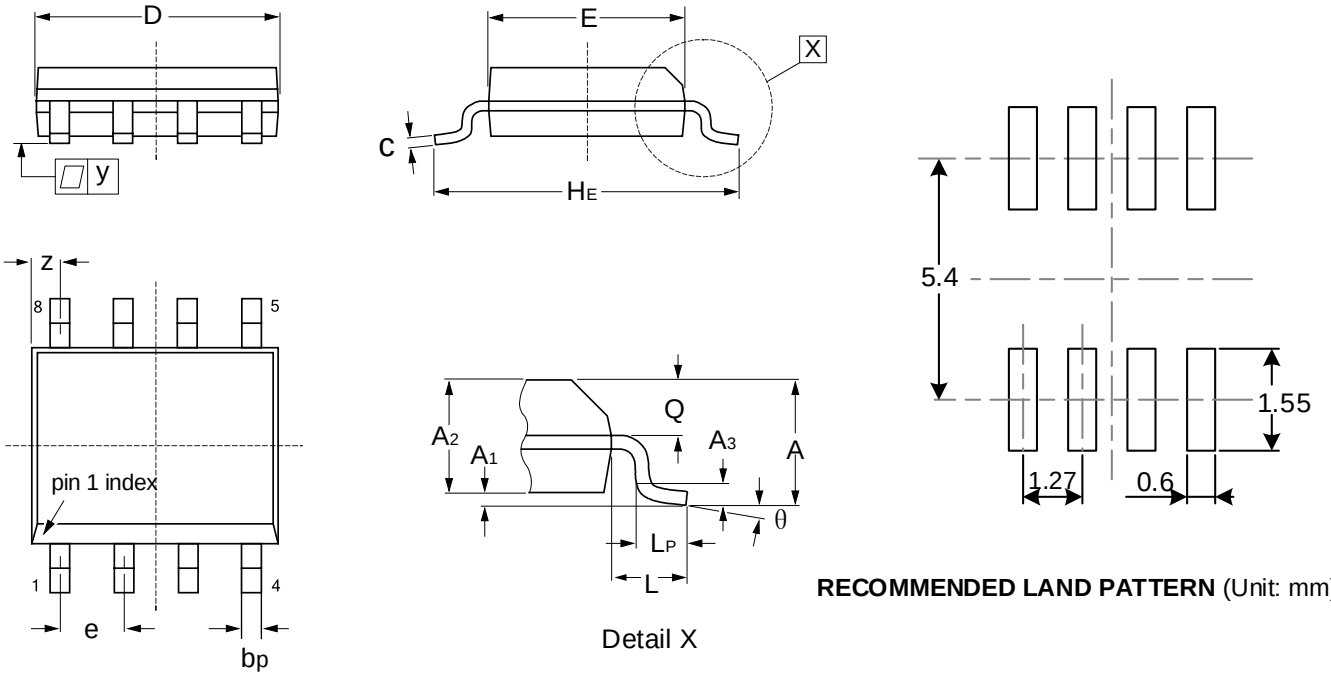



**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | | 1.100 | | 0.043 |
| $A_1$ | 0.050 | 0.150 | 0.002 | 0.006 |
| $A_2$ | 0.800 | 0.950 | 0.031 | 0.037 |
| $A_3$ | 0.25 | | 0.010 | |
| $b_p$ | 0.190 | 0.300 | 0.007 | 0.012 |
| c | 0.100 | 0.200 | 0.004 | 0.008 |
| $D^{(A)}$ | 4.900 | 5.100 | 0.193 | 0.201 |
| $E^{(B)}$ | 4.300 | 4.500 | 0.169 | 0.177 |
| $H_E$ | 6.200 | 6.600 | 0.244 | 0.260 |
| e | 0.650 | | 0.026 | |
| L | 1 | | 0.039 | |
| $L_P$ | 0.500 | 0.750 | 0.020 | 0.030 |
| Q | 0.300 | 0.400 | 0.012 | 0.016 |
| $Z^{(A)}$ | 0.380 | 0.720 | 0.015 | 0.028 |
| y | 0.1 | | 0.004 | |
| θ | 0° | 8° | 0° | 8° |

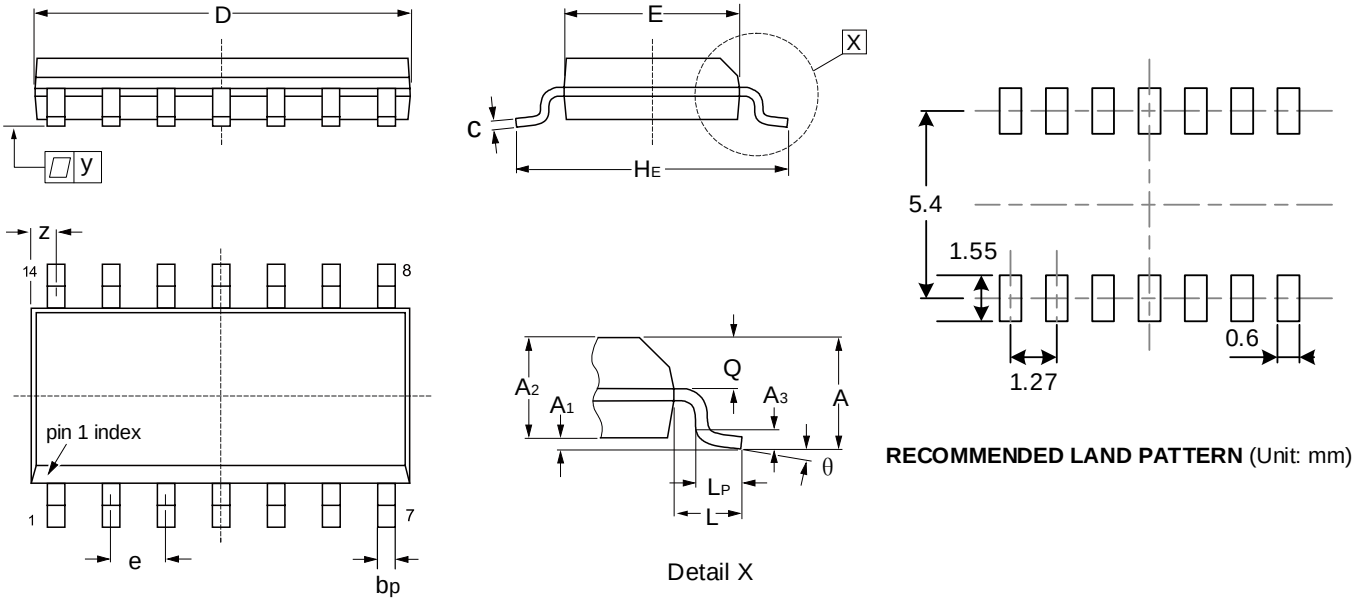
## SOIC-8(SOP8)




**RECOMMENDED LAND PATTERN** (Unit: mm)

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | | 1.750 | | 0.069 |
| $A_1$ | 0.100 | 0.250 | 0.004 | 0.010 |
| $A_2$ | 1.250 | 1.450 | 0.049 | 0.057 |
| $A_3$ | 0.25 | | 0.010 | |
| $b_p$ | 0.360 | 0.490 | 0.014 | 0.019 |
| c | 0.190 | 0.250 | 0.007 | 0.010 |
| $D^{(A)}$ | 4.800 | 5.000 | 0.190 | 0.200 |
| $E^{(B)}$ | 3.800 | 4.000 | 0.150 | 0.160 |
| $H_E$ | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 | | 0.050 | |
| L | 1.05 | | 0.041 | |
| $L_P$ | 0.400 | 1.000 | 0.016 | 0.039 |
| Q | 0.600 | 0.700 | 0.024 | 0.028 |
| $Z^{(A)}$ | 0.300 | 0.700 | 0.012 | 0.028 |
| y | 0.1 | | 0.004 | |
| θ | 0° | 8° | 0° | 8° |

## SOIC-14(SOP14)




**RECOMMENDED LAND PATTERN** (Unit: mm)

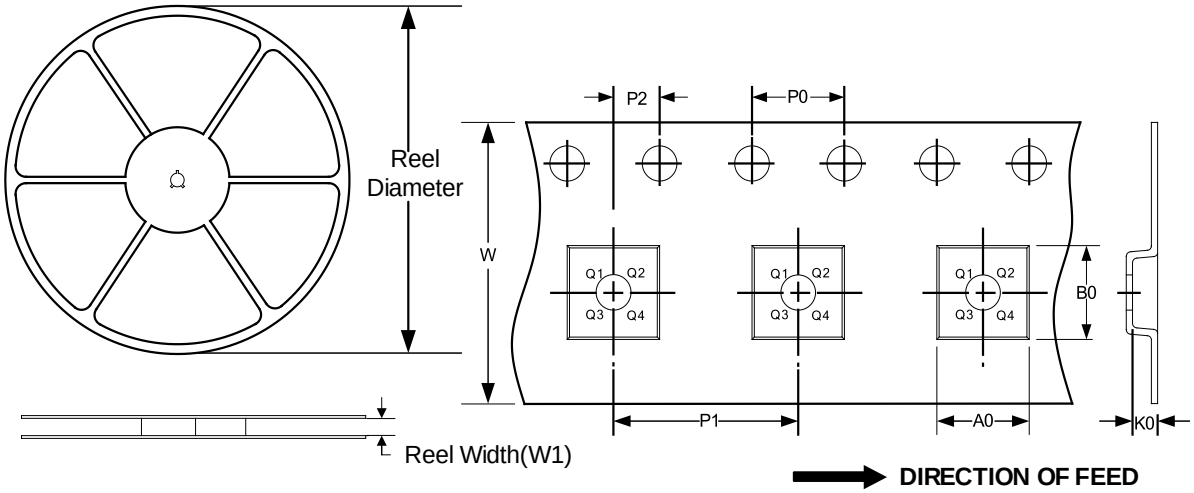
| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | | 1.750 | | 0.069 |
| $A_1$ | 0.100 | 0.250 | 0.004 | 0.010 |
| $A_2$ | 1.250 | 1.450 | 0.049 | 0.057 |
| $A_3$ | 0.25 | | 0.010 | |
| $b_p$ | 0.360 | 0.490 | 0.014 | 0.019 |
| c | 0.190 | 0.250 | 0.007 | 0.010 |
| $D^{(A)}$ | 8.550 | 8.750 | 0.340 | 0.350 |
| $E^{(A)}$ | 3.800 | 4.000 | 0.150 | 0.160 |
| $H_E$ | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270 | | 0.050 | |
| L | 1.05 | | 0.041 | |
| $L_P$ | 0.400 | 1.000 | 0.016 | 0.039 |
| Q | 0.600 | 0.700 | 0.024 | 0.028 |
| $Z^{(A)}$ | 0.300 | 0.700 | 0.012 | 0.028 |
| y | 0.1 | | 0.004 | |
| θ | 0° | 8° | 0° | 8° |

NOTE:

A. Plastic or metal protrusions of 0.15mm maximum per side are not included.
B. Plastic interlead protrusions of 0.25mm maximum per side are not included.
C. All linear dimension is in millimeters.
D. This drawing is subject to change without notice.
E. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
F. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

# 12 TAPE AND REEL INFORMATION

## REEL DIMENSIONS TAPE DIMENSION




NOTE: The picture is only for reference. Please make the object as the standard.

## KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1(mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| SOIC-8(SOP8) | 13" | 12.4 | 6.40 | 5.40 | 2.10 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |
| MSOP-8 | 13" | 12.4 | 5.20 | 3.30 | 1.50 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |
| SOIC-14(SOP14) | 13" | 16.4 | 6.60 | 9.30 | 2.10 | 4.0 | 8.0 | 2.0 | 16.0 | Q1 |
| TSSOP-14 | 13" | 12.4 | 6.95 | 5.60 | 1.20 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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