Femtoampere Input Bias Current Electrometer Amplifier

1 FEATURES

- **Low Input Bias Current:**
  - **±200fA (Max) at T_A =25°C**
- **Low Offset Voltage: 54µV typical @5V supply**
- **Offset voltage drift: ±5µV/°C typical**
- **Integrated guard buffer with 400µV maximum offset**
- **Low voltage noise density: 14nV/$\sqrt{\text{Hz}}$ at 10 kHz**
- **Wide bandwidth: 3.3MHz unity-gain crossover**
- **Supply voltage: 5V to 25V (±2.5V to ±12.5V)**
- **Operating temperature: -40°C to +125°C**
- **Micro SIZE PACKAGES: SOIC-8(SOP8)**

2 APPLICATIONS

- **Laboratory and analytical instrumentation: spectrophotometers, chromatographs, mass spectrometers, and potentiostatic and amperostatic coulometry**
- **Instrumentation: picoammeters and coulombmeters**
- **Transimpedance Amplifier (TIA) for photodiodes, ion chambers, and working electrode measurements**
- **High Impedance Buffering for Chemical Sensors and Capacitive Sensors**

3 DESCRIPTIONS

The RS8491 is a femtoampere (10^{-15}A) level input bias current operational amplifier suitable for use as an electrometer that also includes an integrated guard buffer. It has an operating voltage range of 5V to 25V, enabling it to operate in conventional 5V and 25V single supply systems as well as ±2.5V and ±12.5V dual supply systems.

The integrated guard buffer isolates the input pins from leakage in the printed circuit board (PCB), minimizes board component count, and enables easy system design. The RS8491 is available in an industry-standard surface-mount 8-lead SOIC package with a unique pinout optimized to prevent signals from coupling between the sensitive input pins, the power supplies, and the output pin while enabling easy routing of the guard ring traces.

The RS8491 also offers low offset voltage, low offset drift, and low voltage and current noise needed for the types of applications that require such low leakages. To maximize the dynamic range of the system, the RS8491 has a rail-to-rail output stage.

The RS8491 is available in Green SOIC-8(SOP8) packages. It operates over an ambient temperature range of -40°C to +125°C.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS8491	SOIC-8(SOP8)	4.90mm x 3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

Version	Change Date	Change Item
A.1	2023/11/29	Initial version completed

5 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS8491XK	SOIC-8(SOP8)	8	1	-40°C ~125°C	RS8491	MSL1	Tape and Reel,4000

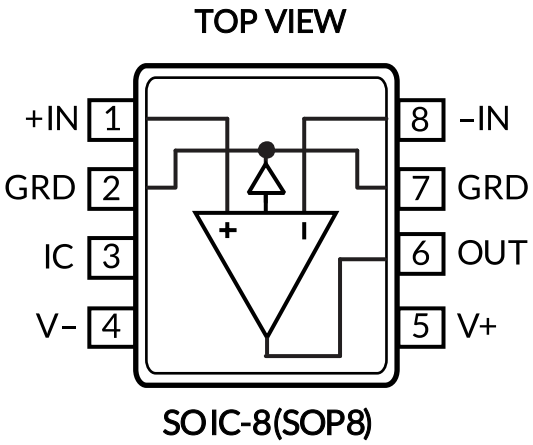
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

6 Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN	I/O (1)	DESCRIPTION
	SOIC-8(SOP8)		
+IN	1	I	Noninverting input
GRD	2	-	Guard
IC	3	I	Internal Connection. This pin must be connected to V− or left unconnected
V-	4	P	Negative supply voltage
V+	5	P	Positive supply voltage
OUT	6	O	Output
GRD	7		Guard
-IN	8	I	Inverting input

(1) I = Input, O = Output, P=Power.

7 SPECIFICATIONS

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
Voltage	Supply, V_S= (V+) - (V-)		-0.7	28	V
	Signal input pin (2)		(V-)-0.5	(V+) +0.5	
	Signal output pin (3)		(V-)-0.5	(V+) +0.5	
Current	Signal input pin (2)		-10	10	mA
	Signal output pin (3)		-10	10	mA
	Output short-circuits (4)		Continuous		
θ_{JA}	Package thermal impedance (5)	SOIC-8(SOP8)		110	°C/W
Temperature	Operating range, T_A		-40	125	°C
	Junction, T_J (6)		-40	150	
	Storage, T_{stg}		-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ±10mA or less.
(4) Short-circuit to ground, one amplifier per package.
(5) The package thermal impedance is calculated in accordance with JESD-51.
(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

7.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1500	
		Machine Model (MM), JEDEC EIA/JESD22-A114	±200	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S= (V+) - (V-)	Single-supply	5		25	V
	Dual-supply	±2.5		±12.5	

7.4 ELECTRICAL CHARACTERISTICS

(At T_A=+25°C, V_S=5V, V_{CM}=V_{OUT}=V_S/2, and R_L=10kΩ connected to V_S/2, Full = -40°C to +125°C, unless otherwise noted.)(1)

PARAMETER	SYMBOL	CONDITION	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
INPUT BIAS CURRENT							
Input Bias Current (4) (5)	I_B		25°C		±50	±200	fA
Input Offset Current (4)	I_{OS}		25°C		±50	±200	fA
OFFSET VOLTAGE							
Input Offset Voltage	V_{OS}	V_{CM}=V_S/2	25°C		±54	±400	μV
		V_{CM}=1.5V to 3V	−40°C to 85°C			±1000	
		V_{CM}=0V to 3V	25°C			±600	
Input Offset Voltage Average Drift	V_{OS} T_C	V_{CM}=1.5V to 3V	−40°C to 85°C		±5		μV/°C
Power-Supply Rejection Ratio	PSRR	V_S=5V to 25V	25°C	83	106		dB
			−40°C to 125°C	70			
NOISE							
Input Voltage Noise	e_n p-p	f= 0.1Hz to 10Hz	25°C		5		μV_{PP}
Input Voltage Noise Density	e_n	f= 10Hz	25°C		80		$nV/\sqrt{Hz}$
		f= 1KHz			16		
		f= 10KHz			14		
Input Current Noise Density	I_n	f= 0.1Hz	25°C		0.85		$fA/\sqrt{Hz}$
Total harmonic distortion + noise	THD+N	AV=1, f =1kHz, V_{IN} =0.5V rms	25°C		0.003		%
INPUT VOLTAGE							
Common-Mode Voltage Range	V_{CM}	V_S=5V	−40°C to 125°C	0		3.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=1.5V to 3.0V	25°C	83	102		dB
			−40°C to 125°C	70			
		V_{CM}=0 to 3.0V	25°C	65			
INPUT IMPEDANCE							
Input Resistance	R_{IN}				> 20		TΩ
Input Capacitance	C_{IN}				8		pF
OPEN-LOOP GAIN							
Open-Loop Voltage Gain	A_{OL}	R_L=10kΩ to V_{CM}, V_{OUT}=0.2V to 4.3V	25°C	110	130		dB
			−40°C to 125°C	105			
FREQUENCY RESPONSE							
Unity gain bandwidth	GBW	V_{IN} = 50mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 11	25°C		3.3		MHz
Unity-Gain Crossover	UGC	V_{IN} = 50 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1	25°C		3.3		MHz
Slew Rate (8)	SR	R_L=10kΩ, C_L=10pF, A_V=1	25°C		2.1		V/μs
Settling Time	t_S	V_{IN}=1V step, R_L=10kΩ, C_L=10 pF, A_V=−1	25°C		1.4		μs
Overload Recovery Time	t_{OR}	V_{IN} × G ≥ V_S, G=-10	25°C		1.0		μs
-3dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN}=20 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 1	25°C		6		MHz
Phase Margin	ΦM	V_{IN}=10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1	25°C		60		degree

ELECTRICAL CHARACTERISTICS (Continued)

(At T_A=+25°C, V_S= 5V, V_{CM}=V_{OUT}=V_S/2, and R_L=10kΩ connected to V_S/2, Full = -40°C to +125°C, unless otherwise noted.)(1)

PARAMETER	SYMBOL	CONDITION	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
OUTPUT							
Output Voltage	V_{OH}	R_L=2 KΩ	25°C		4.92		V
			−40°C to 125°C	4.85			
		R_L=10 KΩ	25°C		4.98		
			−40°C to 125°C	4.95			
	V_{OL}	R_L=2 KΩ	25°C		133		mV
			−40°C to 125°C			160	
		R_L=10 KΩ	25°C		29		
			−40°C to 125°C			40	
Output Source Current (6) (7)	I_{SOURCE}		25°C		30		mA
Output Sink Current (6) (7)	I_{SINK}				-20		
Closed-loop Output Impedance	Z_O	f = 1 MHz, A_V=1	25°C		40		Ω
POWER SUPPLY							
Quiescent Current Per Amplifier	I_Q	I_{OUT}=0A	25°C		1.0	1.6	mA
			−40°C to 125°C			1.8	
INTERNAL GUARD BUFFER							
Guard Offset Voltage	V_{GOS}	V_{CM}=1.5V to 3V	25°C		±75	±400	µV
		V_{CM}=1.5V to 3V	−40°C to 125°C			±800	
		V_{CM}=0.1V to 3V	25°C			±500	
Guard Offset Voltage Drift	$\Delta V_{GOS}/\Delta T$		−40°C to 125°C		1		µV/°C
Output Impedance	Z_{GOUT}		25°C		1		kΩ
Output Voltage Range		V_{GOS} < ±500µV	25°C	0.1		3	V
-3dB Bandwidth	$f_{-3dBGUARD}$	V_{IN} = 20mV rms, C_L = 10pF	25°C		3		MHz

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) This parameter is ensured by design and/or characterization and is not tested in production.

(5) Positive current corresponds to current flowing into the device.

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = ($T_{J(MAX)}$ - T_A) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(7) Short circuit test is a momentary test.

(8) Number specified is the slower of positive and negative slew rates.

ELECTRICAL CHARACTERISTICS

(At T_A=+25°C, V_S= 25V, V_{CM}=V_{OUT}=V_S/2, and R_L=10kΩ connected to V_S/2, Full = -40°C to +125°C, unless otherwise noted.)(1)

PARAMETER	SYMBOL	CONDITION	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
INPUT BIAS CURRENT							
Input Bias Current (4) (5)	I_B		25°C		±50	±200	fA
Input Offset Current (4)	I_{OS}		25°C		±50	±200	fA
OFFSET VOLTAGE							
Input Offset Voltage	V_{OS}	V_{CM}=V_S/2	25°C		±100	±900	μV
		V_{CM}=1.5V to 21V	−40°C to 85°C			±2000	
		V_{CM}=0V to 23V	25°C			±2000	
Input Offset Voltage Average Drift	V_{OS} T_C	V_{CM}=1.5V to 23V	−40°C to 85°C		±3.5		μV/°C
Power-Supply Rejection Ratio	PSRR	V_S=5V to 25V	25°C	83	106		dB
			−40°C to 125°C	70			
NOISE							
Input Voltage Noise	e_n p-p	f= 0.1Hz to 10Hz	25°C		5.5		μV_{PP}
Input Voltage Noise Density	e_n	f= 10Hz	25°C		80		$nV/\sqrt{Hz}$
		f= 1KHz			16		
		f= 10KHz			14		
Input Current Noise Density	I_n	f= 0.1Hz	25°C		0.85		$fA/\sqrt{Hz}$
Total harmonic distortion + noise	THD+N	A_V=1, f =1kHz, V_{IN} =4.5V rms	25°C		0.003		%
INPUT VOLTAGE							
Common-Mode Voltage Range	V_{CM}	V_S=25V	−40°C to 125°C	0		23	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=1.5V to 21V	25°C	95	120		dB
			−40°C to 125°C	90			
		V_{CM}=0 to 23V	25°C	80	85		
INPUT IMPEDANCE							
Input Resistance	R_{IN}				> 20		TΩ
Input Capacitance	C_{IN}				8		pF
OPEN-LOOP GAIN							
Open-Loop Voltage Gain	A_{OL}	R_L=10kΩ, V_{OUT}=0.5V to 24.5V	25°C	110	130		dB
			−40°C to 125°C	105			
FREQUENCY RESPONSE							
Unity gain bandwidth	GBW	V_{IN} = 50mV rms, R_L = 10kΩ, C_L = 10 pF, A_V = 11	25°C		3.3		MHz
Unity-Gain Crossover	UGC	V_{IN} = 50mV rms, R_L = 10 kΩ, C_L = 10pF, A_{VO} = 1	25°C		3.3		MHz
Slew Rate (8)	SR	R_L=10kΩ, C_L=10pF, A_V=1	25°C		2.1		V/μs
Settling Time	t_S	V_{IN} = 2V step, R_L = 10kΩ, C_L = 10 pF, A_V = −1	25°C		2.0		μs
Overload Recovery Time	t_{OR}	V_{IN} × G ≥ V_S, G=-10	25°C		1.0		μs
-3dB Closed-Loop Bandwidth	f_{-3dB}	V_{IN}=20 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_V = 1	25°C		6		MHz
Phase Margin	ΦM	V_{IN}=10 mV rms, R_L = 10 kΩ, C_L = 10 pF, A_{VO} = 1	25°C		60		degree

ELECTRICAL CHARACTERISTICS (Continued)

(At T_A=+25°C, V_S= 25V, V_{CM}=V_{OUT}=V_S/2, and R_L=10kΩ connected to V_S/2, Full = -40°C to +125°C, unless otherwise noted.)(1)

PARAMETER	SYMBOL	CONDITION	TEMP	MIN(2)	TYP(3)	MAX(2)	UNIT
OUTPUT							
Output Voltage	V_{OH}	R_L=2 KΩ	25°C		24.62		V
			−40°C to 125°C	24.5			
		R_L=10 KΩ	25°C	24.8	24.92		
			−40°C to 125°C	24.75			
	V_{OL}	R_L=2 KΩ	25°C		0.61		V
			−40°C to 125°C			0.75	
		R_L=10 KΩ	25°C		0.13	0.2	
			−40°C to 125°C			0.22	
Output Source Current (6) (7)	I_{SOURCE}		25°C		70		mA
Output Sink Current (6) (7)	I_{SINK}				-50		
Closed-loop Output Impedance	Z_O	f = 1 MHz, A_V=1	25°C		40		Ω
POWER SUPPLY							
Quiescent Current Per Amplifier	I_Q	I_{OUT}=0A	25°C		1.1	2.0	mA
			−40°C to 125°C			2.2	
INTERNAL GUARD BUFFER							
Guard Offset Voltage	V_{GOS}	V_{CM}=1.5V to 23V	25°C		±80	±400	µV
		V_{CM}=1.5V to 23V	−40°C to 125°C			±1000	
		V_{CM}= 0.1 to 23V	25°C		±80	±500	
Guard Offset Voltage Drift	$\Delta V_{GOS}/\Delta T$		−40°C to 125°C		2.6		µV/°C
Output Impedance	Z_{GOUT}		25°C		1		kΩ
Output Voltage Range		V_{GOS} < ±500µV	25°C	0.1		23.5	V
-3dB Bandwidth	$f_{-3dBGUARD}$		25°C		3		MHz

NOTE:

(1) Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

(4) This parameter is ensured by design and/or characterization and is not tested in production.

(5) Positive current corresponds to current flowing into the device.

(6) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = ($T_{J(MAX)}$ - T_A) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(7) Short circuit test is a momentary test.

(8) Number specified is the slower of positive and negative slew rates.

7.5 TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

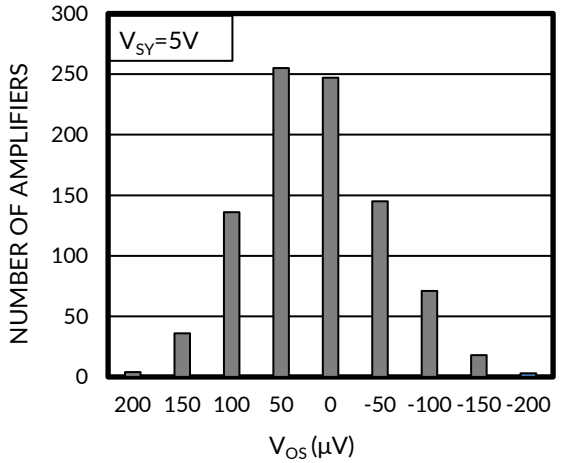


Figure 1. Input Offset Voltage Distribution

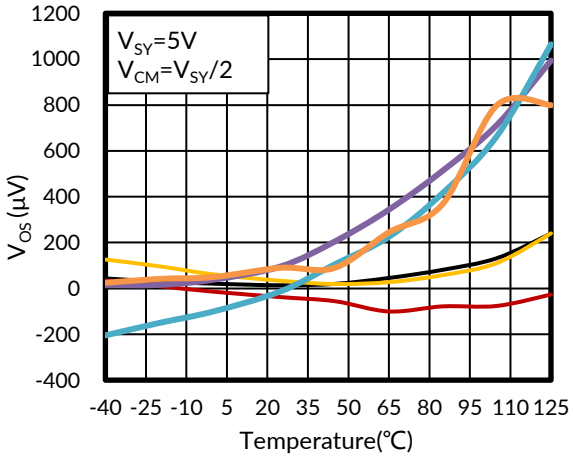


Figure 2. Input Offset Voltage (V_{OS}) vs Temperature

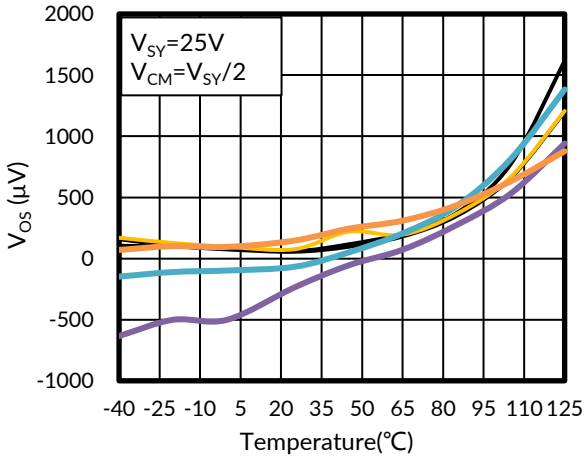


Figure 3. Input Offset Voltage (V_{OS}) vs Temperature

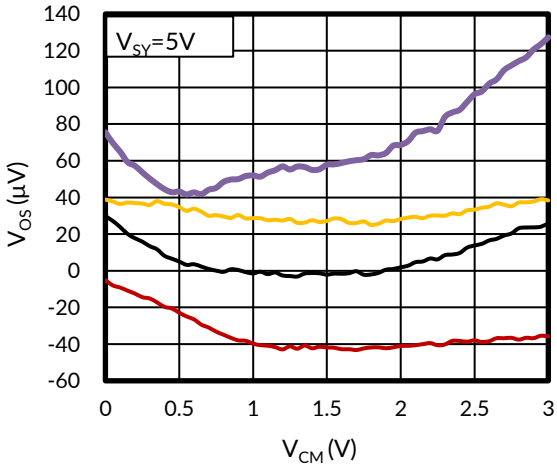


Figure 4. Input Offset Voltage (V_{OS}) vs Common-Mode Voltage (V_{CM})

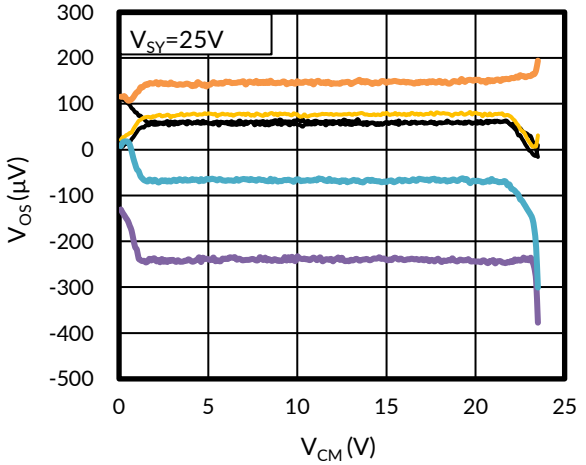


Figure 5. Input Offset Voltage (V_{OS}) vs Common-Mode Voltage (V_{CM})

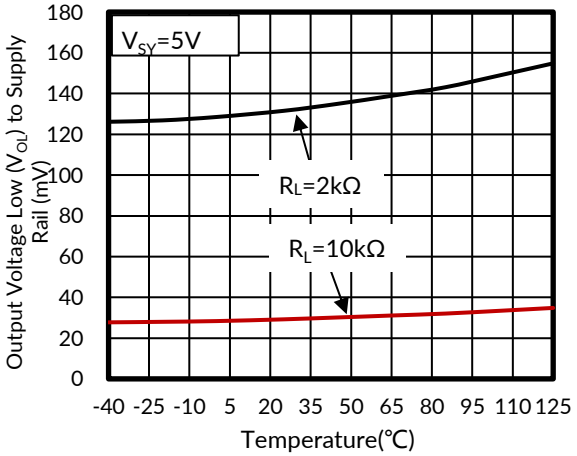


Figure 6. Output Voltage Low (V_{OL}) to Supply Rail vs Temperature

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

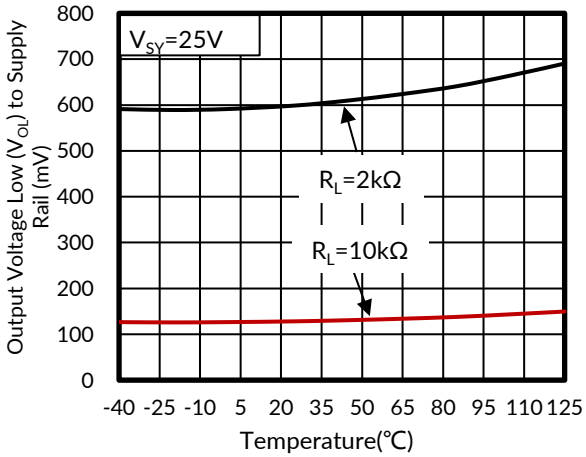


Figure 7. Output Voltage Low (V_{OL}) to Supply Rail vs Temperature

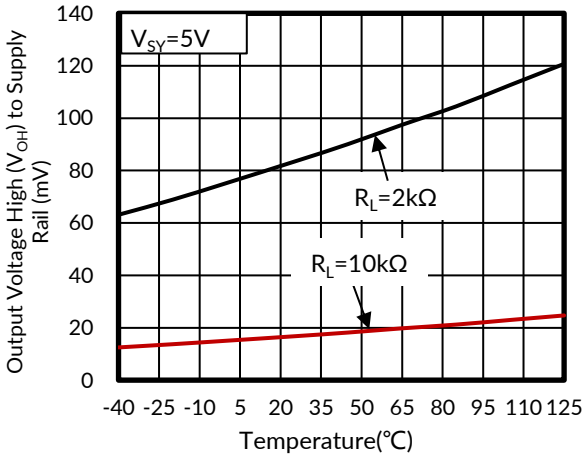


Figure 8. Output Voltage High (V_{OH}) to Supply Rail vs Temperature

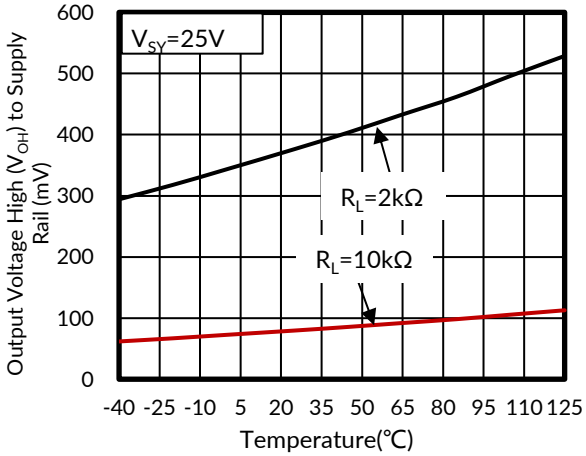


Figure 9. Output Voltage High (V_{OH}) to Supply Rail vs Temperature

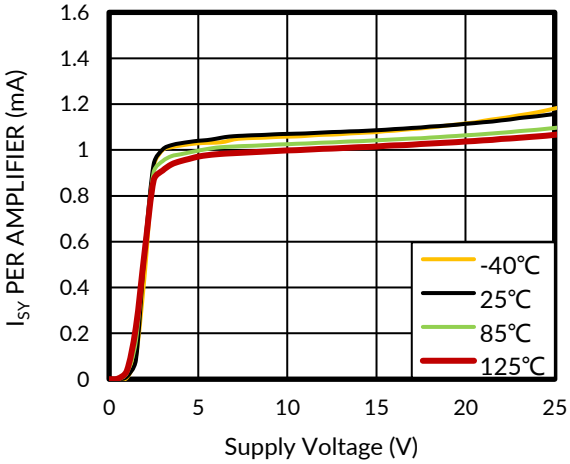


Figure 10. Supply Current (I_{SY}) per Amplifier vs Supply Voltage (V_{SY})

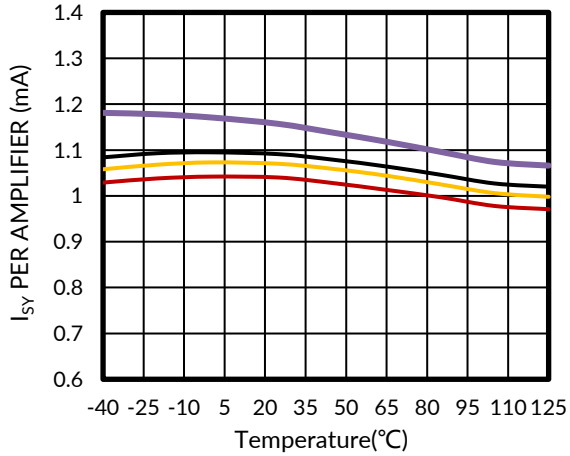


Figure 11. Supply Current (I_{SY}) per Amplifier vs Temperature

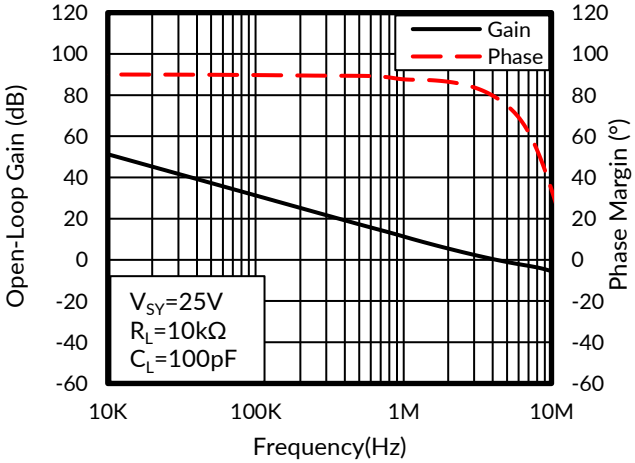


Figure 12. Open-Loop Gain and Phase Margin vs Frequency

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

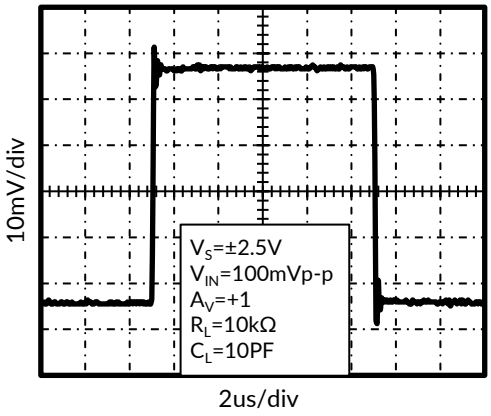


Figure 13. Small-Signal Step Response

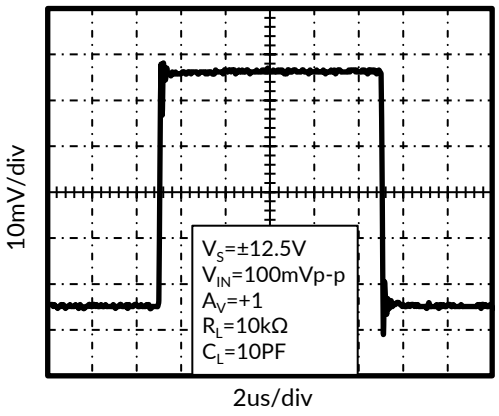


Figure 14. Small-Signal Step Response

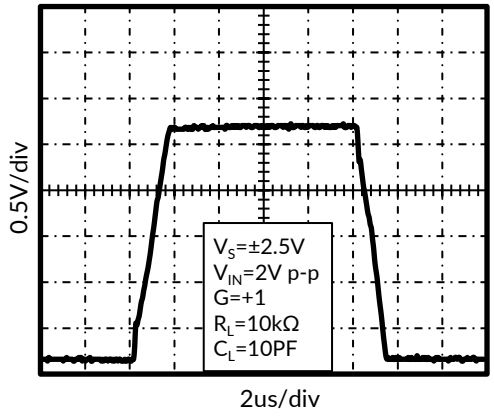


Figure 15. Large-Signal Step Response

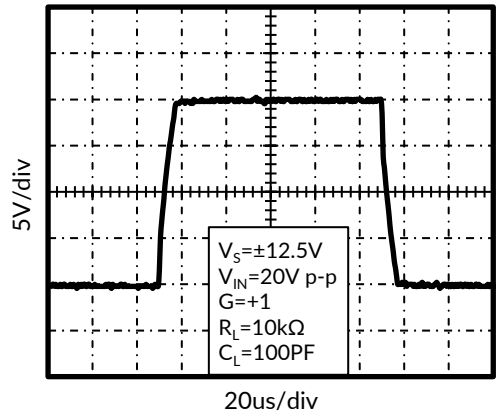


Figure 16. Large-Signal Step Response

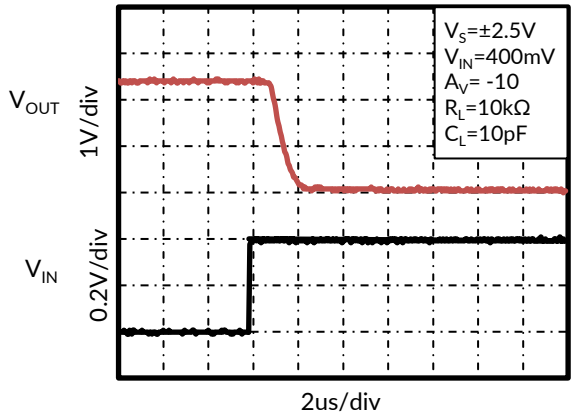


Figure 17. Positive Overload Recovery

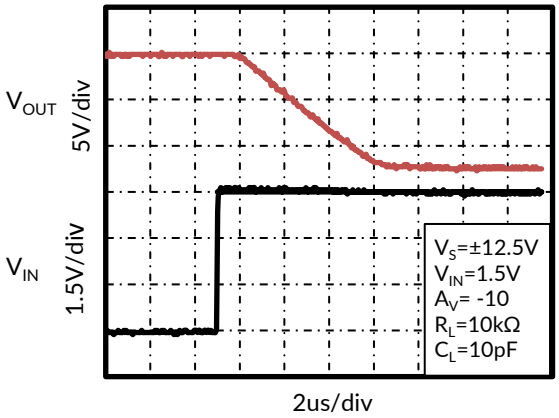


Figure 18. Positive Overload Recovery

TYPICAL CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

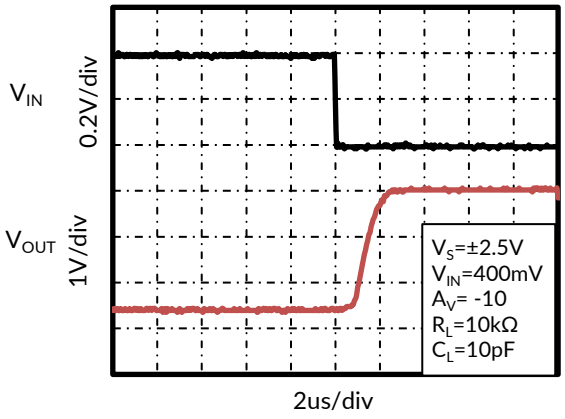


Figure 19. Negative Overload Recovery

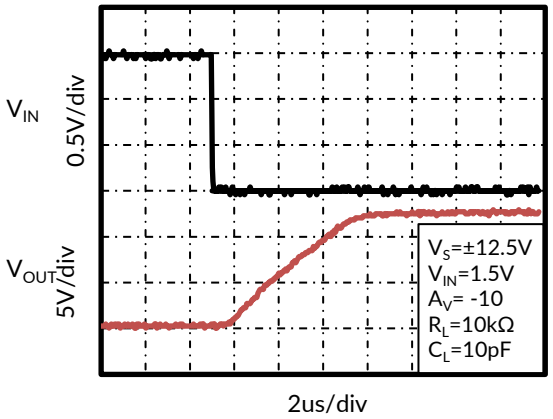


Figure 20. Negative Overload Recovery

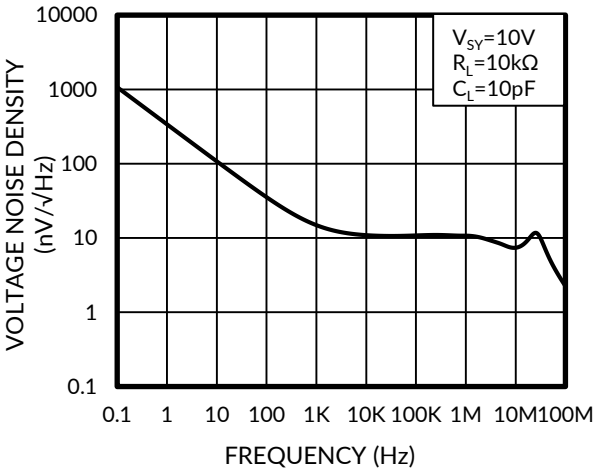


Figure 21. Voltage Noise Density vs Frequency

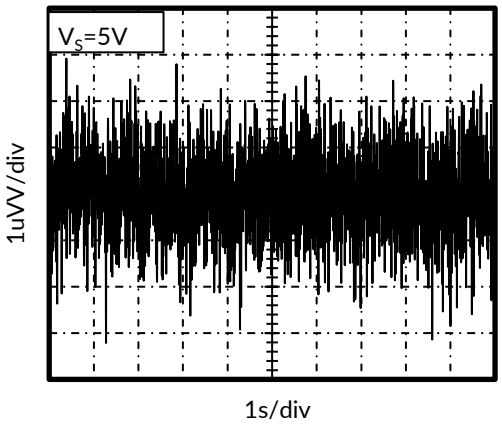


Figure 22. 0.1Hz to 10Hz Input Voltage Noise

GUARD AMPLIFIER

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

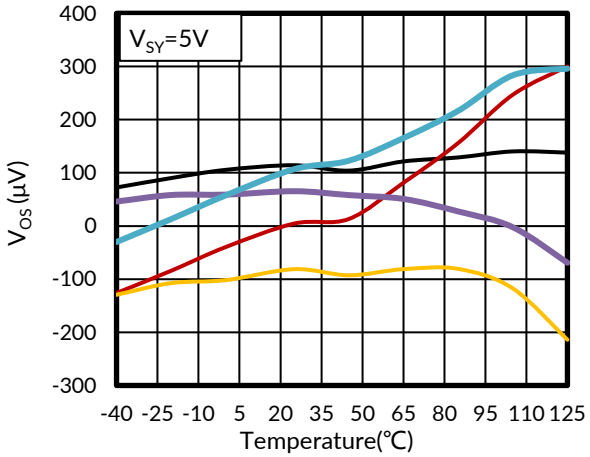


Figure 23. Input Offset Voltage (V_{OS}) vs Temperature

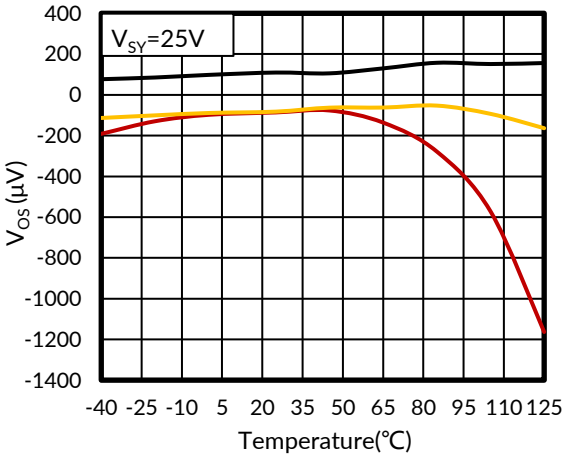


Figure 24. Input Offset Voltage (V_{OS}) vs Temperature

8 Application and Implementation

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 ESD STRUCTURE

The input ESD structure consists of Diode D1 to Diode D6. The noninverting input is coupled to the guard pins (GRD) by the D1 and D2 antiparallel diodes. The inverting input is coupled to the guard pins by the D3 and D4 antiparallel diodes.

The guard pins are connected to the power supplies through Diode D5 and Diode D6. During ESD events, the transient current flows from the input pins through one of the antiparallel diodes and harmlessly into the supplies through one of the power supply diodes. During normal operation, the guard buffer (BUF1) forces the voltage across the antiparallel diodes to 0V. Resistor R1 shields the guard buffer from potentially large capacitances connected to the guard pins. Its value is nominally 1kΩ.

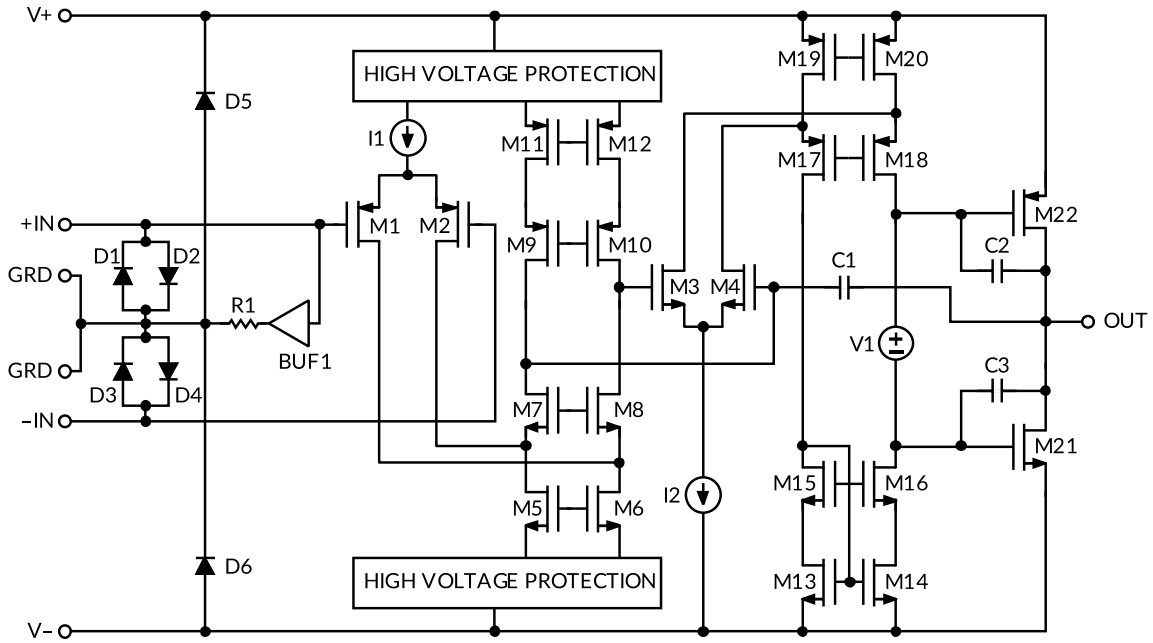


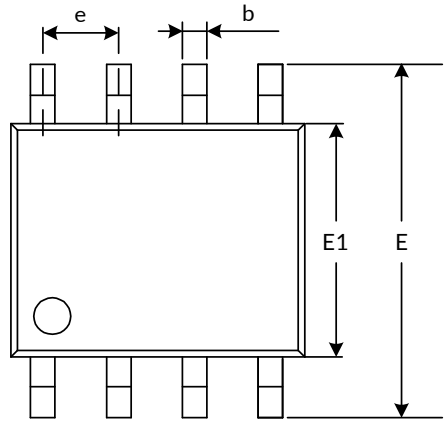
Figure 25. Simplified Schematic

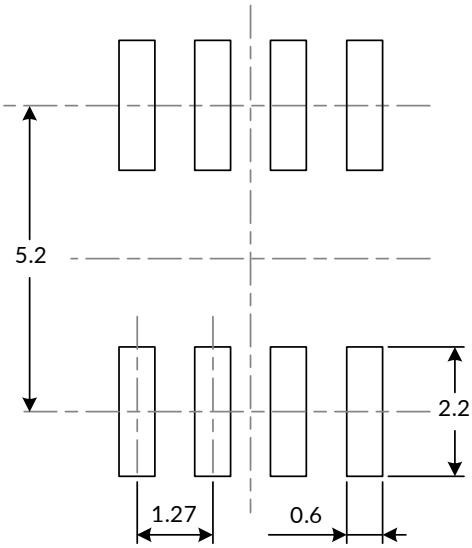
8.2 GUARD BUFFER

The guard buffer (BUF1) is a unity-gain amplifier that creates a low impedance replica of the input common-mode voltage. The buffer input is connected to the noninverting input (IN+). The noninverting input voltage is approximately equal to the input common-mode voltage when the main amplifier feedback loop is settled.

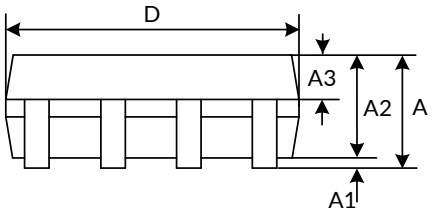
9 PACKAGE OUTLINE DIMENSIONS

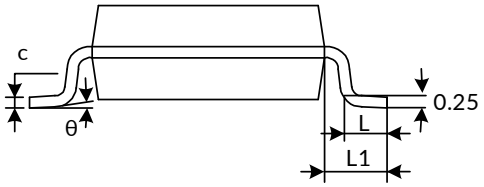
SOIC-8(SOP8) (4)





RECOMMENDED LAND PATTERN (Unit: mm)





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.750		0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.500	0.049	0.059
A3	0.600	0.700	0.024	0.028
b	0.360	0.490	0.014	0.019
c	0.190	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
E1 (1)	3.800	4.000	0.150	0.157
E	5.800	6.200	0.228	0.244
e	1.270 (BSC) (2)		0.050 (BSC) (2)	
L	0.400	1.000	0.016	0.039
L1	1.050 (REF) (3)		0.041 (REF) (3)	
θ	0°	8°	0°	8°

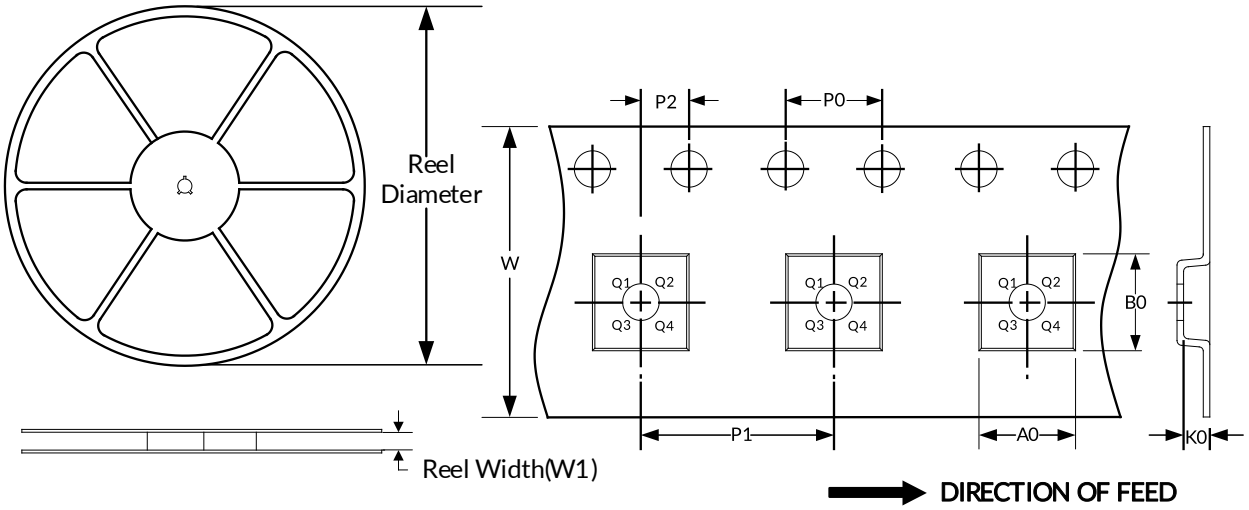
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. REF is the abbreviation for Reference.
4. This drawing is subject to change without notice.

10 TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8(SOP8)	13”	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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