Dual 5A High-Speed, Low-Side Gate Driver

1 FEATURES

- **Industry-Standard Pinout**
- **Two Independent Gate-Drive Channels**
- **5A Peak Source and Sink-Drive Current**
- **TTL and CMOS Compatible Logic Threshold Independent of Supply Voltage**
- **Hysteretic-Logic Thresholds for High Noise Immunity**
- **Inputs Pin-Voltage Levels Not Restricted by VDD Pin Bias Supply Voltage**
- **4.5V to 18V Single-Supply Range**
- **Outputs Held Low During VDD-UVLO, (Ensures Glitch-Free Operation at Power up and Power Down)**
- **Fast Propagation Delays (13ns Typical)**
- **Fast Rise and Fall Times (7ns and 6ns Typical)**
- **Two Outputs are in Parallel for Higher Drive Current**
- **Outputs Held Low When Inputs Floating**
- **Operating Temperature Range of –40°C to 140°C**
- **Micro SIZE PACKAGES: SOIC-8(SOP8)**

2 APPLICATIONS

- **Switched-Mode Power Supplies**
- **DC-DC Converters**
- **Motor Control, Solar Power**
- **Gate Drive for Emerging Wide Band-Gap Power Devices such as GaN**

3 DESCRIPTIONS

The RS8802 dual-channel, high-speed, low-side gate driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the RS8802 is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13ns.

The RS8802 device is capable of handling -4V at input. In addition, the drivers feature matched internal propagation delays between the two channels, these delays are very well suited for applications requiring dual-gate drives with critical timing, such as synchronous rectifiers. This also enables connecting two channels in parallel to effectively increase current-drive capability or driving two switches in parallel with one input signal.

The RS8802 provides 5A source and 5A sink (symmetrical drive) peak-drive current capability at VDD = 12V.

The RS8802 is designed to operate over a wide VDD range of 4.5 V to 18 V and wide temperature range of -40°C to 140°C. Internal Undervoltage Lockout (UVLO) circuitry on VDD pin holds output low outside VDD operating range. The capability to operate at low voltage levels such as below 5V, along with best-in-class switching characteristics, is especially suited for driving emerging wide band-gap power-switching devices as GaN power semiconductor devices.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS8802	SOIC-8(SOP8)	4.90mm×3.90mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Typical Application Diagrams

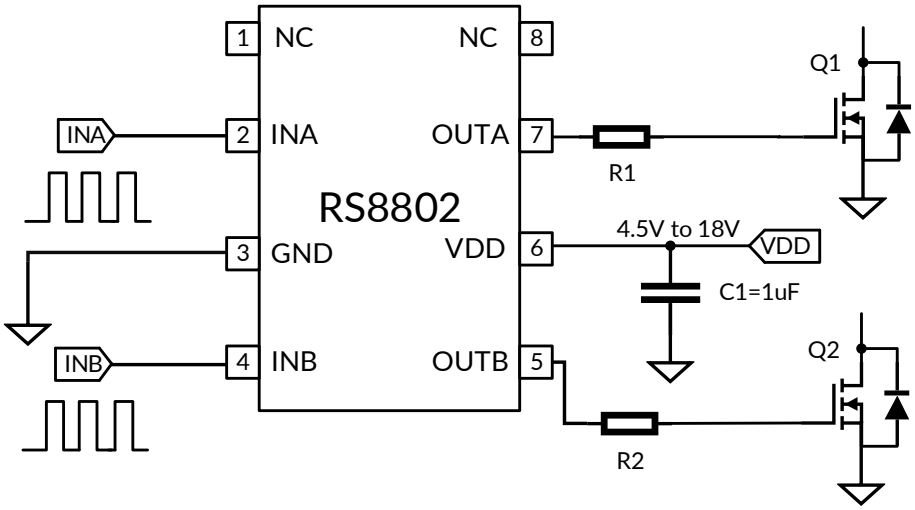


Table of Contents

5 Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2023/12/22	Initial version completed

6 PACKAGE/ORDERING INFORMATION (1)

Orderable Device	Package Type	Op Temp(°C)	Device Marking (2)	MSL (3)	Package Qty
RS8802HXK	SOIC-8(SOP8)	-40°C ~+140°C	RS8802	MSL1	Tape and Reel,4000

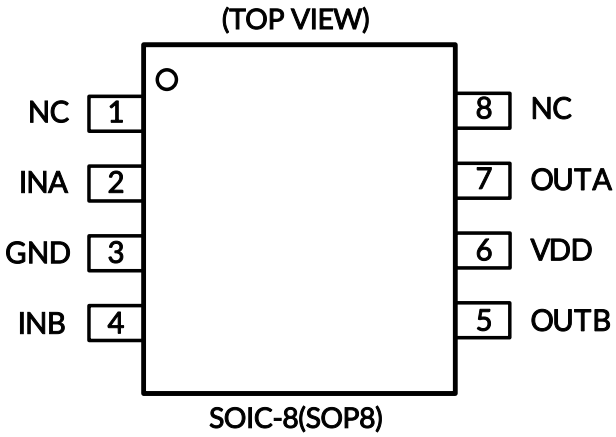
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.

7 Pin Configuration and Functions (Top View)



Pin Description

SOIC-8(SOP8)		I/O (1)	DESCRIPTION
NUMBER	NAME		
1	NC	--	No connection
2	INA	I	Input to channel A. OUTA held LOW if INA is unbiased or floating.
3	GND	G	Ground
4	INB	I	Input to channel B. OUTB held LOW if INB is unbiased or floating.
5	OUTB	O	Output of Channel B
6	VDD	P	Supply input.
7	OUTA	O	Output of Channel A
8	NC	--	No connection

(1) I=input, O=output, G= Ground.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

			MIN	MAX	UNIT
Supply voltage	VDD		-0.3	22	V
OUT voltage	DC		-0.3	VDD+0.3	V
	Repetitive pulse less than 200ns (4)		-2	VDD+0.3	
Output continuous current	I_{OUT_DC}(Source/Sink)			0.4	A
Output pulsed current (0.5us)	I_{OUT_pulsed} (Source/Sink)			5	A
Input voltage	INA, INB (5)		-4	22	V
θ_{JA}	Package thermal impedance (6)	SOIC-8(SOP8)		110	°C/W
T_J operating virtual junction temperature range (7)			-40	150	°C
Storage Temperature Range			-65	150	°C
Lead Temperature (Soldering, 10s)				260	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.

(3) These devices are sensitive to electrostatic discharge; follow proper device-handling procedures.

(4) Values are verified by characterization on bench.

(5) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.

(6) The package thermal impedance is calculated in accordance with JESD-51.

(7) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), MIL-STD-883K METHOD 3015.9	±3000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000	

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	4.5	12	18	V
Operating junction temperature range	-40		140	°C
Input voltage, INA, INB	0		18	V

8.4 ELECTRICAL CHARACTERISTICS

VDD=12V, T_J=-40°C to 140°C, 1μF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
BIAS CURRENTS							
$I_{DD(OFF)}$	Startup current	VDD=3.4V	INA=VDD, INB=GND	35	47	80	uA
			INA = INB = GND	33	45	75	uA
			INA=VDD, INB=VDD	40	51	85	uA
I_{DD}	Startup current	VDD=12V	INA=VDD, INB=GND	270	310	430	uA
			INA = INB = GND	190	220	310	uA
			INA=VDD, INB=VDD	350	400	540	uA
UNDER VOLTAGE LOCKOUT (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C			4.3		V
		T_A = -40°C to 150°C		3.9	4.3	4.5	V
V_{OFF}	Minimum operating Voltage after supply start	T_A = -40°C to 150°C		3.45	4	4.45	V
V_{DD_H}	Supply voltage hysteresis	T_A = 25°C			0.3		V
INPUTS(INA,INB)							
V_{IN_H}	Input signal high threshold	Output high for INA/B pin				2.8	V
V_{IN_L}	Input signal low threshold	Output low for INA/B pin		1.0			V
R_{IN}	Input pull down resistor	VDD=12V,VIN=4V		150	235	310	kΩ
SOURCE/SINK Current (OUTA,OUTB)							
$I_{SRC/SNK}$ (2)	Source/ Sink peak current	C_{LOAD}=0.22μF, F_{SW} = 1kHz			±5		A
OUTPUTS (OUT)							
V_{OD}-V_{OH}	High output voltage	VDD = 12V, I_{OUT}=-10mA			30		mV
		VDD = 4.5V, I_{OUT}=-10mA			35		mV
V_{OL}	Low output voltage	VDD = 12V, I_{OUT}=10mA			5.05		mV
		VDD = 4.5V, I_{OUT}=10mA			5.15		mV
R_{OH}	Output pullup resistance	VDD = 12V, I_{OUT}=10mA			3	4.7	Ω
		VDD = 4.5V, I_{OUT}=10mA			3.5		
R_{OL}	Output pulldown resistance	VDD = 12V, I_{OUT}=10mA			0.5	0.7	Ω
		VDD = 4.5V, I_{OUT}=10mA			0.5		
SWITCHING CHARACTERISTICS							
T_R	Rise time (1) (2)	VDD = 12V, C_{LOAD}=1.8nF			7		ns
		VDD = 4.5V, C_{LOAD}=1.8nF			15.5		
T_F	Fall time (1) (2)	VDD = 12V, C_{LOAD}=1.8nF			6		ns
		VDD = 4.5V, C_{LOAD}=1.8nF			5.5		
t_{D1}	INA to output propagation delay (1) (2)	VDD=12V, 5V input pulse C_{LOAD} =1.8nF			13		ns
		VDD=4.5V, 5V input pulse C_{LOAD} =1.8nF			16		
t_{D2}	INB to output propagation delay (1) (2)	VDD=12V, 5V input pulse C_{LOAD} =1.8nF			13		ns
		VDD=4.5V, 5V input pulse C_{LOAD} =1.8nF			16		

(1) See timing diagrams in Figure 1, Figure 2.
(2) This parameter is ensured by design and/or characterization and is not tested in production.

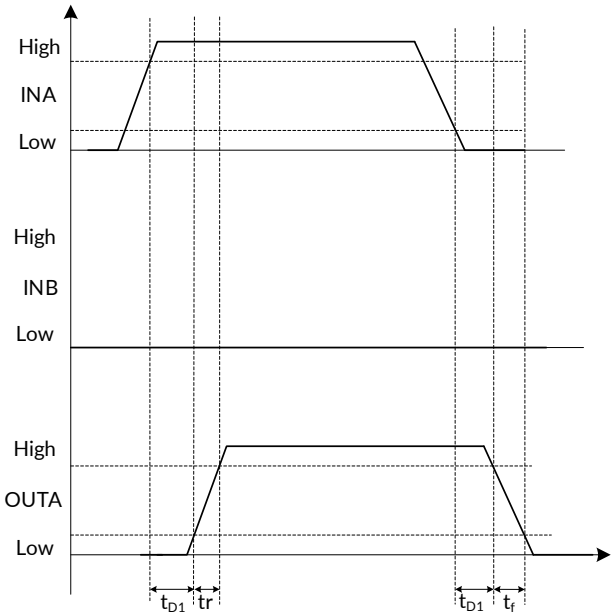


Figure 1. PWM Input to INA pin (INB pin tied to GND)

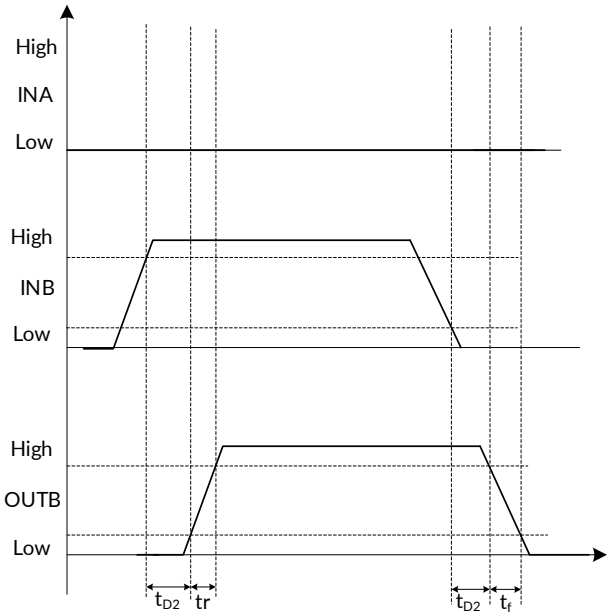


Figure 2. PWM Input to INB pin (INA pin tied to GND)

8.5 TYPICAL PERFORMANCE CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

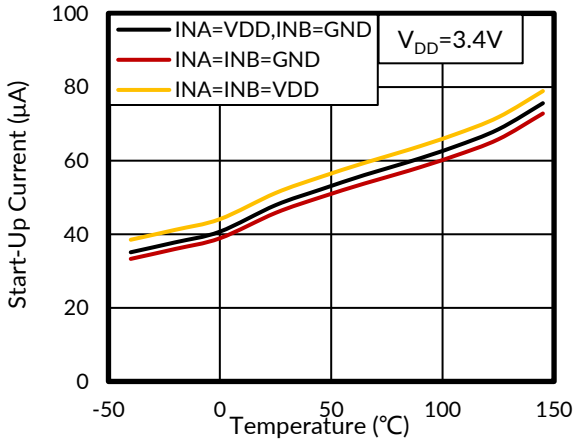


Figure 3. Start-Up Current vs Temperature

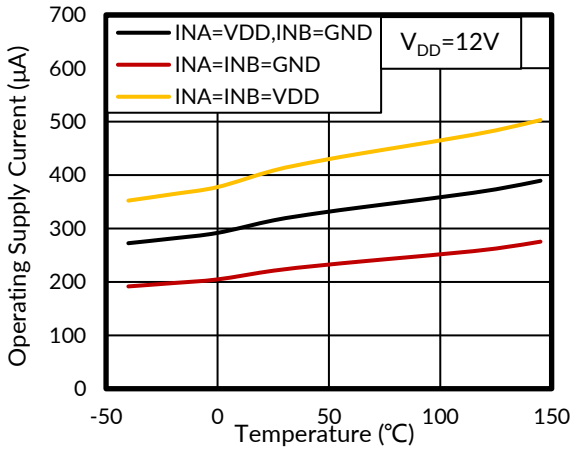


Figure 4. Supply Current vs Temperature (Output in DCON/OFF Condition)

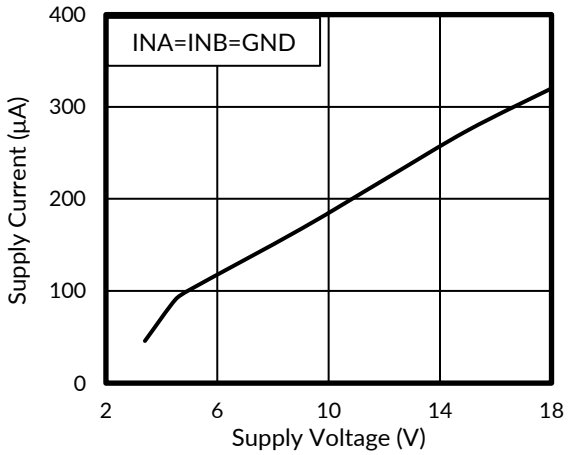


Figure 5. Supply Current vs Supply Voltage

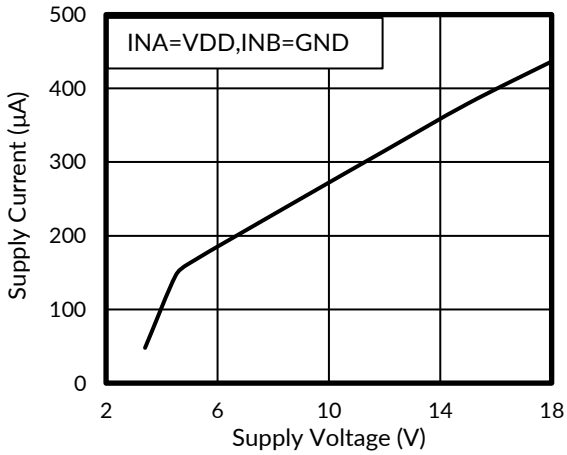


Figure 6. Supply Current vs Supply Voltage

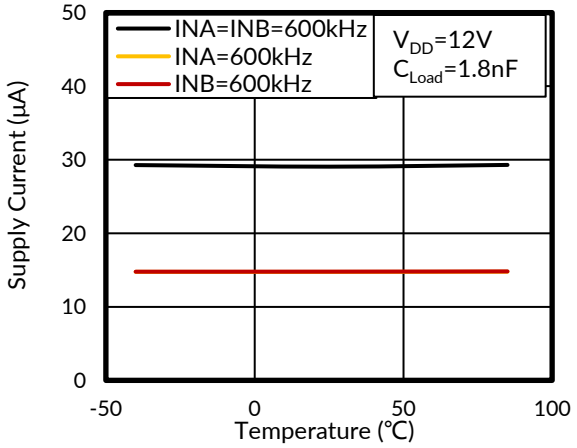


Figure 7. Operating Supply Current vs Temperature (Output Switching)

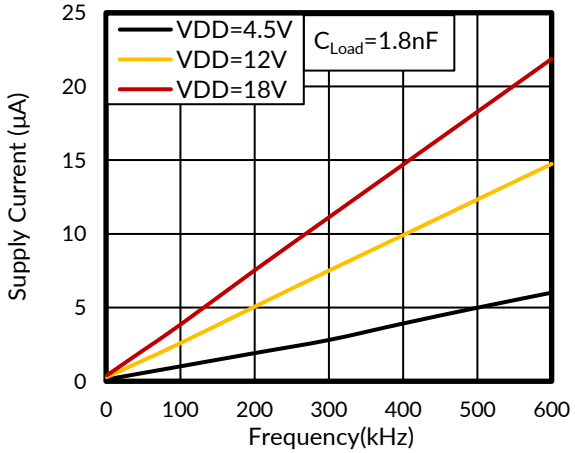


Figure 8. Single Channel Operating Supply Current vs Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

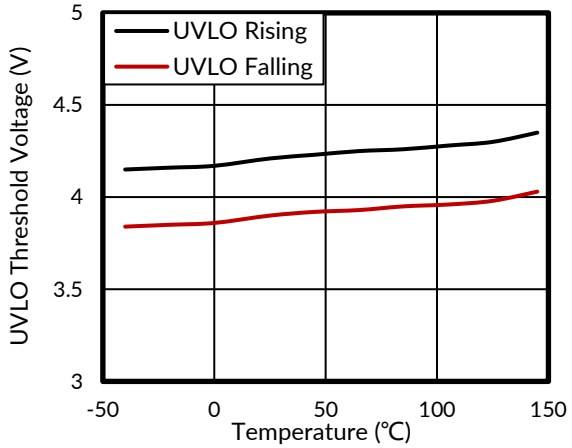


Figure 9. UVLO Threshold Voltage vs Temperature

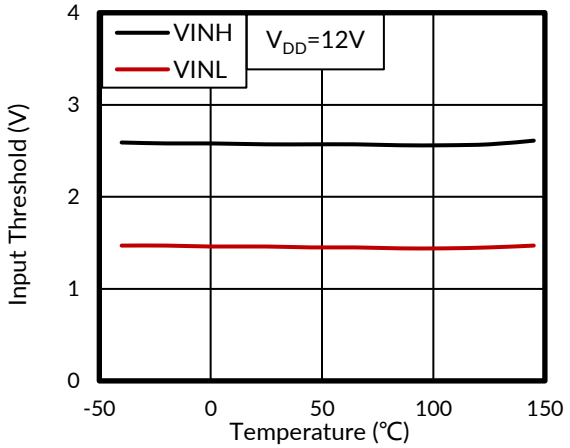


Figure 10. Input Threshold vs Temperature

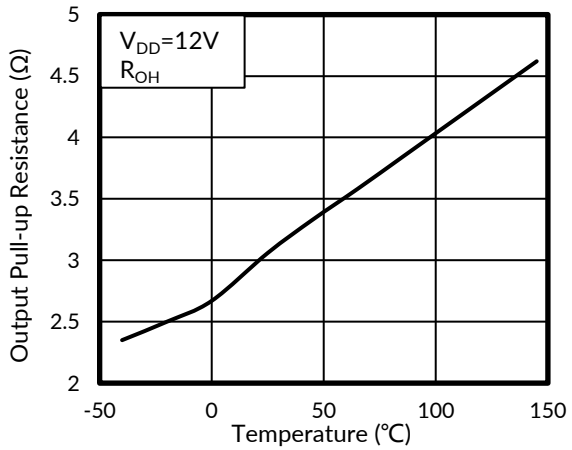


Figure 11. Output Pullup Resistance vs Temperature

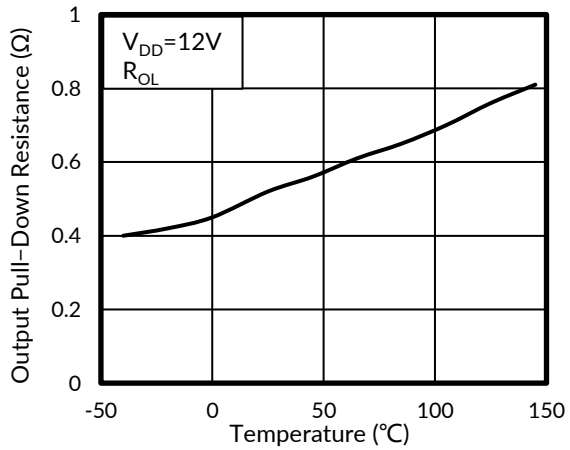


Figure 12. Output Pulldown Resistance vs Temperature

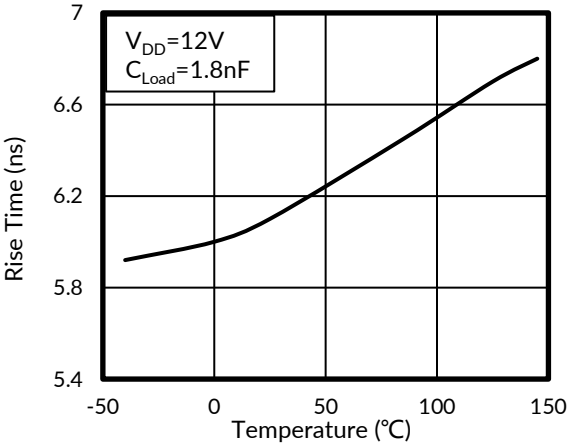


Figure 13. Rise Time vs Temperature

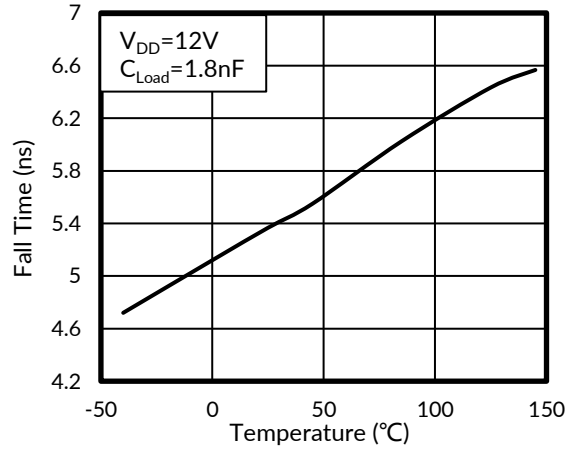


Figure 14. Fall Time vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

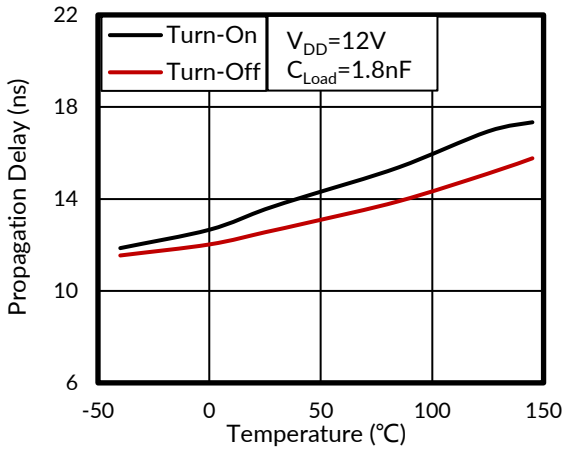


Figure 15. Input to Output Propagation Delay vs Temperature

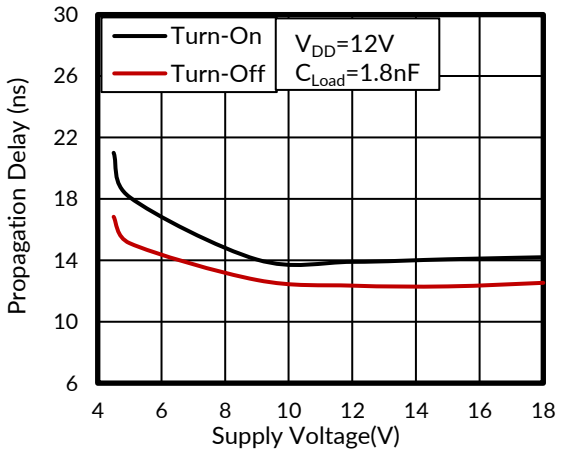


Figure 16. Propagation Delay vs Supply Voltage

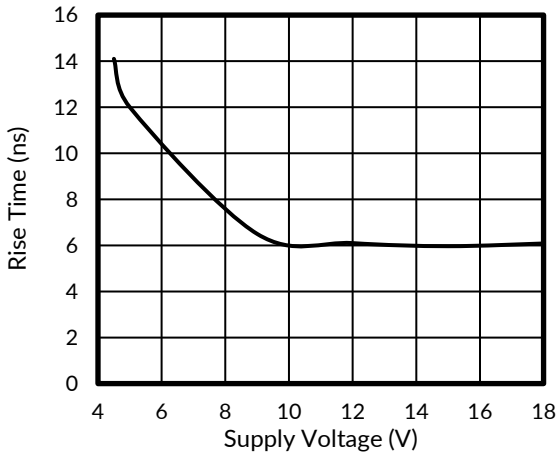


Figure 17. Rise Time vs Supply Voltage

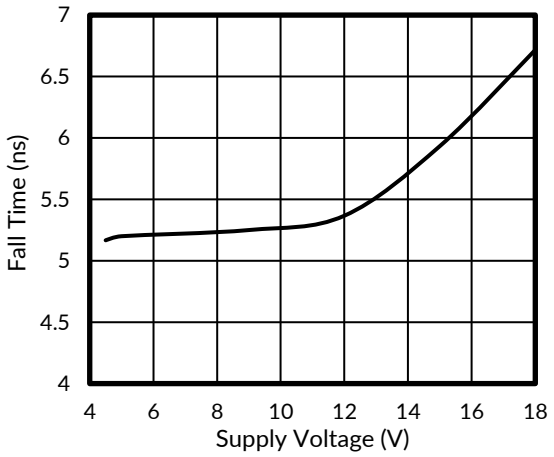


Figure 18. Fall Time vs Supply Voltage

9 Detailed Description

9.1 Overview

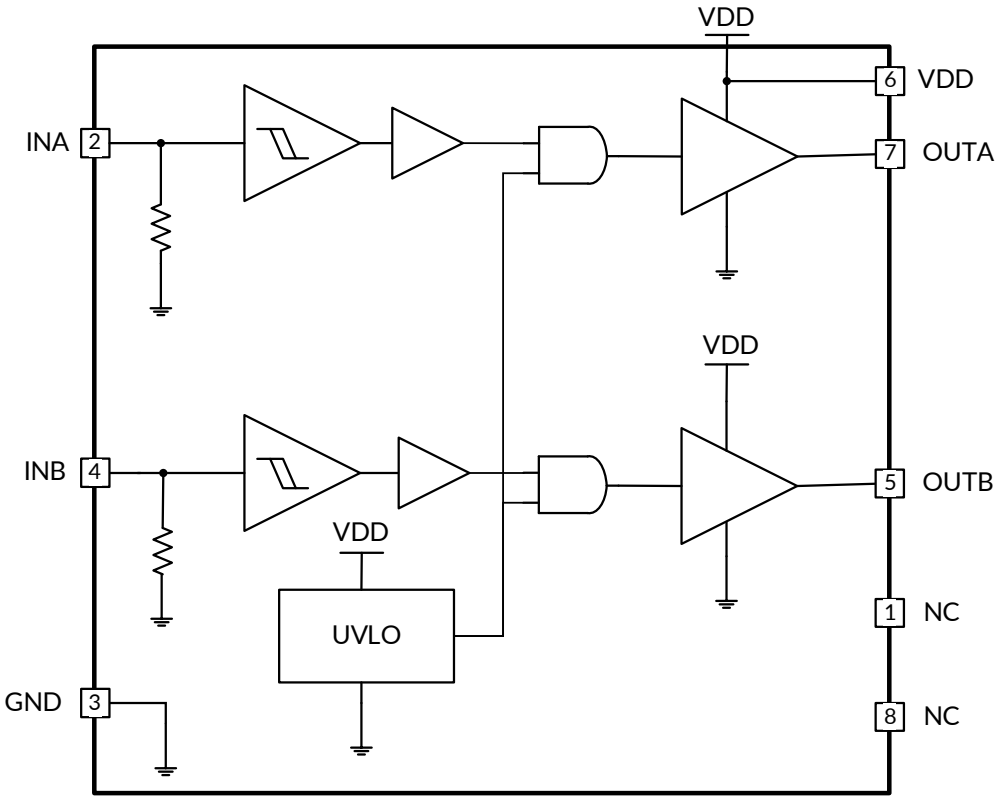
The RS8802 dual-channel, high-speed, low-side gate driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the RS8802 is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay typically 13ns.

The RS8802 device is capable of handling -4V at input.

The RS8802 provides 5A source and sink peak-drive current capability at VDD = 12V.

The RS8802 is designed to operate over a wide VDD range of 4.5V to 18V and wide temperature range of -40°C to 140°C.

9.2 Functional Block Diagram



9.3 V_{DD} and Undervoltage Lockout

The RS8802 has internal Undervoltage Lockout (UVLO) protection feature on the V_{DD}-pin supply-circuit blocks. Whenever the driver is in UVLO condition (for example when V_{DD} voltage is less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.3V with 300mV typical hysteresis.

Because the driver draws current from the V_{DD} pin to bias all internal circuits, for the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1μF ceramic capacitor should be located as close as possible to the V_{DD} to GND pins of the gate driver. In addition, a larger capacitor (such as 1μF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

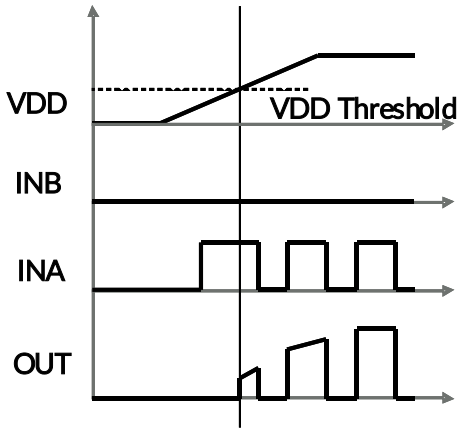


Figure 19. Power-Up (Non-Inverting Drive)

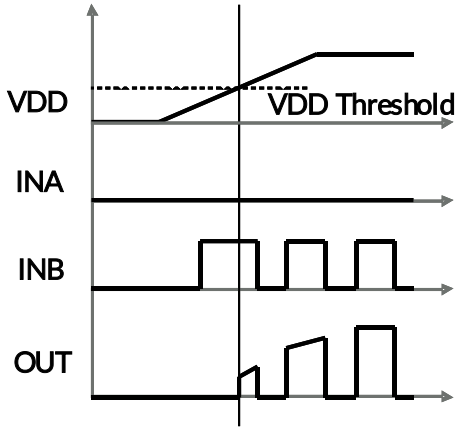


Figure20. Power-Up (Inverting Drive)

9.4 Device Functional Modes

In the normal mode the output state is dependent on states of the INA and INB pins. Table 1 below lists the output states for different input pin combinations.

Table 1. Device Logic Table

INA PIN	INB PIN	OUTA PIN	OUTB PIN
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
Any	Any	L	L
x (1)	x (1)	L	L

(1) x = Floating Condition.

10 Power Supply Recommendations

The bias supply voltage range for which the RS8802 device is rated to operate is from 4.5V to 18V. The lower end of this range is governed by the internal UVLO protection feature on the VDD pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 22V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 2V margin to allow for transient voltage spikes, the maximum recommended voltage for the VDD pin is 18V.

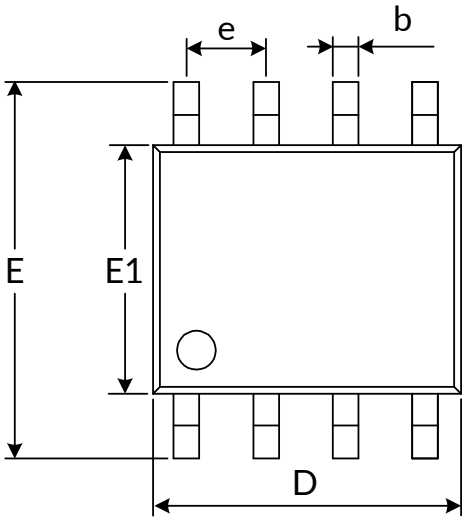
11 Layout

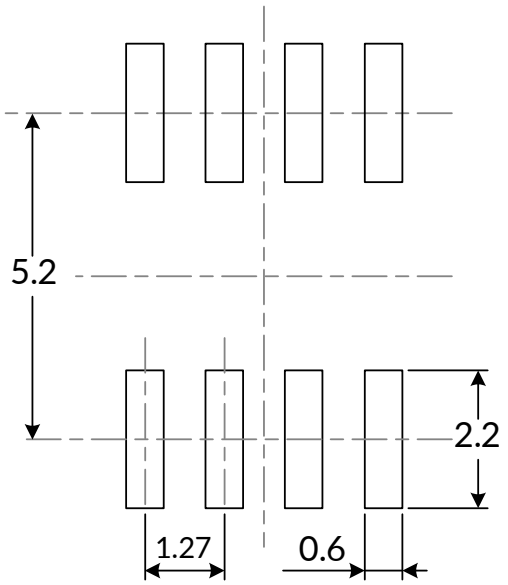
The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to the power device in order to minimize the length of high current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turn on of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.

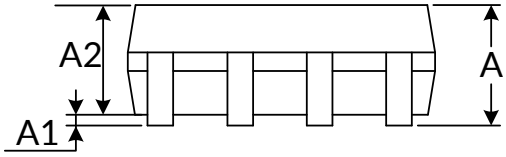
12 PACKAGE OUTLINE DIMENSIONS

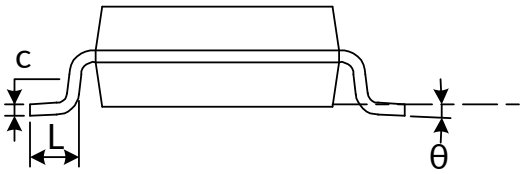
SOIC-8(SOP8) (3)





RECOMMENDED LAND PATTERN (Unit: mm)





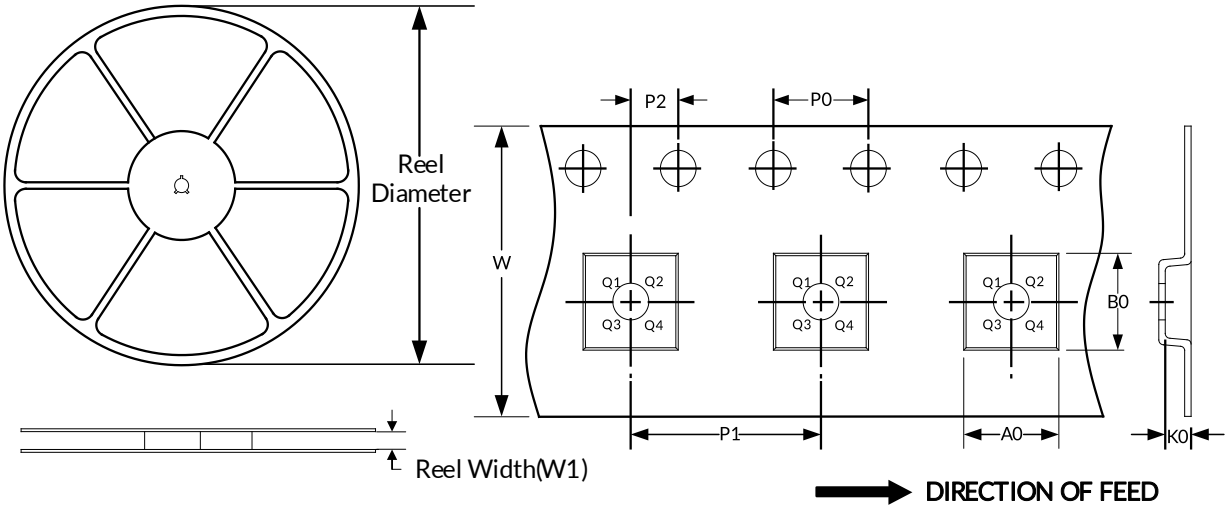
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D (1)	4.800	5.000	0.189	0.197
e	1.270(BSC) (2)		0.050(BSC) (2)	
E	5.800	6.200	0.228	0.244
E1 (1)	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

13 TAPE AND REEL INFORMATION

REEL DIMENSIONS **TAPE DIMENSION**



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width(mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8(SOP8)	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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