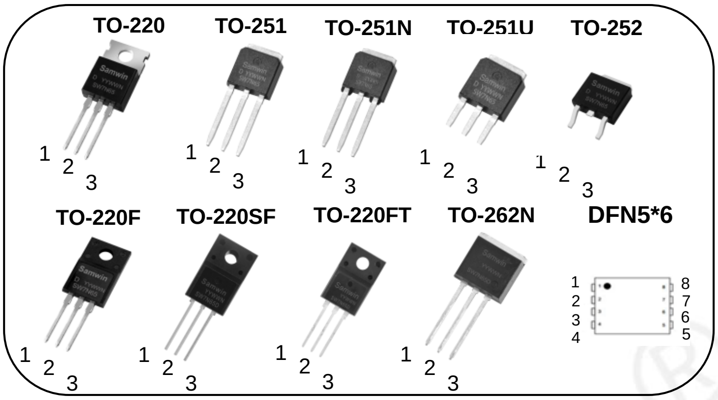
Samwin®

SW7N65D

*N-channel Enhanced mode TO-220/TO-251/TO-251N/TO-251U/TO-252/TO-220F/TO-220SF/TO-262N/DFN5*6/TO-220FT MOSFET*

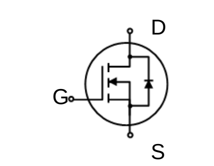
Features

- High ruggedness
- Low $R_{DS(ON)}$ (Typ 1.1Ω) @V_{GS}=10V
- Low Gate Charge (Typ 30nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application:Charger,LED, PC Power



TO-220(F/SF)&TO-251(N)&TO-252&TO-262N：1. Gate 2. Drain 3. Source
DFN5*6：4. Gate 5,6,7,8. Drain 1,2,3,4. Source

BV_{DSS} : 650V
I_D : 7A
$R_{DS(ON)}$: 1.1Ω



General Description

This power MOSFET is produced with advanced technology of SAMWIN.
This technology enable the power MOSFET to have better characteristics, including fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW P 7N65D	SW7N65D	TO-220	TUBE
2	SW I 7N65D	SW7N65D	TO-251	TUBE
3	SW N 7N65D	SW7N65D	TO-251N	TUBE
4	SW UI 7N65D	SW7N65D	TO-251U	TUBE
5	SW D 7N65D	SW7N65D	TO-252	REEL
6	SW F 7N65D	SW7N65D	TO-220F	TUBE
7	SW MN 7N65D	SW7N65D	TO-220SF	TUBE
8	SW J 7N65D	SW7N65D	TO-262N	TUBE
9	SW HA 7N65D	SW7N65D	DFN5*6	REEL
10	SW Y 7N65D	SW7N65D	TO-220FT	TUBE

Absolute maximum ratings

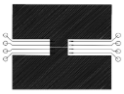
Symbol	Parameter	Value						Unit
		TO220	TO251/TO251N/TO251U	TO252	TO220F/TO220SF/TO220FT	TO262N	DFN5*6	
V_{DSS}	Drain to source voltage	650						V
I_D	Continuous drain current (@T_C=25°C)	7*						A
	Continuous drain current (@T_C=100°C)	4.4*						A
I_{DM}	Drain current pulsed (note 1)	28						A
V_{GS}	Gate to source voltage	±30						V
E_{AS}	Single pulsed avalanche energy (note 2)	430						mJ
E_{AR}	Repetitive avalanche energy (note 1)	40						mJ
dv/dt	Peak diode recovery dv/dt (note 3)	5						V/ns
P_D	Total power dissipation (@T_C=25°C)	208.3	173.6		27.8	186.6		W
	Total power dissipation (@T_a=25°C)						2.4	W
	Derating factor above 25°C	1.67	1.39		0.22	1.5	0.02	W/°C
T_{STG}, T_J	Operating junction temperature & storage temperature	-55 ~ + 150						°C
T_L	Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds.	300						°C

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value						Unit
		TO220	TO251/TO251N/TO251U	TO252	TO220F/TO220SF/TO220FT	TO262N	DFN5*6	
R_{thjc}	Thermal resistance, Junction to case	0.6	0.72		4.5	0.67		ºC/W
R_{thja}	Thermal resistance, Junction to ambient	60	82		50	61	51.4	ºC/W

Note: R_{thja} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is d efined as the solder mounting surface of the drain pins. R_{thjc} is guaranteed by design while R_{thca} is determined by the user's board design.



DFN5*6 R_{thja} ：51.4ºC/W on a 1 in^2 pad of 2oz copper.

Electrical characteristic (T_J= 25ºC unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	650			V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25ºC		0.51		V/ºC
I_{DSS}	Drain to source leakage current	V_{DS}=650V, V_{GS}=0V			1	uA
		V_{DS}=520V, T_J=125ºC			50	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V			100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V			-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	2.5		4.5	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D = 3.5A, T_J=25ºC		1.1	1.4	Ω
		V_{GS}=10V, I_D = 3.5A, T_J=125ºC		2.4		Ω
G_{fs}	Forward transconductance	V_{DS}=30 V, I_D =3.5A		6.3		S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		1230		pF
C_{oss}	Output capacitance			108		
C_{rss}	Reverse transfer capacitance			16		
$t_{d(on)}$	Turn on delay time	V_{DS}=350V, I_D=7A, R_G=25Ω (note 4,5)		16		ns
t_r	Rising time			36		
$t_{d(off)}$	Turn off delay time			83		
t_f	Fall time			40		
Q_g	Total gate charge	V_{DS}=520V, V_{GS}=10V, I_D=7A (note 4,5)		30		nC
Q_{gs}	Gate-source charge			5		
Q_{gd}	Gate-drain charge			15		
R_g	Gate resistance	V_{DS}=0V, Scan F mode		1.7		Ω

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			7	A
I_{SM}	Pulsed source current				28	A
V_{SD}	Diode forward voltage drop.	I_S=7A, V_{GS}=0V			1.4	V
t_{rr}	Reverse recovery time	I_S=7A, V_{GS}=0V, dI_F/dt=100A/us		436		ns
Q_{rr}	Reverse recovery charge			3.6		uC

※. Notes

1. Repeatitive rating : pulse width limited by junction temperature.
2. L = 17.5mH, I_{AS} = 7A, V_{DD} = 50V, R_G=25Ω, Starting T_J = 25ºC
3. I_{SD} ≤ 7A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25ºC
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%.
5. Essentially independent of operating temperature.

Fig. 1. On-state characteristics

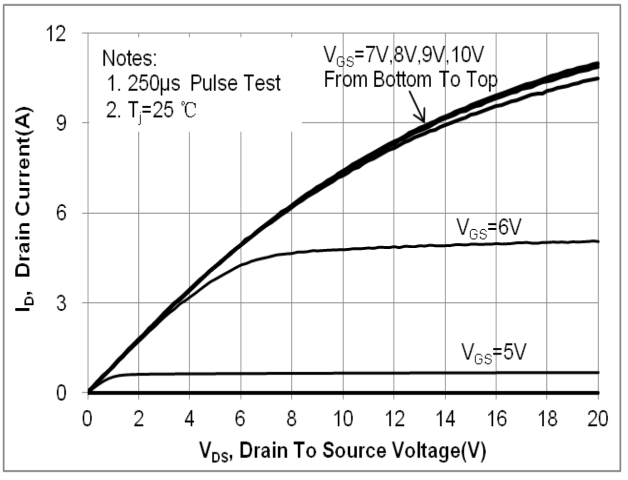


Fig. 2. Transfer Characteristics

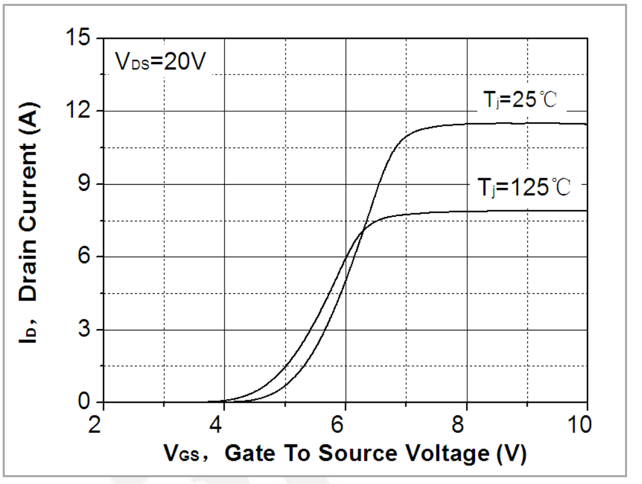


Fig. 3. On-resistance variation vs. drain current and gate voltage

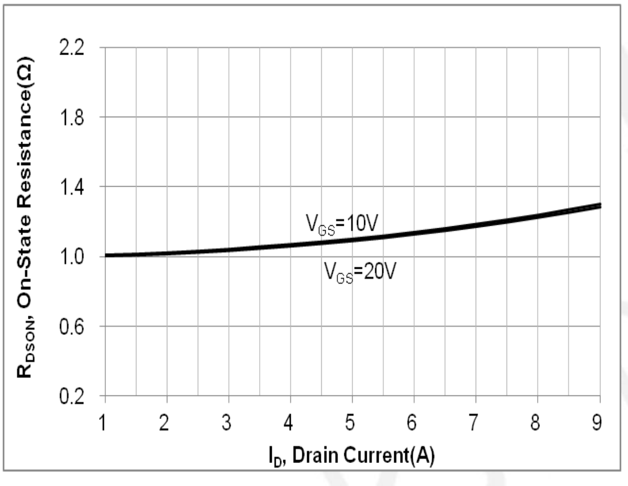


Fig. 4. On-state current vs. diode forward voltage

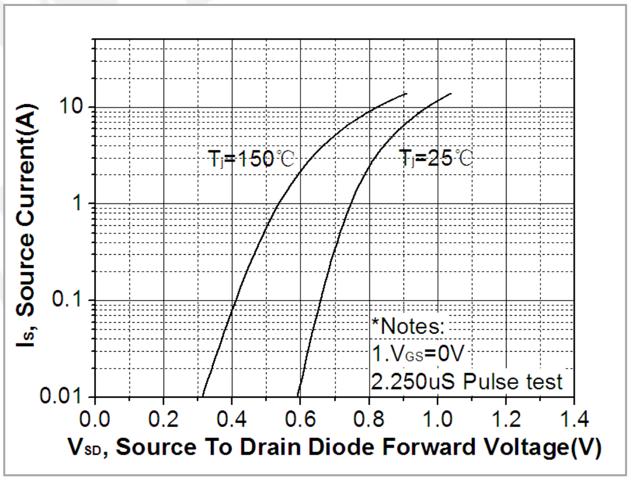


Fig 5. Breakdown Voltage Variation vs. Junction Temperature

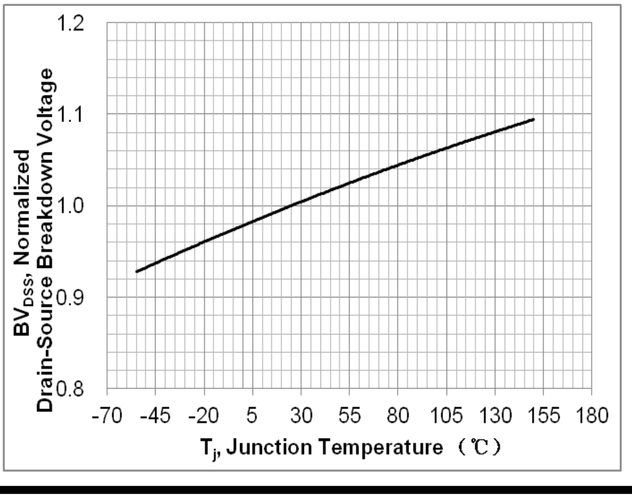


Fig. 6. On resistance variation vs. junction temperature

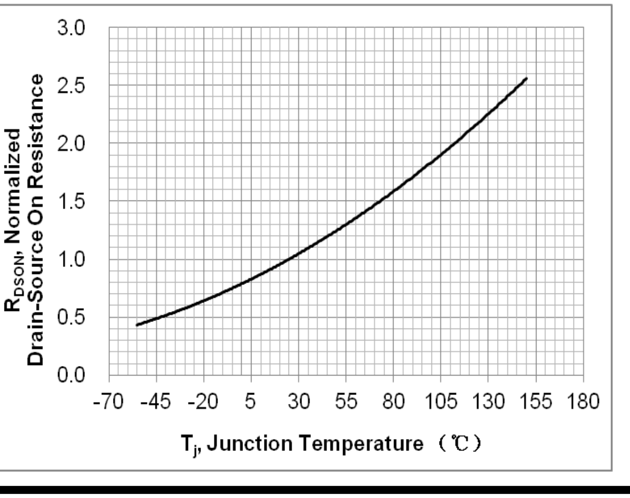


Fig. 7. Gate charge characteristics

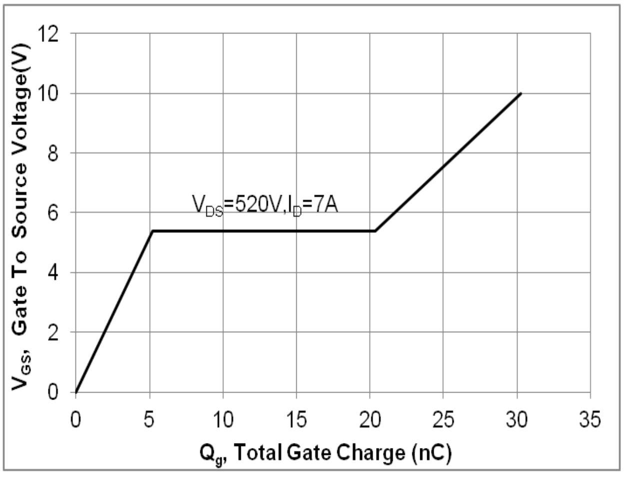


Fig. 8. Capacitance Characteristics

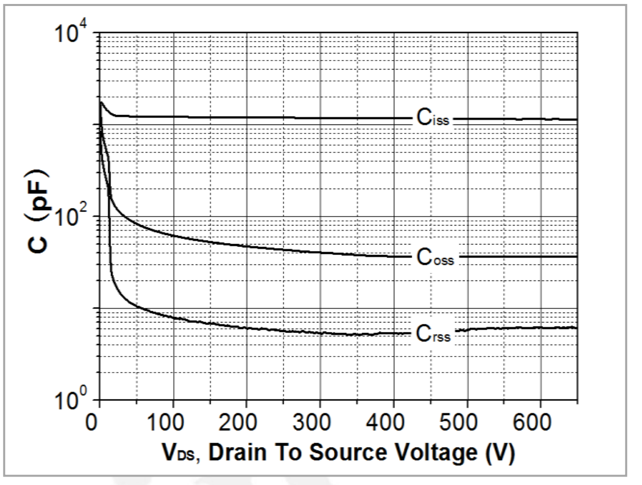


Fig. 9. Maximum safe operating area(TO-220)

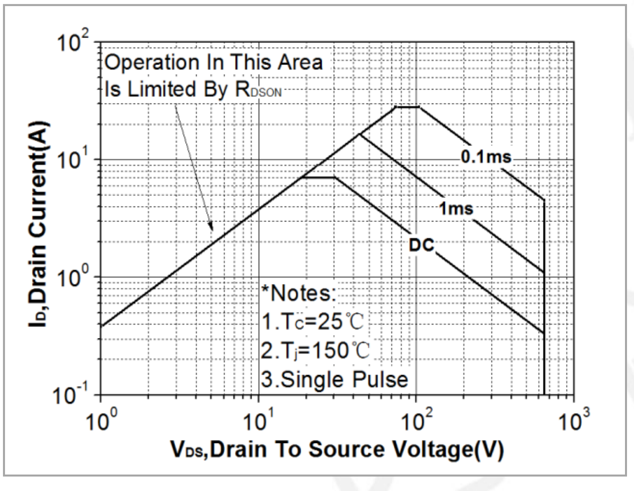


Fig. 10. Maximum safe operating area (TO-251/TO-251N/TO-251U/TO-252)

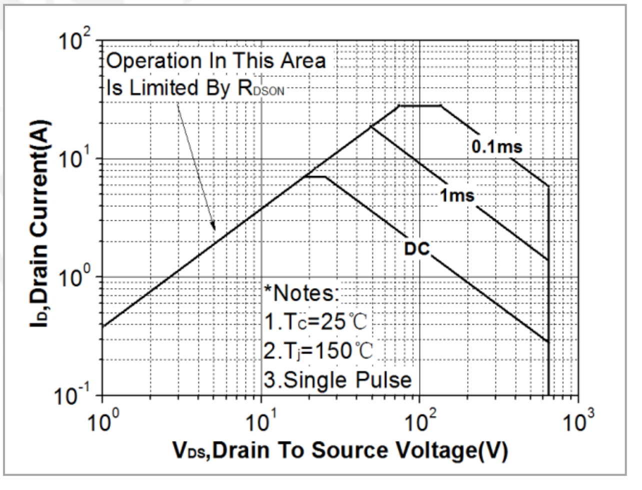


Fig. 11. Maximum safe operating area (TO-220F/TO-220SF/TO-220FT)

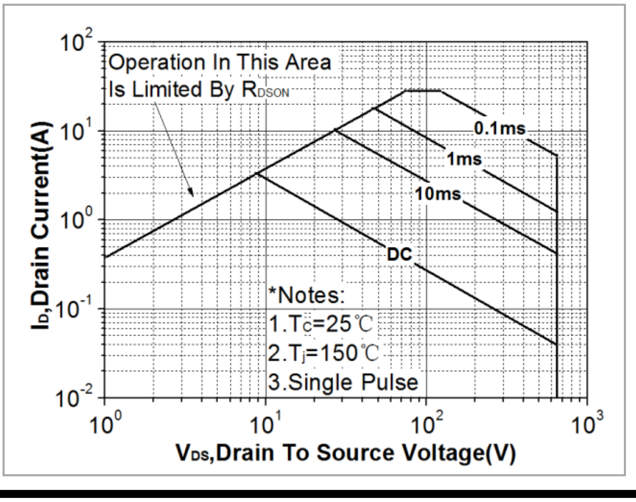


Fig. 12. Maximum safe operating area(TO-262N)

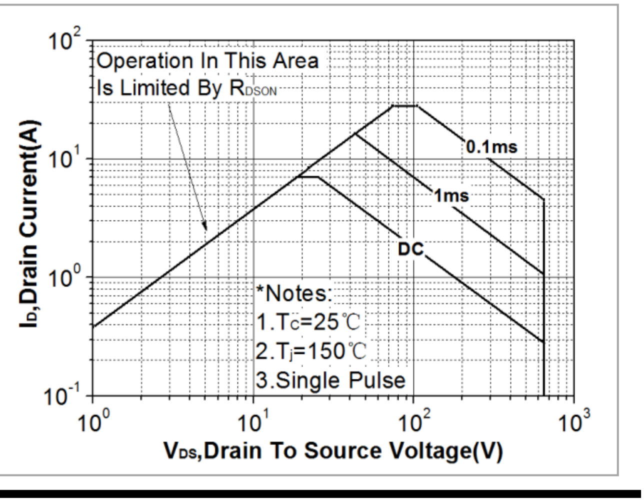


Fig. 13. Maximum safe operating area(DFN5*6)

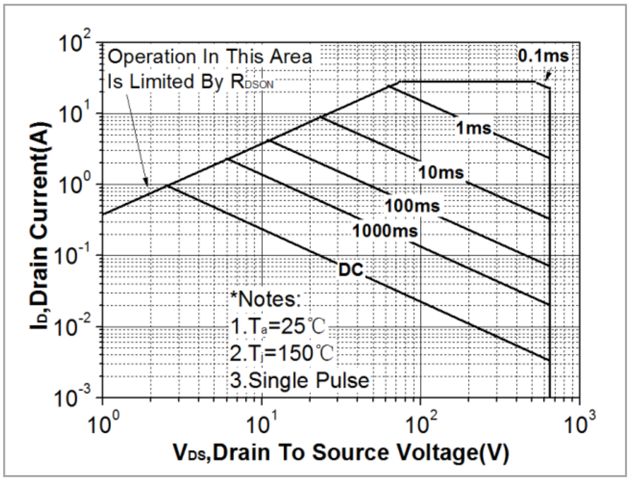


Fig. 14. Transient thermal response curve(TO-220)

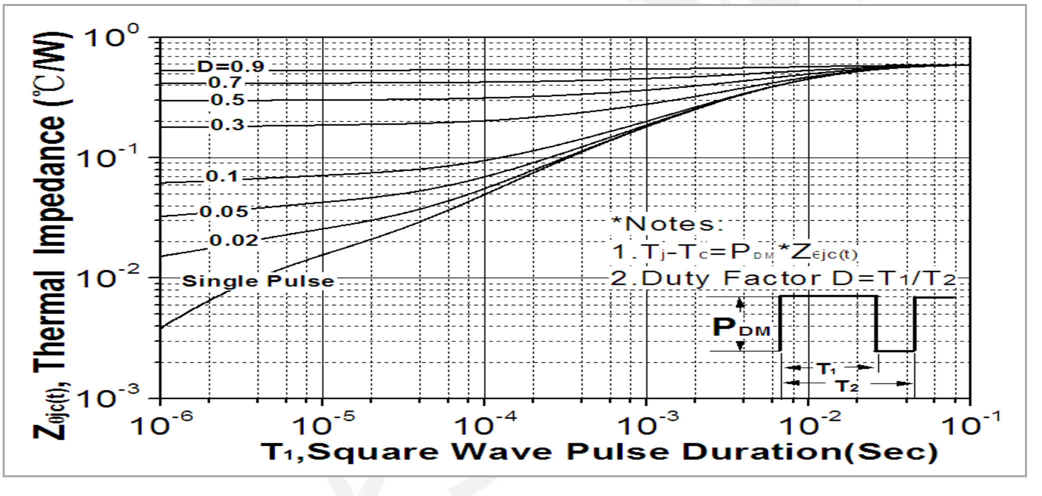


Fig. 15. Transient thermal response curve (TO-251/TO-251N/TO-251U/TO-252)

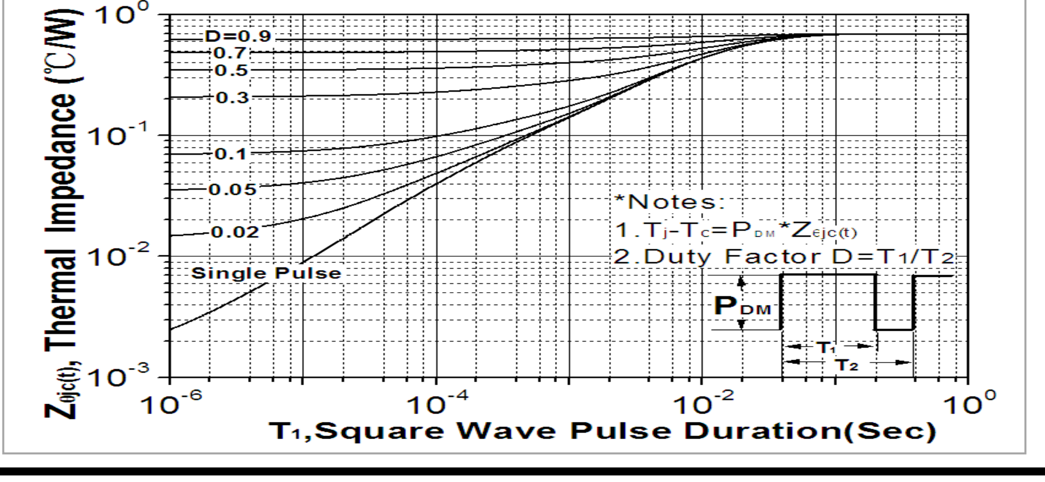


Fig. 16. Transient thermal response curve(TO-220F/TO-220SF/TO-220FT)

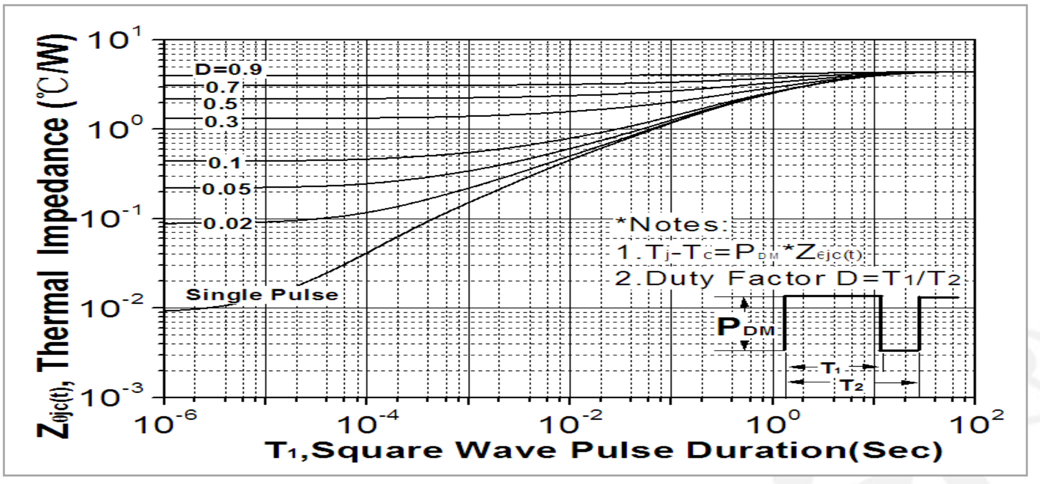


Fig. 17. Transient thermal response curve(TO-262N)

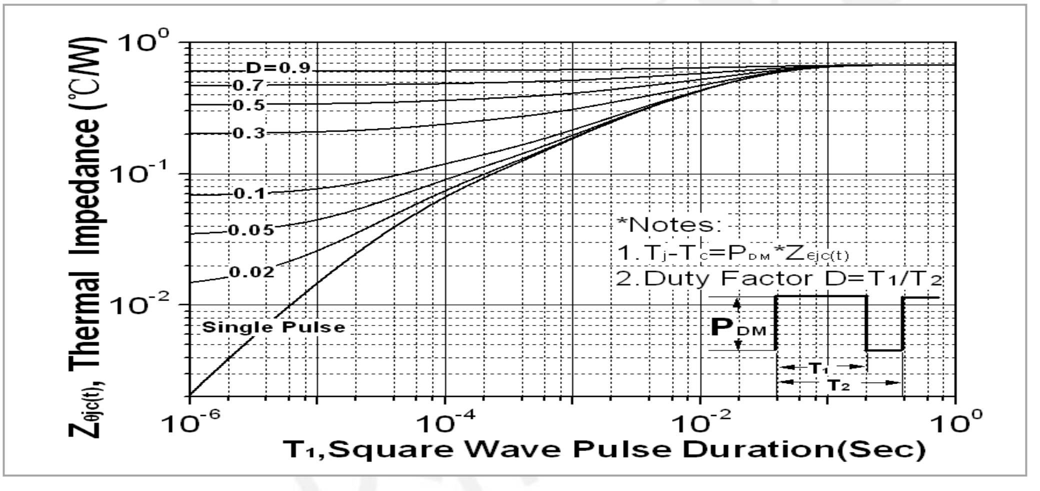


Fig. 18. Transient thermal response curve(DFN5*6)

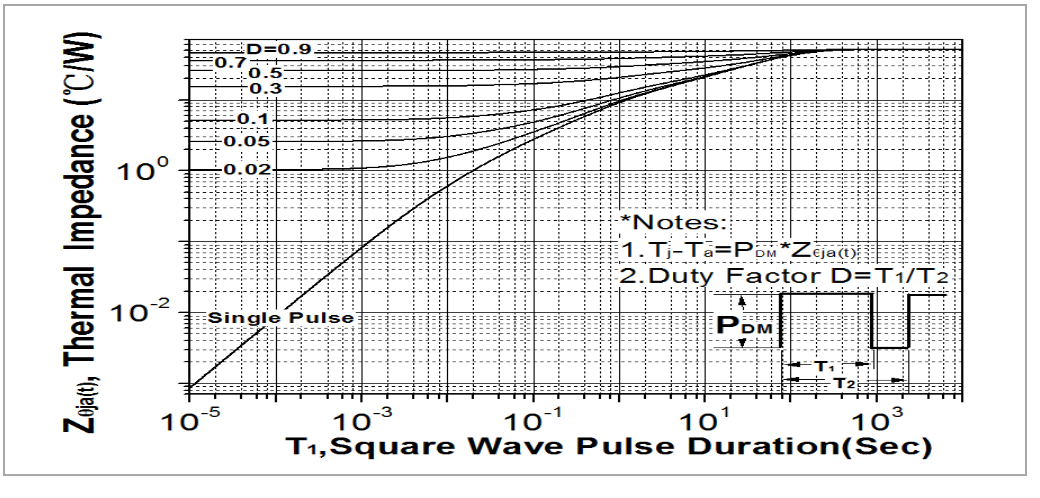


Fig. 19. Gate charge test circuit & waveform

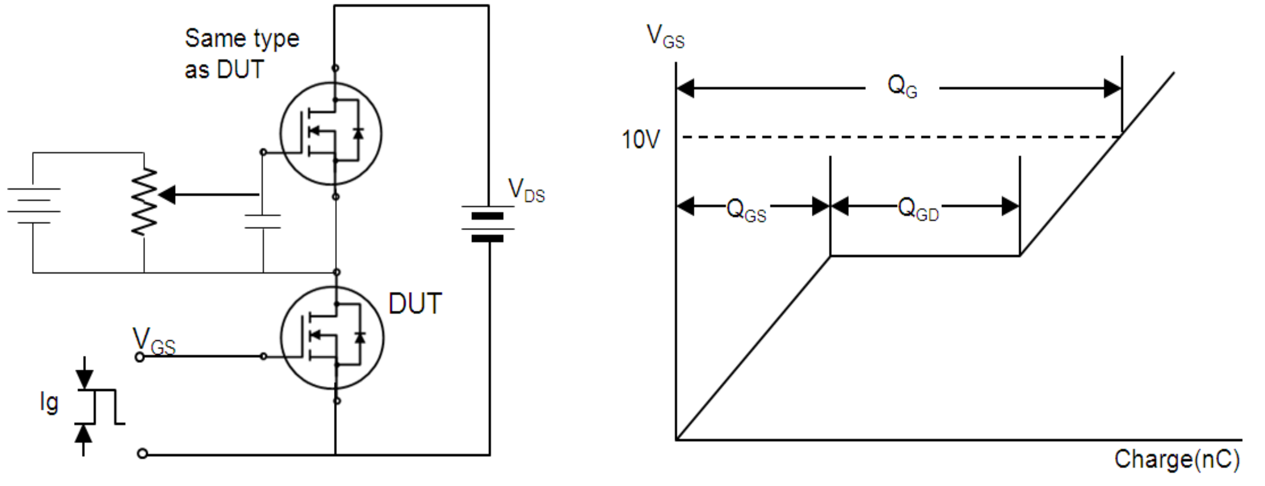


Fig. 20. Switching time test circuit & waveform

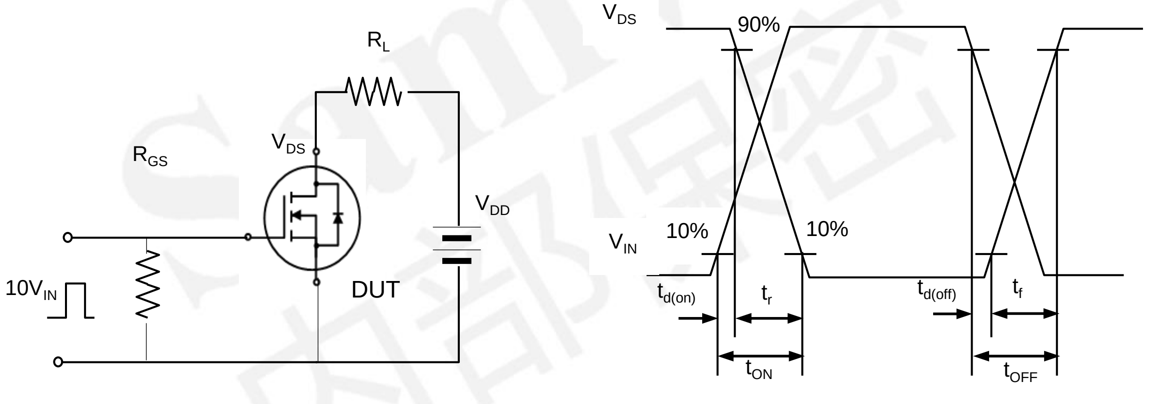


Fig. 21. Unclamped Inductive switching test circuit & waveform

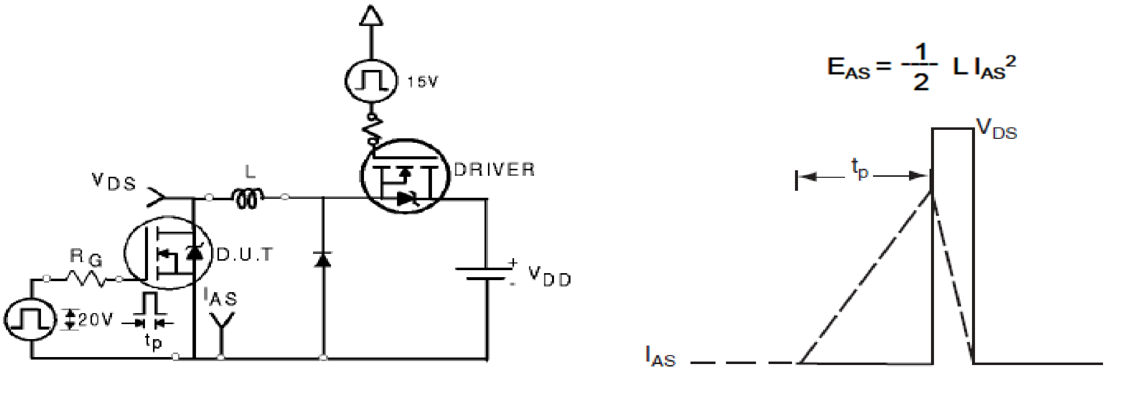
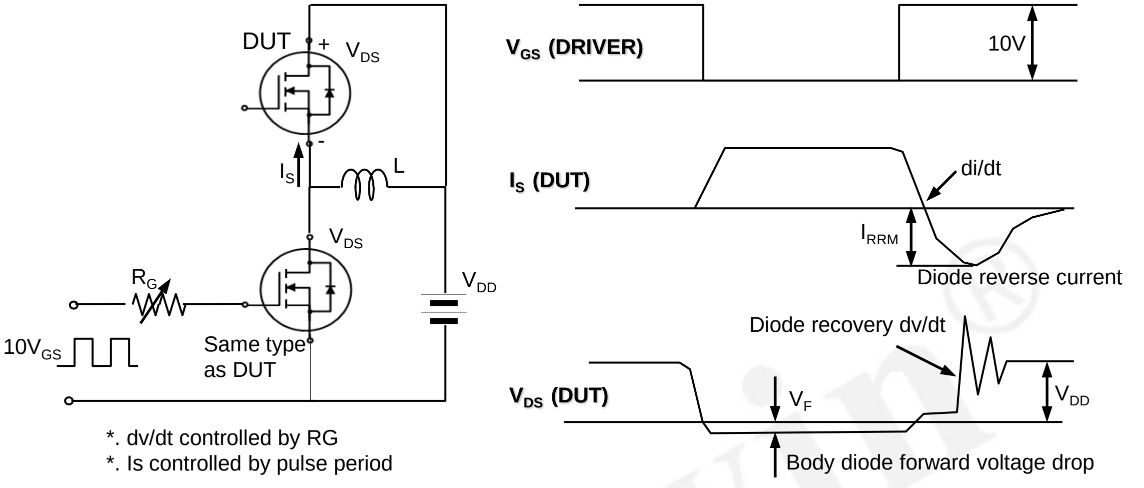


Fig. 22. Peak diode recovery dv/dt test circuit & waveform



DISCLAIMER

* All the data & curve in this document was tested in SEMIPOWER TESTING & APPLICATION CENTER.
* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.
* Qualification standards can also be found on the Web site (**http://www.semipower.com.cn**)
* Suggestions for improvement are appreciated, Please send your suggestions to **samwin@samwinsemi.com**