Qseven

User Manual

µQ7-C72

µQseven® Rel. 2.1 Compliant Module
with NXP i.MX 8M Mini & NXP i.MX 8M Nano
Applications Processors

www.seco.com

REVISION HISTORY

Revision	Date	Note	Rif
1.0	12th February 2021	First Release	AR

Every effort has been made to ensure the accuracy of this manual. However, SECO S.p.A. accepts no responsibility for any inaccuracies, errors or omissions herein. SECO S.p.A. reserves the right to change precise specifications without prior notice to supply the best product possible.

For further information on this module or other SECO products, but also to get the required assistance for any and possible issues, please contact us using the dedicated web form available at http://www.seco.com (registration required).

Our team is ready to assist.

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Chapter 1. INTRODUCTION

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- Information and assistance
- RMA number request
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- Electrostatic Discharges
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1.1 Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/us/support/online-rma.html (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

Warning!
All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

1.2 Information and assistance

What do I have to do if the product is faulty?

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance. A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

  E-mail: technical.service@seco.com

  Fax (+39) 0575 350210
- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

Note: Please have the following information before asking for technical assistance:

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

1.3 RMA number request

To request a RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

A RMA Number will be sent within 1 working day (only for on-line RMA requests).

1.4 Safety

The µQ7-C72 module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

!

Always switch the power off, and unplug the power supply unit, before handling the board and/or connecting cables or other boards.

Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.

If the board has become wet, never connect it to any external power supply unit or battery.

Check carefully that all cables are correctly connected and that they are not damaged.

1.5 Electrostatic Discharges

The µQ7-C72 module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

!

Whenever handling a SM-B69 module, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

1.6 RoHS compliance

The µQ7-C72 module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

1.7 Terminology and definitions

API	Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems
CAN Bus	Controller Area network, a protocol designed for in-vehicle communication
DDC	Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU)
DDR	Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock.
eDP	embedded Display Port, a type of digital video display interface developed especially for internal connections between boards and digital displays
FFC/FPC	Flexible Flat Cable / Flat Panel Cable
GBE	Gigabit Ethernet
Gbps	Gigabits per second
GND	Ground
GPI/O	General purpose Input/Output
I2C Bus	Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability
I2S	Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986
JTAG	Joint Test Action Group, common name of IEEE1149.1 standard for testing printed circuit boards and integrated circuits through the Debug port
DDR4	Double Data Rate Synchronous Dynamic Random Access Memory, 4th generation
LVDS	Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications
Mbps	Megabits per second
MIPI	Mobile Industry Processor Interface alliance
MMC/eMMC	MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip.
N.A.	Not Applicable
N.C.	Not Connected
OpenGL	Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics
OpenVG	Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics
OTG	On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port.
PCI-e	Peripheral Component Interface Express
PHY	Abbreviation of Physical, it is the device implementing the Physical Layer of ISO/OSI-7 model for communication systems

PWM	Pulse Width Modulation
PWR	Power
RGMII	Reduced Gigabit Reduced Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer (PHY)
SD	Secure Digital, a memory card type
SDIO	Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on.
SM Bus	System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices.
SPI	Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line.
TBM	To be measured
TTL	Transistor-transistor Logic
USB	Universal Serial Bus
uSDHC	Ultra Secure Digital Host Controller

1.8 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

Reference	Link
CAN Bus	http://www.bosch-semiconductors.de/en/ubk_semiconductors/safe/ip_modules/can_literature/can_literature.html
eDP	http://www.vesa.org
Gigabit Ethernet	http://standards.ieee.org/about/get/802/802.3.html
I2C	http://www.nxp.com/documents/other/UM10204_v5.pdf
I2S	https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf
LVDS	http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf
MMC/eMMC	http://www.jedec.org/committees/jc-649
NXP i.MX 8M Mini processors	i.MX 8M Mini | Arm Cortex A53 | Cortex M4 | NXP
NXP i.MX 8M Nano processor	i.MX 8M Mini Nano| Arm Cortex A53 | Cortex M7 | NXP
OpenGL	http://www.opengl.org
OpenVG	http://www.khronos.org/openvg
PCI Express	http://www.pcisig.com/specifications/pciexpress
Qseven® Design Guide	https://sget.org/wp-content/uploads/2018/09/Qseven_Design_Guide_2_0.pdf
Qseven® specifications	https://sget.org/wp-content/uploads/2018/09/Qseven-Spec_2.1.pdf
SD Card Association	https://www.sdcard.org/home
SDIO	https://www.sdcard.org/developers/overview/sdio
SM Bus	http://www.smbus.org/specs
USB 2.0 and USB OTG	http://www.usb.org/developers/docs/usb_20_070113.zip

Chapter 2.
OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Block Diagram

2.1 Introduction

The µQ7-C72 is a Q7 Rel. 2.1 compliant module, in µQseven® format, based on embedded NXP i.MX 8M Mini & 8M Nano Applications Processors, featuring ARM® Cortex®-A52 processors, Single-, Dual- or Quad- Core + general purpose Cortex®-M4 processor, with frequencies up to 1.8GHz, which are ideal for applications requiring multimedia capabilities.

The board offers a very high level of integration, both for all most common used peripherals in ARM world and for bus interfaces normally used in x86 world, like PCI-Express.

All this comes out in the extremely reduced space offered by µQseven® boards, which offers all functionalities of standard boards in just 40 x 70mm.

This solution allows combining the advantages of a standard, ready-to-use board, like µQseven® boards are, with all advantages offered by ARM application specific processors like NXP i.MX 8M Mini & 8M Nano, in its different versions (Single Core, Dual Core, Quad Core)

Moreover, NXP i.MX 8M Mini & 8M Nano processors integrate two separated accelerators for Video Processing, Image Processing, 2D and 3D GPUs, giving the processor incredible graphical performances.

The board is completed with up to 4GB DDR4-2400 32-bit bus memory directly soldered on board (up to 2GB DDR4-2400 16-bit bus memory for i.MX 8M Nano), and one eMMC 5.1 Flash Drive, directly accessible like any standard Hard Disk Drive, with up to 64GB of capacity.

The board can support 24 bit Single/Dual Channel LVDS interface, which can be configured to work as two independent 24 bit Single Channel interfaces. As a factory alternative, one eDP interface is available.

HW video decoding of the most common coding standard (i.e., H.265, H.264, VP9, VP8, and others) is supported. Also H.264, VP8 encoding is supported.

Many other features available through the standard Qseven® connector are native for i.MX 8M Mini & 8M Nano processors: 1 x SD/SDIO/MMC interface, 1x PCI-express x1 lane (only with i.MX 8M Mini), 1x CAN interface (optional), I2S Audio interface, 5 x USB 2.0 host Ports (4x USB 2.0 with i.MX 8M Nano), 1xUART interface, SPI interface, 8x GPIOs, SM bus and I2C interface.

RGMII i.MX 8M Mini & 8M Nano native interface is internally carried to a TI DP83867 Ethernet Transceiver, allowing the implementation of a Gigabit Ethernet interface. The networking capabilities of this module are extended by optional WiFi 802.11 a/b/g/n/ac + BT 5.0 NGFF module soldered on-board.

The µQ7-C72 module is part of SECO's "Just! Embedded" product line, which are modules totally designed around the features offered by the SOC only, with very few add-ons. This lead to essential, "ready-to-use" and "ready-to-market" products, which allow the reduction of design risks with minimal effort and cost. This allows also to take the most advantage possible from the pin-multiplexing possibilities offered by the i.MX 8M Mini & 8M Nano processors; indeed, most of the Qseven® standard interfaces, when are not required, can be reprogrammed to offer other functionalities already implemented inside the i.MX 8M Mini & 8M Nano processors itself. Optionally, the module can be equipped with a low-power additional RTC, which would replace in working the i.MX 8M Mini & 8M Nano native RTC (more power consuming).

For external interfacing to standard devices, a carrier board with a 230-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as integration of other peripherals/devices not already included in µQ7-C72 module.

2.2 Technical Specifications

Processors

NXP i.MX 8M Mini Family based on ARM® Cortex®-A53 cores + general purpose Cortex®-M4 400MHz processor:

- i.MX 8M Mini Quad - Full featured, 4x Cortex®-A53 cores, up to 1.8GHz
- i.MX 8M Mini Dual - Full featured, 2x Cortex®-A53 cores, up to 1.8GHz
- i.MX 8M Mini Solo - Full featured, 1x Cortex®-A53 cores, up to 1.8GHz
- i.MX 8M Mini Quad Lite - 4x Cortex®-A53 cores, up to 1.8GHz, no VPU
- i.MX 8M Mini Dual Lite - 2x Cortex®-A53 cores, up to1.8GHz, no VPU
- i.MX 8M Mini Solo Lite - 1x Cortex®-A53 cores, up to 1.8GHz, no VPU

NXP i.MX 8M Nano Family based on ARM® Cortex®-A53 cores + general purpose Cortex®-M7 750MHz processor:

- i.MX 8M Nano Quad - Full featured, 4x Cortex®-A53 cores, up to1.5GHz
- i.MX 8M Nano Dual - Full featured, 2x Cortex®-A53 cores, up to 1.5GHz
- i.MX 8M Nano Solo - Full featured, 1x Cortex®-A53 cores, up to 1.5GHz
- i.MX 8M Nano Quad Lite - 4x Cortex®-A53 cores, up to 1.5GHz, no VPU
- i.MX 8M Nano Dual Lite - 2x Cortex®-A53 cores, up to 1.5GHz, no VPU
- i.MX 8M Nano Solo Lite - 1x Cortex®-A53 cores, up to 1.8GHz, no VPU

Memory

Soldered Down DDR4-2400 memory, 32-bit interface, up to 4GB (i.MX8M Mini)
Soldered Down DDR4-2400 memory, 16-bit interface, up to 2GB (i.MX8M Nano)

Graphics

i.MX 8M Mini Family of processors:
Vivante GC320 2D accelerator + GCNanoUltra 3D accelerator
OpenGL ES 2.0, OpenVG 1.1 support
Embedded VPU (not for Lite processors), supporting:

- HW Decoding of VP9, HEVC/H.265, AVC/H.264, VP8
- HW Encoding of AVC/H.264, VP8

i.MX 8M Nano Family of processors:
Vivante GC7000UL 2D/3D GPU
OpenGL ES 3.1, OpenCL1.2, Vulkan support

Video Interfaces

Single/Dual Channel 18/24-bit LVDS interface or eDP interface (factory alternatives)

! *** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated. Please also check paragraph 4.1*

Video Resolution

LVDS, resolution up to 1920x1080 @ 60Hz

Mass Storage

eMMC 5.1 Drive soldered on-board, up to 64GB
SD / MMC / SDIO interface
Optional QSPI Flash for booting

PCI Express

1 x PCI-e x1 (only with i.MX 8M Mini)

Networking

1 x Gigabit Ethernet interface
Optional WiFi 802.11 a/b/g/n/ac + BT 5.0 NGFF module onboard

USB

5x USB 2.0 Host ports (i.MX 8M Mini)
4x USB 2.0 Host ports (i.MX 8M Nano)

Audio

I2S Audio interface

Serial ports

1x 4-wire UART + 1 x Debug UART
Optional CAN interface

Other Interfaces

SPI interface
Watchdog
8x GPIO
SM Bus
I2C interface

Power supply voltage: $+5V_{DC}$ and $+5V_{SB}$

Operating System: Linux (Yocto)

Operating temperature:

Commercial version 0°C ÷ +60°C **.
Industrial version -40°C ÷ +85°C **(limited to -30°C ÷ +85°C with WiFI / BT module on board).

Dimensions: 40 x 70 mm (µQseven, 1.57" x 2.76")

2.3 Electrical Specifications

According to Qseven® specifications, µQ7-C72 board needs to be supplied only with an external +5V_{DC} power supply.

5 Volts standby voltage needs to be supplied for working in ATX mode.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from +5V_RUN power rail.

2.3.1 Power Consumption

µQ7-C72 module, like all Qseven modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which provide also the required voltage to the board, deriving it from its power supply source.

Anyway, it has been possible to measure power consumption directly on VCC power rail (5VDC)that supplies the board.

The power consumption has been measured in three different configurations of µQ7-C72 module, on the industrial temperature range:

- Config 1: i.MX 8M Mini Dual, DDR4 SDRAM 2 GB, eMMC 32GB, LVDS, Wi-Fi / BLE, CAN interface
- Config 2: i.MX 8M Mini Solo, DDR4 SDRAM 1 GB, eMMC 16GB, eDP, CAN interface
- Config 3: i.MX 8M Mini Quad, DDR4 SDRAM 4 GB, eMMC 64GB, LVDS, Wi-Fi / BLE, CAN interface

Status	Config 1				Config 2				Config 3			
	Average Value		Peak Value		Average Value		Peak Value		Average Value		Peak Value	
Idle	1.99W	0.398A	2.1W	0.42A	2.4W	0.48A	2.43W	0.486A	2.73W	0.546A	2.82W	0.564A
Boot	2.18W	0.463A	3.61W	0.722A	2.18W	0.44A	3.12W	0.624A	2.4W	0.48A	4.09W	0.82A
Video playback	3.28W	0.659A	3.92W	0.787A	3.33W	0.66A	3.9W	0.78A	3.55W	0.71A	4.36W	0.87A
Stress Test	3.52W	0.705A	4.24W	0.848A	3.58W	0.715A	3.95W	0.791A	4.56W	0.918A	5.02W	1A
Battery Backup (VCC_RTC)	590nA											
Suspend	N.A.											
Soft-Off (VCC_5V_SB)	18mA											

2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VCC: Power Supply +5VDC ±5%

VCC_5V_SB: Standby Power Supply +5VDC ±5%

VCC_RTC: 3V backup cell input. VCC_RTC is connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

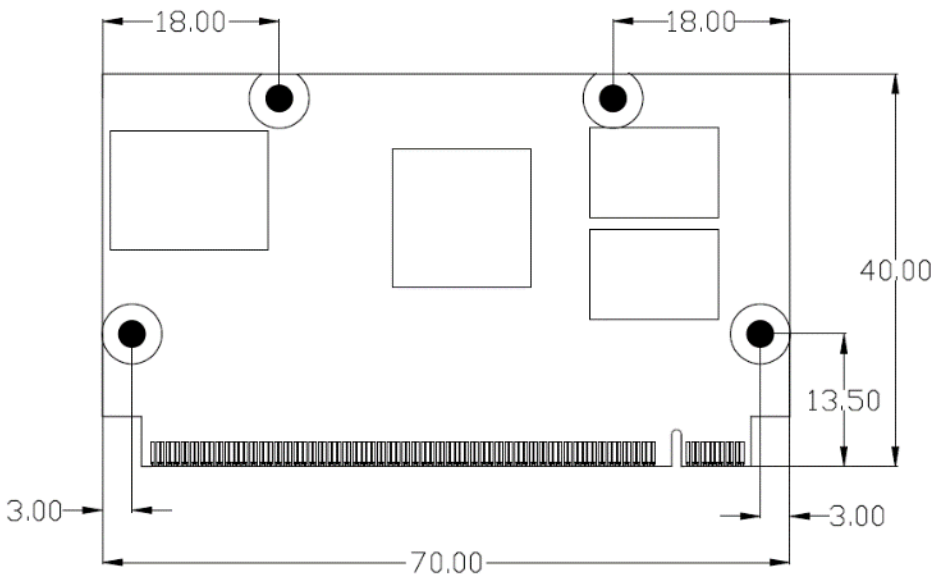
2.4 Mechanical Specifications

According to Qseven® specifications, board dimensions are: 40 x 70 mm (1.57" x 2.76").

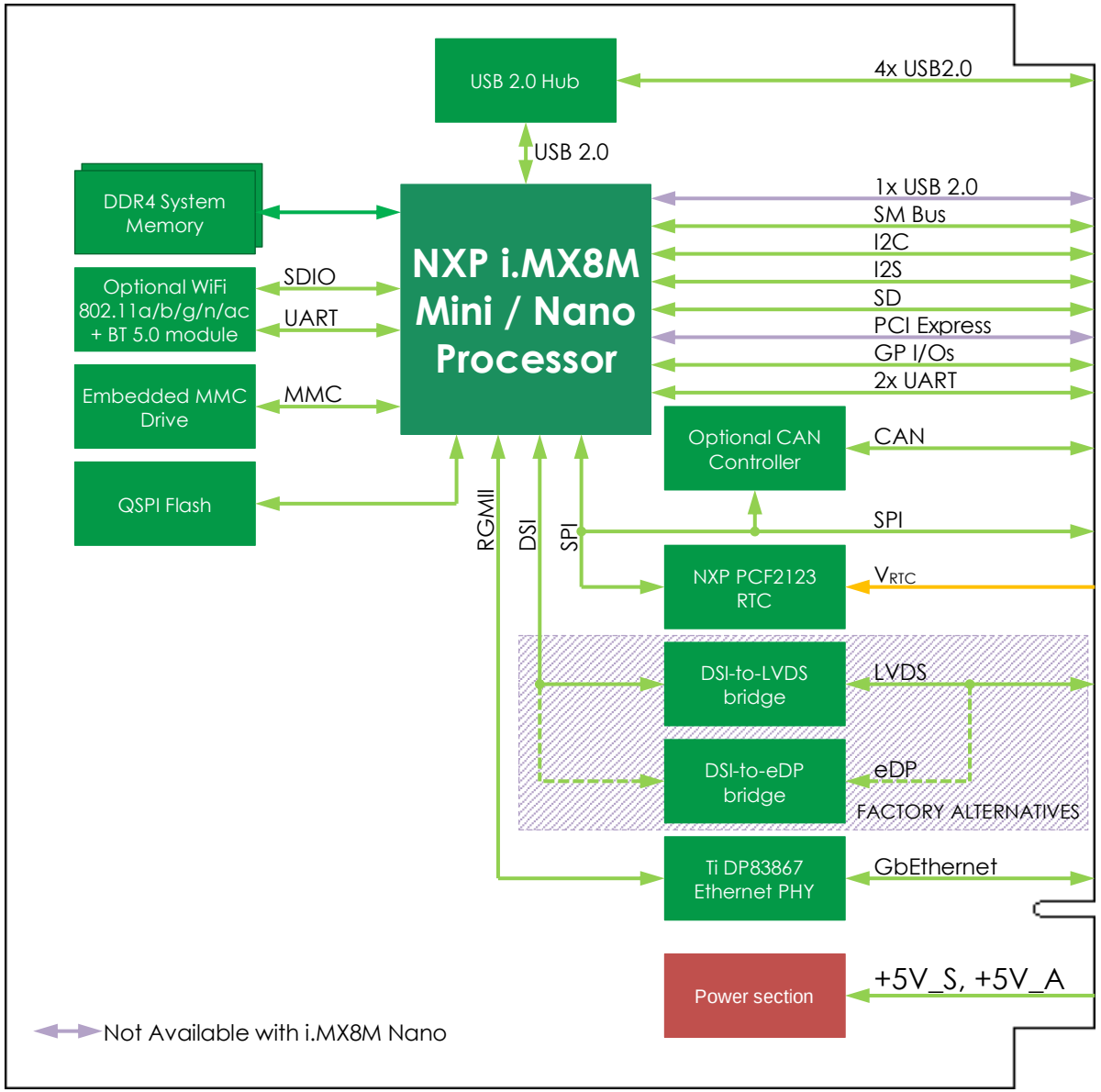
Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs. Qseven® specification suggests two connector heights, 7.8mm and 7.5mm, but it is also possible to use different connector heights, also remaining compliant to the standard.

When using different connector heights, please consider that, according to Qseven® specifications, components placed on bottom side of µQ7-C72 will have a maximum height of 2.2mm ± 0.1. Keep this value in mind when choosing the MXM connector's height, if it is needed to place components on the carrier board in the zone below the Qseven® module.



2.5 Block Diagram



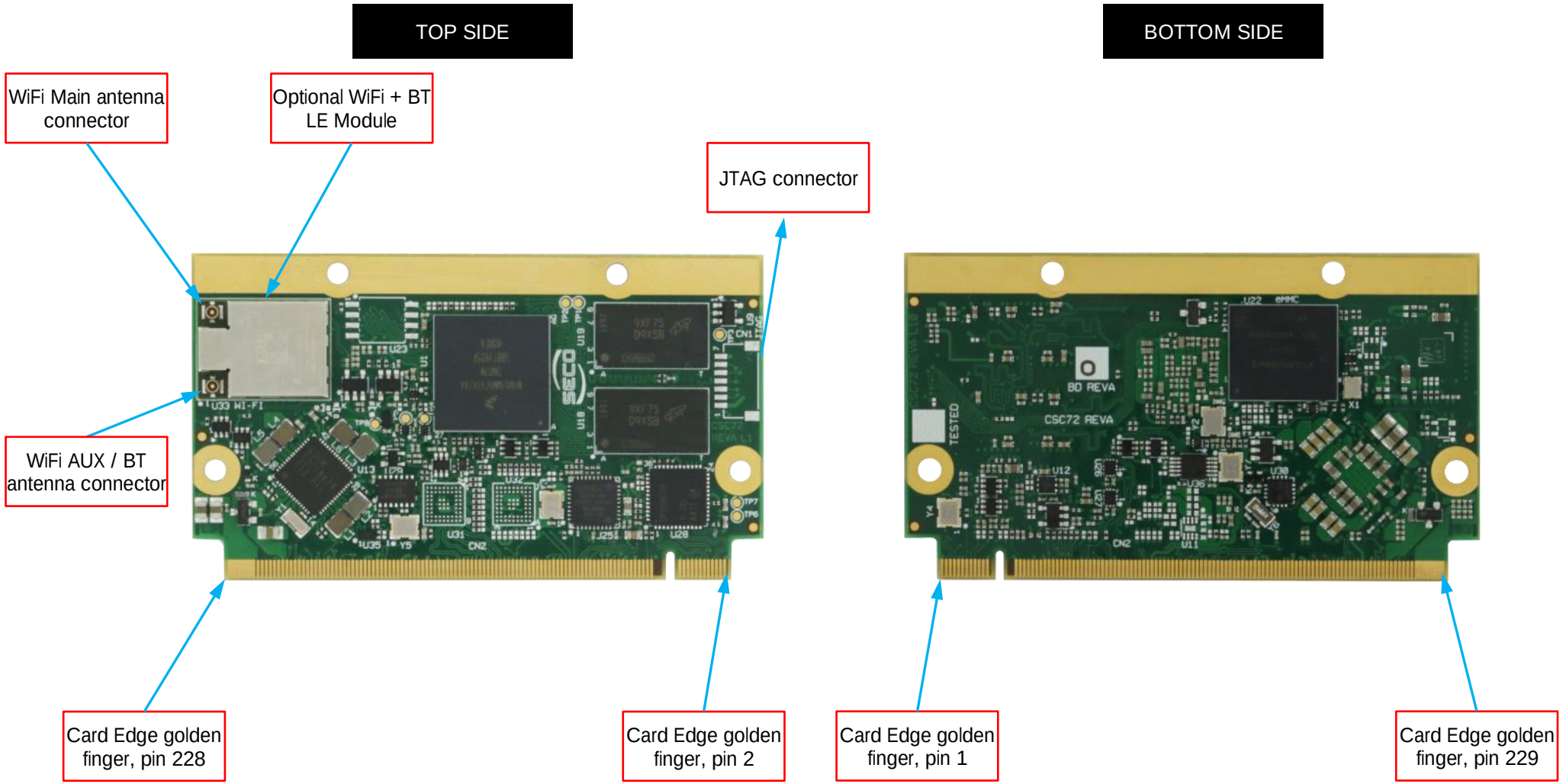
Chapter 3. CONNECTORS

- Introduction
- Connectors description

3.1 Introduction

According to Qseven® specifications, all interfaces to the board are available through a single card edge connector.

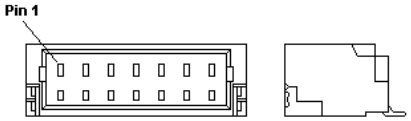
Moreover, two additional RF connectors for antennas on optional WiFi/BT module have been placed.



3.2 Connectors description

3.2.1 JTAG connector

NXP i.MX8 Mini and Nano processors have a system JTAG Controller (SJC) and support two JTAG modes, debug mode and test mode. This interface is accessible through connector CN1, type JST p/n SM07B-SRSS-TB with the following pinout. Please refer to NXP i.MX8 Mini development reference manual for correct implementation.



JTAG Connector- CN1	
1	+3.3V_ALW
2	JTAG_TCK
3	JTAG_TMS
4	JTAG_TDI
5	JTAG_TDO
6	JTAG_RST
7	GND

3.2.2 Qseven® Connector

According to Qseven® specifications, all interface signals are reported on the card edge connector, which is a 230-pin Card Edge that can be inserted into standard 230 pin MXM connectors, as described in Qseven® specifications.

Not all signals contemplated in Qseven® standard are implemented on MXM connector, due to the functionalities really implemented on µQ7-C72 module. Therefore, please refer to the following table for a list of effective signals reported on MXM connector.

Furthermore, many signals available on the card edge connector can be used to implement different functionalities, by exploiting the pin-muxing functionalities offered by NXP i.MX8M Mini and i.MX8M Nano processors.

For accurate signals description, please consult the following paragraphs. In the first instance, the signals with exclusive functionality will be described thoroughly. After them, it will be given a table with a complete list of all pins with all possible alternative functionalities.

NOTE: Even pins are available on top side of CPU board; odd pins are available on bottom side of CPU board. Please refer to board photos.

Qseven® Golden Finger Connector – CN2							
BOTTOM SIDE				TOP SIDE			
SIGNAL GROUP	Type	Pin name	Pin nr.	Pin nr.	Pin name	Type	SIGNAL GROUP
	PWR	GND	1	2	GND	PWR	
GBE	I/O	GBE_MDI3-	3	4	GBE_MDI2-	I/O	GBE
GBE	I/O	GBE_MDI1+	5	6	GBE_MDI2+	I/O	GBE
GBE	O	GBE_LINK100#	7	8	GBE_LINK1000#	I/O	GBE
GBE	I/O	GBE_MDI1-	9	10	GBE_MDI0-	I/O	GBE
GBE	I/O	GBE_MDI1+	11	12	GBE_MDI0+	I/O	GBE
GBE	O	GBE_LINK#	13	14	GBE_ACT#	O	GBE
	REF	GBE_CTREF	15	16	SUS_S5#	O	PWR_MGMT
PWR_MGMT	I	WAKE#	17	18	SUS_S3#	O	PWR_MGMT
	N.A.	N.C.	19	20	PWRBTN#	I	PWR_MGMT
	N.A.	N.C.	21	22	N.C.	N.A.	
	PWR	GND	23	24	GND	PWR	
	PWR	GND	25	26	PWGIN	I	PWR_MGMT
Muxed functionalities	I	BATLOW#	27	28	RSTBTN#	I	PWR_MGMT
	N.A.	N.C.	29	30	N.C.	N.A.	

	N.A.	N.C.	31	32	N.C.	N.A.	
	N.A.	N.C.	33	34	GND	PWR	
	N.A.	N.C.	35	36	N.C.	N.A.	
	N.A.	N.C.	37	38	N.C.	N.A.	
	PWR	GND	39	40	GND	PWR	
MISC	I	BOOT_ALT#	41	42	SDIO_CLK	O	SDIO
SDIO	I/O	SDIO_CD#	43	44	N.C.	N.A.	
SDIO	O	SDIO_CMD	45	46	SDIO_WP	I/O	SDIO
SDIO	O	SDIO_PWR#	47	48	SDIO_DAT1	I/O	SDIO
SDIO	I/O	SDIO_DAT0	49	50	SDIO_DAT3	I/O	SDIO
SDIO	I/O	SDIO_DAT2	51	52	N.C.	N.A.	
	N.A.	N.C.	53	54	N.C.	N.A.	
	N.A.	N.C.	55	56	USB_OTG_PEN	O	USB
	PWR	GND	57	58	GND	PWR	
AUDIO	O	I2S_WS	59	60	SMB_CLK	I/O	MISC
AUDIO	O	I2S_RST#	61	62	SMB_DAT	I/O	MISC
AUDIO	O	I2S_CLK	63	64	SMB_ALERT#	I/O	MISC
AUDIO	I	I2S_SDI	65	66	GP0_I2C_CLK	I/O	MISC
AUDIO	O	I2S_SDO	67	68	GP0_I2C_DAT	I/O	MISC
	N.A.	N.C.	69	70	WDTRIG#	I	MISC
MISC	O	THRMTRIP#	71	72	WDOUT	O	MISC
	PWR	GND	73	74	GND	PWR	
	N.A.	N.C.	75	76	N.C.	N.A.	
	N.A.	N.C.	77	78	N.C.	N.A.	
	N.A.	N.C.	79	80	N.C.	N.A.	
	N.A.	N.C.	81	82	USB_P4-	I/O	USB
	N.A.	N.C.	83	84	USB_P4+	I/O	USB
	N.A.	N.C.	85	86	N.C.	N.A.	
USB	I/O	USB_P3-	87	88	USB_P2-	I/O	USB
USB	I/O	USB_P3+	89	90	USB_P2+	I/O	USB

USB	I	USB_VBUS	91	92	USB_ID	I	USB
USB	I/O	USB_P1-	93	94	USB_P0-	I/O	USB
USB	I/O	USB_P1+	95	96	USB_P0+	I/O	USB
	PWR	GND	97	98	GND	PWR	
eDP/LVDS	O	eDP0_TX0+/LVDS_A0+	99	100	LVDS_B0+	O	LVDS
eDP/LVDS	O	eDP0_TX0-/LVDS_A0-	101	102	LVDS_B0-	O	LVDS
eDP/LVDS	O	eDP0_TX1+/LVDS_A1+	103	104	LVDS_B1+	O	LVDS
eDP/LVDS	O	eDP0_TX1-/LVDS_A1-	105	106	LVDS_B1-	O	LVDS
eDP/LVDS	O	eDP0_TX2+/LVDS_A2+	107	108	LVDS_B2+	O	LVDS
eDP/LVDS	O	eDP0_TX2-/LVDS_A2-	109	110	LVDS_B2-	O	LVDS
eDP/LVDS	O	LVDS_PPEN	111	112	LVDS_BLEN	O	LVDS
eDP/LVDS	O	eDP0_TX3+/LVDS_A3+	113	114	LVDS_B3+	O	LVDS
eDP/LVDS	O	eDP0_TX3-/LVDS_A3-	115	116	LVDS_B3-	O	LVDS
	PWR	GND	117	118	GND	PWR	
eDP/LVDS	O	eDP0_AUX+/LVDS_A_CLK+	119	120	LVDS_B_CLK+	O	LVDS
eDP/LVDS	O	eDP0_AUX-/LVDS_A_CLK-	121	122	LVDS_B_CLK-	O	LVDS
LVDS		LVDS_BLT_CTRL/GP_PWM_OUT0	123	124	N.C.	N.A.	N.C.
	N.A.	N.C.	125	126	eDP_HPD#	I	eDP
	N.A.	N.C.	127	128	N.C.	N.A.	
CAN	O	CAN0_TX	129	130	CAN0_RX	I	CAN
	N.A.	N.C.	131	132	N.C.	N.A.	
	N.A.	N.C.	133	134	N.C.	N.A.	
	PWR	GND	135	136	GND	PWR	
	N.A.	N.C.	137	138	N.C.	N.A.	
	N.A.	N.C.	139	140	N.C.	N.A.	
	PWR	GND	141	142	GND	PWR	
	N.A.	N.C.	143	144	N.C.	N.A.	
	N.A.	N.C.	145	146	N.C.	N.A.	
	PWR	GND	147	148	GND	PWR	
	N.A.	N.C.	149	150	N.C.	N.A.	

	N.A.	N.C.	151	152	N.C.	N.A.	
HDMI	O	HDMI_HPD#	153	154	N.C.	N.A.	
PCI-E	O	PCIE_CLK_REF+	155	156	PCIE_WAKE#	I	PCI-E
PCI-E	O	PCIE_CLK_REF-	157	158	PCIE_RST#	O	PCI-E
	PWR	GND	159	160	GND	PWR	
	N.A.	N.C.	161	162	N.C.	N.A.	
	N.A.	N.C.	163	164	N.C.	N.A.	
	PWR	GND	165	166	GND	PWR	
	N.A.	N.C.	167	168	N.C.	N.A.	
	N.A.	N.C.	169	170	N.C.	N.A.	
UART	O	UART0_TX	171	172	UART0_RTS#	O	UART
	N.A.	N.C.	173	174	N.C.	N.A.	
	N.A.	N.C.	175	176	N.C.	N.A.	
UART	I	UART0_RX	177	178	UART0_CTS#	I	UART
PCI-E	O	PCIE0_TX+	179	180	PCIE0_RX-	I	PCI-E
PCI-E	O	PCIE0_TX-	181	182	PCIE0_RX+	I	PCI-E
	PWR	GND	183	184	GND	PWR	
GPIO	I/O	GPIO0	185	186	GPIO1	I/O	GPIO
GPIO	I/O	GPIO2	187	188	GPIO3	I/O	GPIO
GPIO	I/O	GPIO4	189	190	GPIO5	I/O	GPIO
GPIO	I/O	GPIO6	191	192	GPIO7	I/O	GPIO
	PWR	VCC_RTC	193	194	N.C.	N.A.	
	N.A.	N.C.	195	196	GP_PWM_OUT1	O	MISC
	PWR	GND	197	198	GND	PWR	
SPI	O	SPI_MOSI	199	200	SPI_CS0#	O	SPI
SPI	I	SPI_MISO	201	202	N.C.	N.A.	
SPI	O	SPI_CLK	203	204	MFG_NC4	N.A.	MFG
	PWR	VCC_5V_SB	205	206	VCC_5V_SB	PWR	
	N.A.	N.C.	207	208	MFG_NC2	N.A.	MFG
MFG	N.A.	MFG_NC1	209	210	N.C	N.A.	

N.A.	N.C.	211	212	N.C	N.A.
N.A.	N.C.	213	214	N.C	N.A.
N.A.	N.C.	215	216	N.C	N.A.
N.A.	N.C.	217	218	N.C	N.A.
PWR	VCC	219	220	VCC	PWR
PWR	VCC	221	222	VCC	PWR
PWR	VCC	223	224	VCC	PWR
PWR	VCC	225	226	VCC	PWR
PWR	VCC	227	228	VCC	PWR
PWR	VCC	229	230	VCC	PWR

3.2.3 PCI Express interface signals

The µQ7-C72 module can offer one PCI Express x1 lane, which is directly managed by i.MX8 Mini processor.

Note that this interface is only made available with by i.MX8 Mini family of processors.

PCI express Gen 2.0 (5Gbps) is supported.

Here following the signals involved in PCI express management:

PCIE0_RX+/PCIE0_RX-: PCI Express lane #0, Receiving Input Differential pair

PCIE0_TX+/PCIE0_TX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE_CLK_REF+/PCIE_CLK_REF-: PCI Express Reference Clock, Differential Pair

PCIE_RST#: Reset Signal that is sent from Qseven® Module to any PCI-e device available on the carrier board. It is a +3.3V_RUN active-low signal; it can be used directly to drive externally a single RESET Signal. In case there is the need to supply Reset signal to multiple devices, it is recommended to provide for a buffer on the carrier board.

PCIE_WAKE#: Wake up Signal that is asserted from any PCI-e device available on the carrier board to Qseven® Module. It is a 3V3_RUN active-low signal with a 10kΩ pull-up resistor.

3.2.4 UART interface signals

According to Qseven® Rel. 2.1 specifications, µQ7-C72 offers one UART interface, directly managed by i.MX8 Mini and Nano processor (all versions).

Here following the signals related to UART interface:

UART0_TX: UART Interface, Serial data Transmit (output) line, +3.3V_RUN electrical level.

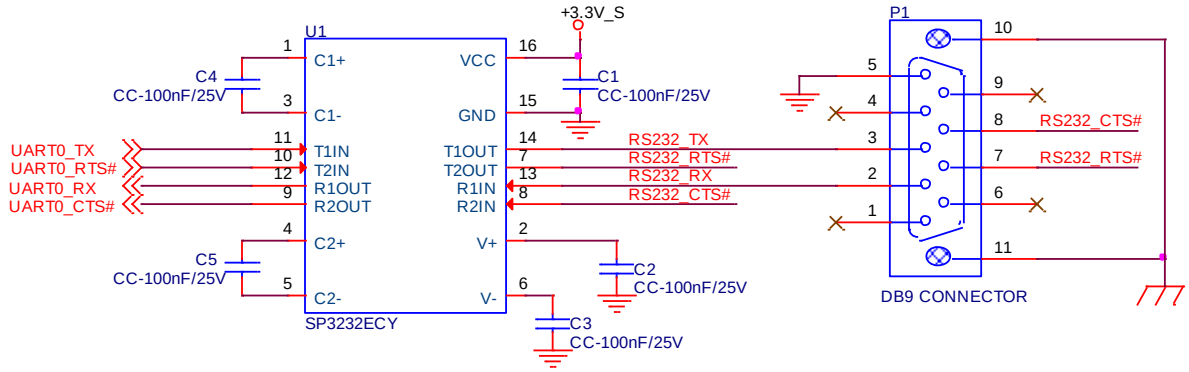
UART0_RX: UART Interface, Serial data Receive (input) line, +3.3V_RUN electrical level.

UART0_RTS#: UART Interface, Handshake signal, Request to Send (output) line, +3.3V_RUN electrical level.

UART0_CTS#: UART Interface, Handshake signal, Clear to Send (Input) line, +3.3V_RUN electrical level.

Please consider that interface is at TTL electrical level; therefore, please evaluate well the typical scenario of application. If it isn't needed explicitly to interface directly at TTL level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

The following schematic shows an example of implementation of RS-232 transceiver for the Carrier board



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All schematics (henceforth also referred to as material) contained in this manual are provided by SECO S.p.A for the sole purpose of supporting the customers' internal development activities.

The schematics are provided "AS IS". SECO makes no representation regarding the suitability of this material for any purpose or activity and disclaims all warranties and conditions with regard to said material, including but not limited to, all expressed or implied warranties and conditions of merchantability, suitability for a specific purpose, title and non-infringement of any third party intellectual property rights.

The customer acknowledges and agrees to the conditions set forth that these schematics are provided only as an example and that he will conduct an independent analysis and exercise judgment in the use of any and all material. SECO declines all and any liability for use of this or any other material in the customers' product design

3.2.5 Gigabit Ethernet signals

The Gigabit Ethernet interface is realised, on µQ7-C72 module by using a Texas Instruments DP83867CRRGZR Gigabit Ethernet transceiver, which is interfaced to NXP i.MX 8M Mini and Nano processors through an RGMII interface.

Here following the signals involved in PCI express management

GBE_MDI0+/GBE_MDI0-: Media Dependent Interface (MDI) I/O differential pair #0

GBE_MDI1+/GBE_MDI1-: Media Dependent Interface (MDI) I/O differential pair #1

GBE_MDI2+/GBE_MDI2-: Media Dependent Interface (MDI) I/O differential pair #2, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

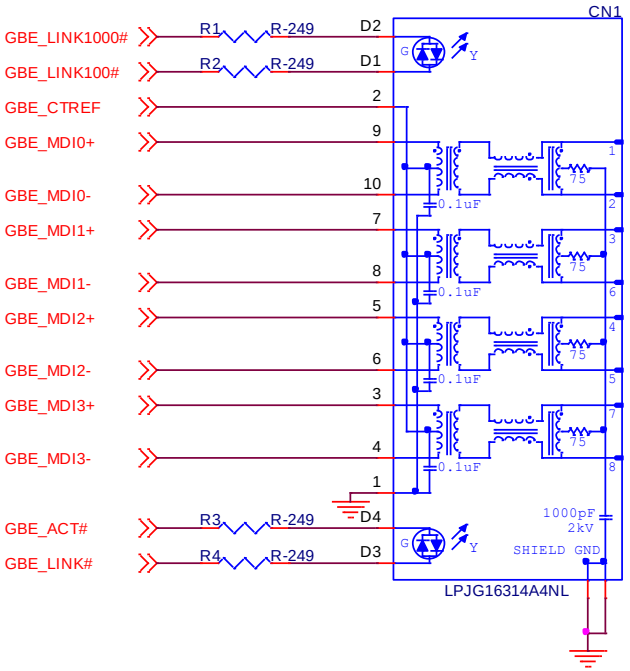
GBE_MDI3+/GBE_MDI3-: Media Dependent Interface (MDI) I/O differential pair #3, only used for 1Gbps Ethernet mode (not for 10/100Mbps modes)

GBE_ACT#: Ethernet controller activity indicator, Active Low Output signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor

GBE_LINK#: Ethernet controller link indicator, Active Low Output signal, electrical level +3.3V_RUN with10kΩ pull-up resistor

GBE_LINK100#: Ethernet controller 100Mbps link indicator, Active Low Output signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor

GBE_LINK1000#: Ethernet controller 1Gbps link indicator, Active Low Output signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor



These signals can be connected, on the Carrier board, directly to an RJ-45 connector, in order to complete the Ethernet interface.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary.

Unused differential pairs and signals can be left unconnected. Please look to the schematic above as an example of implementation of Gigabit Ethernet connector. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. DP83867 PHY, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on Qseven® golden finger connector

3.2.6 USB interface signals

The module µQ7-C72 with NXP i.MX 8M Mini family of processors has up to 5x USB ports consisting of 1x USB 2.0 OTG port from the NXP i.MX 8M Mini processor USB controller, and 4x USB 2.0 host ports coming from a Microchip USB 2514B-AEZC USB 2.0 hub controller.

When configured with NXP i.MX 8M Nano family of processors, µQ7-C72 has only 4x USB 2.0 host ports, and the USB1 OTG port is not available.

Here following the signals related to USB interfaces.

USBP0+/USBP0-: Universal Serial Bus Downstream Port #1 differential pair (coming out from USB 2.0 hub controller).

USBP1+/USBP1-: Universal Serial Bus Port #1 differential pair (coming out from NXP i.MX 8M Mini processors USB 2.0 controller).

USBP2+/USBP2-: Universal Serial Bus Downstream Port #2 differential pair (coming out from USB 2.0 hub controller).

USBP3+/USBP3-: Universal Serial Bus Downstream Port #3 differential pair (coming out from USB 2.0 hub controller).

USBP4+/USBP4-: Universal Serial Bus Downstream Port #4 differential pair (coming out from USB 2.0 hub controller).

USB_ID: USB ID Input This signal must be driven as an open collector signal by external circuitry placed on the carrier board. It must be tied to GND when USB Port #1 has to be set to work in Host mode. When not driven, USB Port#1 will work in Client mode.

USB_VBUS: USB Client Connect Pin, electrical level +5V_ALW. When USB Port #1 is set to work in Client mode, then this signal shall be used to inform the USB controller when an external USB Host is connected (signal High) or disconnected (Signal Low)

USB_OTG_PEN: USB Power enable pin for USB Port 1, electrical level +3.3V_RUN. This pin Enables the Power for the USB-OTG port on the carrier board.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed.

3.2.7 SDIO interface signals

The NXP i.MX 8M Mini and Nano processors include an Ultra Secured Digital Host Controller (uSDHC), providing the interface between the host system and an SD / SDIO/ MMC card interface.

Such an SD controller complies with SD Host Controller Standard Specification version 2.0 / 3.0, with MMC System Specifications version up to 5.1, with the SDIO Card Specifications version 2.0 / 3.0.

The SD port is externally accessible through the golden edge finger connector, and can work in 1-bit and 4-bit mode.

Signals involved with SD interface are the following:

SDIO_PWR#: SD power enable. Active Low Output signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor. This signal can be used on the Carrier board to enable the power line for the SD card.

SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +3.3V_RUN with 100kΩ pull-up resistor. This signal must be externally pulled low to signal that a SD Card Device is present.

SDIO_CLK: Clock Line (output), 50MHz maximum frequency for High Speed Mode.

SDIO_CMD: Command/Response line. Bidirectional signal, electrical level +3.3V_RUN, used to send command from the Host to the connected card, and to send the response from the card to the Host.

SDIO_WP: Write Protect input, electrical level +3.3V_RUN with 100kΩ pull-down resistor. It is used to communicate the status of Write Protect switch of the external SD card. Since microSD cards don't manage this signal, it is important that, when designing carrier boards with microSD slots, this signal must be tied to GND, otherwise the OS will always consider the card as protected from writing.

SDIO_DAT[0÷3]: SD Card data bus. SDIO_DAT0 signal is used for all communication modes. SDIO_DAT[1÷3] signals are required for 4-bit communication mode.

3.2.8 Audio interface signals

µQ7-C72 module supports I2S audio format, thanks to native support offered by the processor to this audio codec standard.

Here following the signals related to AC'97/I2S Audio interface:

I2S_WS: I2S Word Select Signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

I2S_RST#: I2S Codec Reset. Active Low signal Output from the module to the Carrier board, electrical level +3.3V_RUN.

I2S_CLK: I2S Serial Data Clock signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

I2S_SDO: I2S Serial Data Out signal. Output from the module to the Carrier board, electrical level +3.3V_RUN.

I2S_SDI: I2S Serial Data In signal. Input to the module from the Carrier board, electrical level +3.3V_RUN.

All these signals have to be connected, on the Carrier Board, to an I2S Audio Codec. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

3.2.9 LVDS and eDP Flat Panel signals

All processors included in i.MX 8M Mini and Nano family provide a four-lane MIPI display serial interface operating up to a maximum bit rate of 1.5 Gbps. The MIPI-DSI is used to implement a 18/24 bit Single/Dual Channel LVDS or, as a factory alternative, an eDP interface

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for primary channel are LVDS:

LVDS_A0+ / LVDS_A0- : LVDS Channel #A differential data pair #0
LVDS_A1+/ LVDS_A1-: LVDS Channel #A differential data pair #1
LVDS_A2+/LVDS_A2-: LVDS Channel #A differential data pair #2
LVDS_A3+/ LVDS_A3-: LVDS Channel #A differential data pair #3
LVDS_A_CLK+ / LVDS_A_CLK-: LVDS Channel #A differential Clock

OR the signals for primary channel are eDP:

eDP0_TX0+/ eDP0_TX0-: embedded DisplayPort Channel #0 differential data pair #0
eDP0_TX1+/ eDP0_TX1-: embedded DisplayPort Channel #0 differential data pair #1
eDP0_TX2+/ eDP0_TX2-: embedded DisplayPort Channel #0 differential data pair #2
eDP0_TX3+/ eDP0_TX3-: embedded DisplayPort Channel #0 differential data pair #3
eDP0_AUX+/ eDP0_AUX-: embedded DisplayPort Channel #0 auxiliary channel
eDP0_HPD#: eDP channel 0 Hot Plug Detect. Active Low Signal, +3.3V_RUN electrical level input with 100kΩ pull-up resistor.

The signals for secondary channel are LVDS:

LVDS_B0+ / LVDS_B0- : LVDS Channel #B differential data pair #0
LVDS_B1+/ LVDS_B1-: LVDS Channel #B differential data pair #1
LVDS_B2+/LVDS_B2-: LVDS Channel #B differential data pair #2
LVDS_B3+/ LVDS_B3-: LVDS Channel #B differential data pair #3
LVDS_B_CLK+ / LVDS_B_CLK-: LVDS Channel #B differential Clock

In addition, the following control signals are present:

LVDS_PPEN: +3.3V_RUN electrical level Output, Panel Power Enable signal. It can be used to turn On/Off the connected display.

LVDS_BLEN: +3.3V_RUN electrical level Output, Panel Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of connected display.

LVDS_BLT_CTRL: this signal can be used to adjust the panel backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations.

The module has a Texas Instruments SN65DSI84 DSI to FlatLink™ compatible LVDS output bridge, connected from one channel of the four-lane MIPI-DSI of the processor to the LVDS Channel #A and #B interfaces of the edge connector.

As a factory alternative, the module has a Texas Instrument SN65DSI86 MIPI® DSI to eDP™ bridge, connected from one channel of the four-lane MIPI display serial interface to eDP0 interface of the edge connector.

3.2.10 GPIO interface signals

The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

This module provides up to 8xGPIO.

The signals related to GPIO are as follows:

GPIO[0:7]: General Purpose Input/Output, electrical level +3.3V_RUN.

3.2.11 SPI interface signals

The signals related to SPI are as follows:

SPI_CS0#: SPI primary Chip select, active low output signal. Electrical level +3.3V_RUN

SPI_SCK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +3.3V_RUN

SPI_MISO: SPI0 Master Data Input, electrical level +3.3V_RUN. Input to i.MX 8M Mini / Nano from SPI devices embedded on the Carrier Board

SPI_MOSI: SPI0 Master Data Output, electrical level +3.3V_RUN. Output from i.MX 8M Mini / Nano to SPI devices embedded on the Carrier Board

SPI interface can support speed up to 20MHz.

3.2.12 CAN interface signals

The NXP i.MX 8M Mini and Nano processors provide as a factory option a Controller Area Network (CAN) interface through a Microchip MCP2518FD External CAN FD Controller with SPI interface.

The signals related to CAN are as follows:

CAN0_TX: CAN transmitting signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor

CAN0_RX: CAN receiving signal, electrical level +3.3V_RUN with 10kΩ pull-up resistor

Please consider that it is not possible to connect Qseven® CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

3.2.13 Power Management signals

According to Qseven® specifications, on the golden edge finger connector there is a set of signals that are used to manage the power rails and power states.

The signals involved are:

PWGIN: Power Good Input, +5V_RUN tolerant active high signal. It must be driven on the carrier board to signal that power supply section is ready and stable. When this signal is asserted, the module will begin the boot phase. The signal must be kept asserted for all the time that the module is working.

PWRBTN#: Power Button Input, active low, +3.3V_ALW voltage level with 100kΩ pull-up resistor and 100nF filtering capacitor. When working in ATX mode, this signal can be connected to a momentary push-button: a pulse to GND of this signal will switch power supply On or Off.

RSTBTN#: Reset Button Input, active low, +3.3V_ALW voltage signal with 100kΩ pull-up resistor and 100nF filtering capacitor. This signal can be connected to a momentary push-button: a pulse to GND of this signal will reset the Qseven® module.

BATLOW#: Battery Low Input, active low, +3.3V_ALW voltage signal with 10kΩ pull-up resistor. This signal can be driven on the carrier board to signal that the system battery is low, or that some battery-related event has occurred. Can be left unconnected if not used

WAKE#: Wake Input, active low +3.3V_ALW electrical voltage signal with 10kΩ pull-up resistor. This signal can be driven low, on the carrier board, to report that a Wake-up event has occurred, and consequently the module must turn itself on. It can be left unconnected if not used.

SUS_S3#: S3 status output, active low +3.3V_ALW electrical voltage signal. This signal must be used, on the carrier board, to shut off the power supply to all the devices that must become inactive during S3 (Suspend to RAM) power state.

SUS_S5#: S5 status output, active low +3.3V_ALW electrical voltage signal. This signal is used, on the carrier board, to shut off the power supply to all the devices

that must become inactive only during S5 (Soft Off) power state.

3.2.14 Miscellaneous, Thermal Management and Fan control signals

Here following, a list of Qseven® compliant signals that complete the features of µQ7-C72 module.

WDTRIG#: Watchdog Trigger Input. It is an active low signal, +3.3V_ALW voltage. This signal can be used to reset and restart, via Hardware, the internal Watchdog Timer (which is usually managed via Software using µQ7-C72 dedicated API - Application Program Interface - libraries).

WDOUT: Watchdog event indicator Output. It is an active high signal, +3.3V_ALW voltage. When this signal goes high (active), it reports out to the devices on the Carrier board that internal Watchdog's timer expired without being triggered, neither via HW nor via SW.

GP0_I2C_CLK: general purpose I2C Bus clock line. Bidirectional signal, electrical level +3.3V_RUN with a 1kΩ pull-up resistor. It is managed by the SOCs' I2C controller. I2C Bus is able to work in Standard mode (bitrate up to 100Kbps), Fast mode (bitrate up to 400Kbps), Fast-mode Plus (bitrate up to 1Mbps), High-speed mode (bitrate up to 3.4Mbps).

GP0_I2C_DAT: general purpose I2C Bus data line. Bidirectional signal, electrical level +3.3V_RUN with a 1kΩ pull-up resistor. It is managed by the SOCs' I2C controller.

SMB_CLK: SM Bus control clock line for System Management. Bidirectional signal, electrical level +3.3V_RUN with a 1kΩ pull-up resistor

SMB_DAT: SM Bus control data line for System Management. Bidirectional signal, electrical level +3.3V_RUN with a 1kΩ pull-up resistor

SMB_ALERT#: SM Bus Alert line for System Management. Bidirectional signal, active low, electrical level +3.3V_RUN with a 10kΩ pull-up resistor. Any device place on the SM Bus can drive this signal low to signal an event on the bus itself.

THRMTRIP#: Thermal Trip Output. Active Low, +3.3V_RUN voltage signal Thermal Trip indicates an overheating condition of the processor. When goes active, the system immediately transitions to the S5 State (Soft Off).

GP_PWM_OUT1: General purpose PWM output (Open Drain signal).

BOOT_ALT#: Boot Alternate Input. This signal and USB_VBUS (only for i.MX 8M Mini) allow different options for selecting boot device type. See following tables.

i.MX 8M Mini		
BOOT_ALT#	USB_VBUS	Boot device
Tied to GND	Host mode	µSD
Floating/ 3.3V	Host mode	USB1 OTG
Floating/ 3.3V	Client mode	eMMC

i.MX 8M Nano	
BOOT_ALT#	Boot device
Tied to GND	µSD
Floating/ 3.3V	eMMC

3.2.15 Manufacturing signals

According to Qseven® Standard specifications, rel. 2.1, on pin designed as MFG_NCx (208÷209) are carried NXP i.MX 8M Mini / Nano Internal UART2 signals for firmware and boot loader implementations. MFG_NC4 (pin 204) signal is tied to GND through 1kΩ pull-down resistor.

Pin 208 (MFG_NC2) signal	Pin 209 (MFG_NC1) signal
DEBUG_UART_RX	DEBUG_UART_TX

!

The UART interface available on MFG_NCx pins is reserved only for the manufacturing phase; it must not be used by the customer.

It is not possible at all to use these pins to trace the software (for debug purposes)

Chapter 4.
APPENDICES

- Thermal Design

4.1 Thermal Design

A parameter that has to be kept in very high consideration is the thermal design of the system.

Highly integrated modules, like µQ7-C72 module, offer to the user very good performances in minimal spaces, therefore allowing the systems' minimisation. On the counterpart, the miniaturising of IC's and the rise of operative frequencies of processors lead to the generation of a big amount of heat, that must be dissipated to prevent system hang-off or faults.

Qseven® specifications take into account the use of a heatspreader, which will act only as thermal coupling device between the Qseven® module and an external dissipating surface/cooler. The heatspreader also needs to be thermally coupled to all the heat generating surfaces using a thermal gap pad, which will optimise the heat exchange between the module and the heatspreader.

The heatspreader is not intended to be a cooling system by itself, but only as means for transferring heat to another surface/cooler, like heatsinks, fans, heat pipes and so on. Conversely, heatsinks in some situation can represent the cooling solution. Indeed, when using µQ7-C72 module, it is necessary to consider carefully the heat generated by the module in the assembled final system, and the scenario of utilisation.

Until the module is used on a development Carrier board, on free air, just for software development and system tuning, then a finned heatsink could be sufficient for module's cooling. Anyhow, please remember that all depends also on the workload of the processor. Heavy computational tasks will generate much heat with all processor versions. Therefore, it is always necessary that the customer study and develop accurately the cooling solution for his system, by evaluating processor's workload, utilisation scenarios, the enclosures of the system, the air flow and so on. This is particularly needed for industrial grade modules.

SECO can provide µQ7-C72 specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

Ordering Code	Description
QC72-DISS-1	µQ7-C72 Heat Spreader (Passive)
QC72-DISS-2	µQ7-C72 Heat Sink (Passive)

Warning!

The thermal solutions available with SECO boards are tested in the commercial temperature range (0-60°C), without housing and inside climatic chamber. Therefore, the customer is suggested to study, develop and validate the cooling solution for his system, considering ambient temperature, processor's workload, utilisation scenarios, enclosures, air flow and so on.

In particular, the heatspreader is not intended to be a cooling system by itself, but only as the standard means for transferring heat to cooler, like heatsinks, cold plate, heat pipes and so on.

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