Grove - Cape for BeagleBone Series

Release date： 9/20/2015

Version： 1.0

Wiki: http://www.seeedstudio.com/wiki/Grove_Cape_for_BeagleBone_Series

Bazaar: http://www.seeedstudio.com/depot/Grove-Cape-for-BeagleBone-Series-p-1718.html

Document Revision History

Revision	Date	Author	Description
1.0	Sep 21, 2015	Victor.He	Create file

Document Revision History

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Under the supervision of Seeed Technology Inc., this manual has been compiled and published which covered the latest product description and specification. The content of this manual is subject to change without notice.

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1. Introduction

A true open hardware, BeagleBone Series is credit-card-sized Linux computer that connects to the Internet and runs software such as Android 4.0 and Ubuntu. With plenty of I/O and processing power for real-time analysis provided by an AM335x 720MHz ARM® processor, BeagleBone can be complemented with cape plug-in boards to augment functionality.
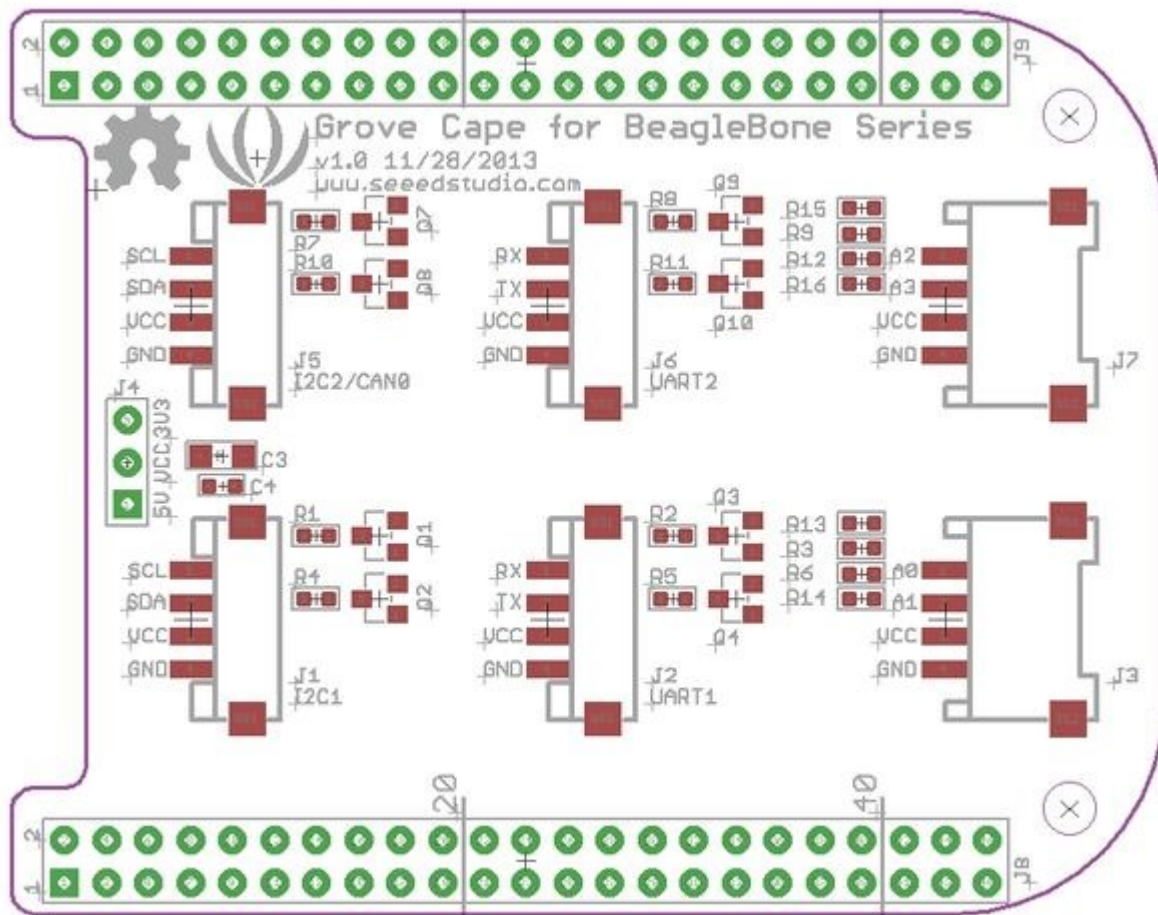
And this Grove - Grove Cape for BeagleBone Series is an expansion board for BeagleBone Series to work with abundant Grove resources. There are 6 ready Grove sockets on the board covering functions like UART, I2C and ADC. And in this way, all Grove Modules are accessible for the BeagleBone board. Want to make some projects with BeagleBone and need some sensors or display? This Grove - Grove Cape for BeagleBone Series can bring you this convenience.

2. Specification

Voltage	3.3~5V
Current	<0.5uA
Dimension	69.9X54.8X17.5 mm
Digital I/o port voltage protection	
Digital allows maximum input voltage	5V
Analog input by partial pressure resistance	Ratio of 1.8/5
Analog port allows maximum input voltage	5V

3. Interface

J1, J5: can be used for I2C.

J2, J6: can be used for UART.

J3, J7: can be used for ADC.

The pins decribe mapping to the Grove Cape for BeagleBone Series board as show below:

Grove Interface	Grove Pin	A/D	I²C	UART	BeagleBone Pin	BeagleBone function
J1	1		SCL1		J8.17	gpio[5]/
J1	2		SDA1		J8.18	gpio[4]/
J5	1		SCL2		J8.19	gpio[13]/
J5	2		SDA2		J8.20	gpio[12]/
J2	1			RX1	J8.26	gpio[14]/
J2	2			TX1	J8.24	gpio[15]/
J6	1			RX2	J8.22	gpio[2]/
J6	2			TX2	J8.21	gpio[3]/
J3	1	AIN0			J8.39	
J3	2	AIN1			J8.40	
J7	1	AIN2			J8.37	
J7	2	AIN3			J8.38	

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