

The documentation and process conversion measures necessary to comply with this document shall be completed by 26 September 2015.

INCH-POUND

MIL-PRF-19500/391P
26 June 2015
SUPERSEDING
MIL-PRF-19500/391N
20 May 2014

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, NPN, SILICON, LOW-POWER, ENCAPSULATED (THROUGH-HOLE AND SURFACE MOUNT), AND UNENCAPSULATED, RADIATION HARDNESS ASSURANCE, DEVICE TYPES 2N3019, 2N3057A, AND 2N3700, QUALITY LEVELS JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for NPN, silicon, low-power transistors. Four levels of product assurance are provided for each device type as specified in [MIL-PRF-19500](#). Two levels of product assurance are provided for the unencapsulated device types 2N3019 and 2N3700. Radiation hardness assurance (RHA) level designators "M", "D", "P", "L", "R", "F", "G" and "H" are appended to the device prefix to identify devices, which have passed RHA requirements.

* 1.2 Package outlines and die topography. The device packages for the encapsulated device types are as follows: TO-5 in accordance with [figure 1](#), TO-39 in accordance with [figure 2](#), TO-18 in accordance with [figure 3](#), and surface mount versions UB in accordance with [figure 4](#). The dimensions and topography for JANHC and JANKC unencapsulated die are as follows: A version die in accordance with [figure 5](#), B version die in accordance with [figure 6](#), and C version die in accordance with [figure 7](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

I_C	V_{CB0}	V_{EBO}	V_{CEO}	T_J and T_{STG}
<u>A dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>°C</u>
1	140	7	80	-65 to +200

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1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$. - Continued.

Types	P_T $T_A = +25^\circ\text{C}$ (1) (2)	P_T $T_C = +25^\circ\text{C}$ (1) (2)	P_T $T_{SP(1S)} = +25^\circ\text{C}$ (1) (2)	$R_{\theta JA}$ (2) (3) (4)	$R_{\theta JC}$ (2) (3)	$R_{\theta JSP(1S)}$ (2) (3)
	$\frac{W}{}$	$\frac{W}{}$	$\frac{W}{}$	$\frac{^\circ\text{C}}{W}$	$\frac{^\circ\text{C}}{W}$	$\frac{^\circ\text{C}}{W}$
2N3019	0.800	5	N/A	195	30	N/A
2N3019S	0.800	5	N/A	195	30	N/A
2N3057A	0.500	1.8	N/A	325	80	N/A
2N3700	0.500	1	N/A	325	150	N/A
2N3700UB	0.500	N/A	1.5	325	N/A	90

(1) For derating, see figures 8, 9, 10, 11, 12, and 13.

(2) See 3.3.

(3) For thermal curves, see figures 14, 15, 16, 17, 18, 19, and 20.

(4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figures 8 and 12 for the UB package and use $R_{\theta JA}$.1.4 Primary electrical characteristics.

Limits	h_{FE1} $V_{CE} = 10\text{ V dc}$ $I_C = 150\text{ mA dc}$	h_{FE2} $V_{CE} = 10\text{ V dc}$ $I_C = 0.1\text{ mA dc}$	h_{FE3} (1) $V_{CE} = 10\text{ V dc}$ $I_C = 10\text{ mA dc}$	h_{FE4} (1) $V_{CE} = 10\text{ V dc}$ $I_C = 500\text{ mA dc}$
Min	100	50	90	50
Max	300	300		300

Types	Limit	h_{FE5} (1) $V_{CE} = 10\text{ V dc}$ $I_C = 1\text{ A dc}$	$ h_{fe} $ $f = 20\text{ MHz}$ $V_{CE} = 10\text{ V dc}$ $I_C = 50\text{ mA dc}$	C_{obo} $100\text{ kHz} \leq f \leq 1\text{ MHz}$ $V_{CB} = 10\text{ V dc}$ $I_E = 0$
2N3019, 2N3019S 2N3057A, 2N3700 2N3700UB	Min Max	15	5 20	μF 12

Types	Limits	$V_{CE(sat)1}$ (1) $I_C = 150\text{ mA dc}$ $I_B = 15\text{ mA dc}$	$V_{CE(sat)2}$ (1) $I_C = 500\text{ mA dc}$ $I_B = 50\text{ mA dc}$	$V_{BE(sat)}$ (1) $I_C = 150\text{ mA dc}$ $I_B = 15\text{ mA dc}$
2N3019, 2N3019S 2N3057A, 2N3700 2N3700UB	Min Max	V_{dc} 0.2	V_{dc} 0.5	V_{dc} 1.1

(1) Pulsed, see 4.5.1.

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.5](#) for PIN construction example and [6.6](#) for a list of available PINs.

* 1.5.1 JAN brand and quality level designators.

1.5.1.1 Encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: JANTX", "JANTXV" and "JANS".

* 1.5.1.2 Unencapsulated devices (die). See [6.7](#) for unencapsulated devices. "JANHC" and "JANKC".

* 1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels applicable for this specification sheet from lowest to highest for JANS quality levels are as follows: "M", "D", "P", "L", "R", "F", "G", and "H". The RHA levels applicable for this specification sheet from lowest to highest for JANTXV quality levels are as follows: "R", "F".

* 1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: 3019, 3019S, 3057A, 3700, AND 3700UB.

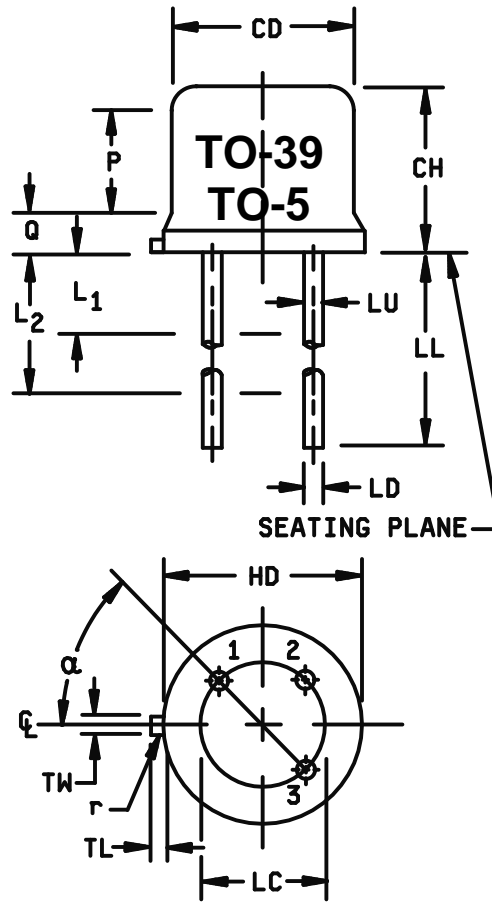
* 1.5.4 Suffix symbols. The following suffix letters are incorporated in the PIN in the order listed in the table as applicable:

	Blank suffix indicates dimension LL is 1.50 min, 1.75 max (2N3019 only)
S	Indicates dimension LL is 0.500 (12.70 mm) minimum, 0.750 (19.05 mm) maximum. (2N3019 only)
UB	Indicates a surface mount (2N3700UB)

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on [QML-19500](#).

* 1.5.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifiers that are applicable for this specification sheet are "A", "B", and "C".

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TP		5.08 TP		6
LD	.016	.021	0.41	0.53	7, 8
LL	.500	.750	12.70	19.05	7, 8, 12
LU	.016	.019	0.41	0.48	7, 8
L ₁		.050		1.27	7, 8
L ₂	.250		6.35		7, 8
Q		.050		1.27	5
TL	.029	.045	0.74	1.14	4
TW	.028	.034	0.71	0.86	3
r		.010		0.25	10
α	45° TP		45° TP		6
P	.100		2.54		

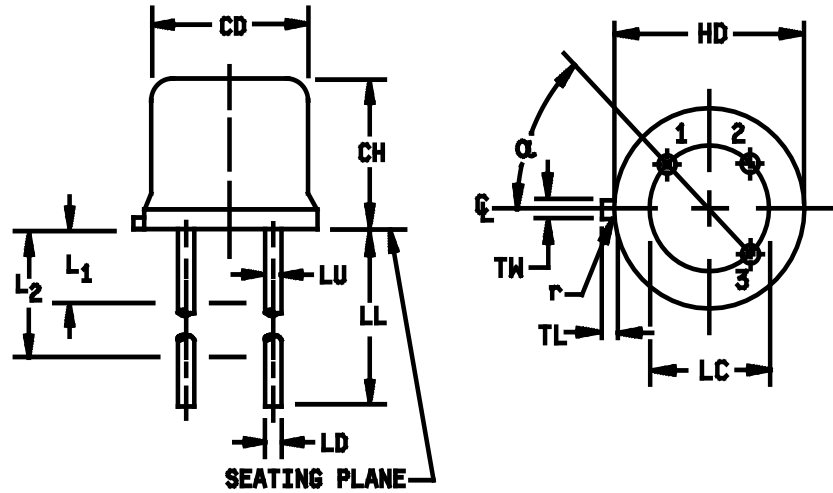


NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
7. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.
12. For "S" suffix devices, dimension LL is 0.500 (12.70 mm) minimum, 0.750 (19.05 mm) maximum.
13. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

*

FIGURE 1. Physical dimensions for device types 2N3019 (TO-5) and 2N3019S (TO-39).



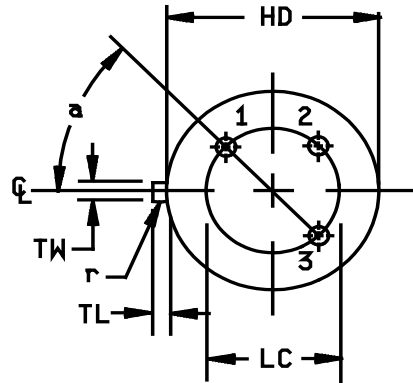
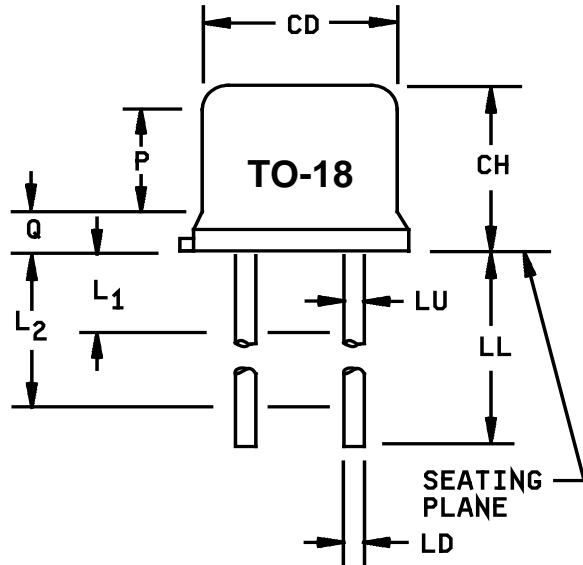
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.065	.085	1.65	2.16	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7
LL	.500	1.750	12.70	44.45	7
LU	.016	.019	0.41	0.48	7
L1		.050		1.27	7
L2	.250		6.35		7
TL	.028	.048	0.71	1.22	3
TW	.036	.046	0.91	1.17	2
r		.007		0.18	10, 11
α	45° TP		45° TP		6

NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
6. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
7. All three leads.
8. The collector shall be internally connected to the case.
9. Dimension r (radius) applies to both inside corners of tab.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.
11. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 2. Physical dimensions for 2N3057A (TO-46).

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L1		.050		1.27	7,8
L2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
α	45° TP		45° TP		6
1, 2, 9, 11, 12					

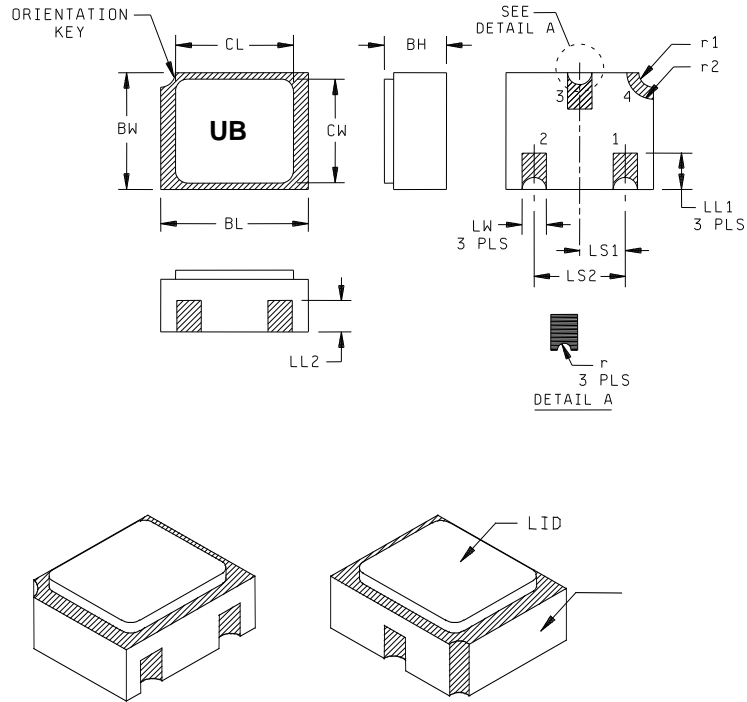


NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TH shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods or by the gauge and gauging procedure shown in figure 2.
7. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 3. Physical dimensions for type 2N3700 (TO-18).

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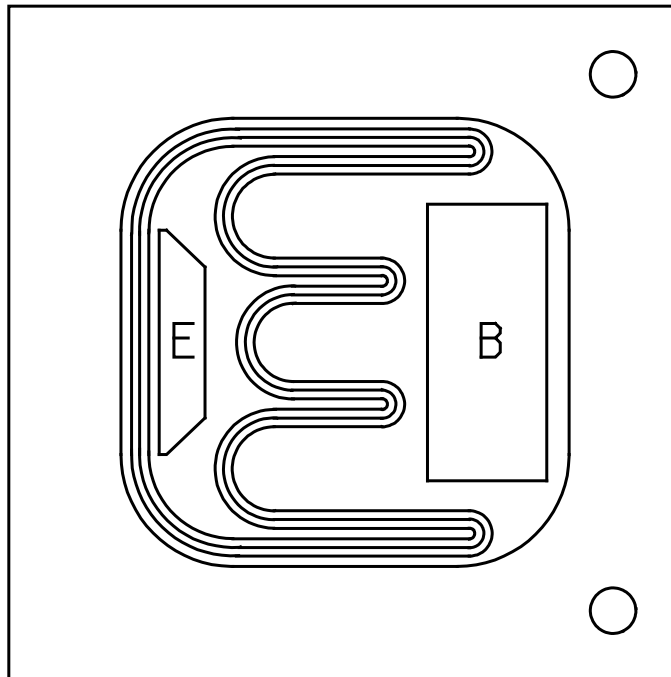


Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	
LS1	.035	.040	0.89	1.02	
LS2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:

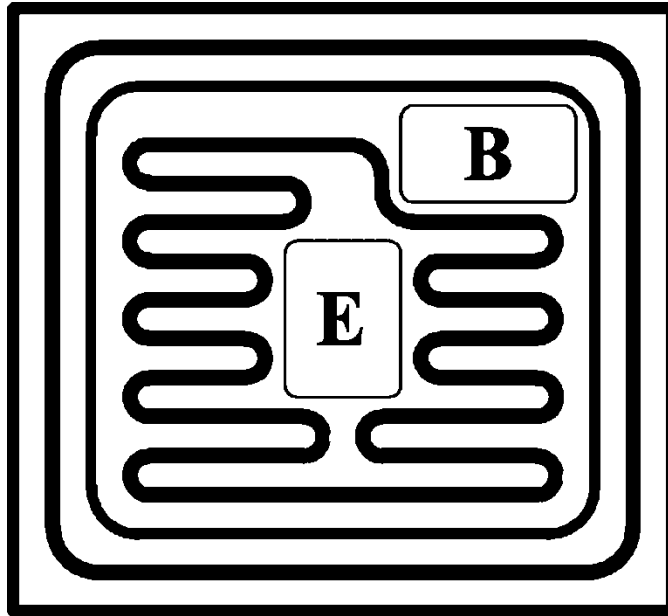
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas.
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 4. Physical dimensions, surface mount (2N3700UB).



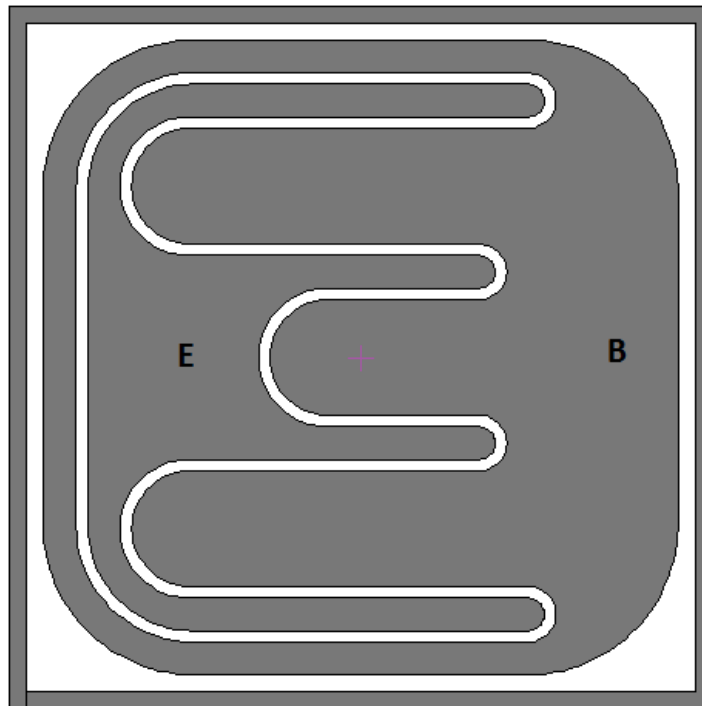
Die size: .030 x .030 inch (0.762 x 0.762 mm).
Die thickness: .008 ±.0016 inch (0.2032 mm ±0.04064 mm).
Base pad: .004 x .010 inch (0.1016 mm x 0.254 mm).
Emitter pad: .0023 x .007 inch (0.05842 mm x 0.1778 mm).
Back metal: Gold, 6,500 ±1,950 Å.
Top metal: Aluminum, 12,000 Å minimum; 14,500 Å nominal.
Back side: Collector.
Glassivation: SiO₂, 7,500 ±1,500 Å.

FIGURE 5. JANHCA and JANKCA die (2N3700 and 2N3019) dimensions.



1. Chip size.....024 x .026 inch \pm .002 inch (0.610 X 0.660 \pm 0.051 millimeter).
2. Chip thickness.....010 inch \pm .0015 inch (0.254 \pm 0.0381 millimeter).
3. Top metal.....Aluminum 15,000Å minimum, 18,000Å nominal.
4. Back metal.....Gold:3,500Å minimum, 5,000Å nominal.
5. Backside.....Collector.
6. Bonding pad.....B = .004 inch x .006 inch (0.102 X 0.152 millimeter).
E = .004 inch x .0055 inch (0.102 X 0.140 millimeter).

FIGURE 6. JANHCB and JANKCB die (2N3700) dimensions.



- | | |
|-------------------|--|
| 1. Chip size | .023 x .023 inch \pm .002 inch (0.584 X 0.584 \pm 0.051 millimeter). |
| 2. Chip thickness | .010 inch \pm .002 inch (0.254 \pm 0.508 millimeter). |
| 3. Top metal | Aluminum 16,000Å minimum, 20,000Å nominal. |
| 4. Back metal | Gold: 5,000Å \pm 500Å. |
| 5. Backside | Collector. |
| 6. Bonding pad | B = .004 inch x .010 inch (0.102 X 0.254 millimeter).
E = .0039 inch x .0039 inch (0.992 X 0.099 millimeter). |

FIGURE 7. JANHCC and JANKCC die (2N3700) dimensions.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

PCB Printed circuit board.
R_{θJA} Thermal resistance junction to ambient.
R_{θJC} Thermal resistance junction to case.
R_{θJSP(IS)} Thermal resistance junction to solder pads (infinite sink mount to PCB).
T_{SP(IS)} Temperature of solder pads (infinite sink mount to PCB).
UB Surface mount case outlines (see [figure 4](#)).

* 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#) (2N3019, TO-5, 2N3019S, TO-39), [figure 2](#) (2N3057A, TO-46), [figure 3](#) (2N3700, TO-18), [figure 4](#) (2N3700UB, surface mount) [figure 5](#) (JANHCA, JANKCA), [figure 6](#) (JANHCB, JANKCB), and [figure 7](#) (JANHCB, JANKCB) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements, PIN designators, and test levels shall be as defined in [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.8 Marking. Marking shall be in accordance with [MIL-PRF-19500](#), except for the UB suffix package. Marking on the UB package shall consist of an abbreviated part number, the date code, and the manufacturers symbol or logo. The prefixes JAN, JANTX, JANTXV, and JANS can be abbreviated as J, JX, JV, and JS respectively. The "2N" prefix can also be omitted. The radiation hardened designator M, D, P, L, R, F, G, or H shall immediately precede (or replace) the device "2N" identifier (depending upon degree of abbreviation required).

* 3.9 Workmanship. Transistors shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [table I](#), [table II](#), and [table III](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with [MIL-PRF-19500](#).

4.3 Screening (JANTX, JANTXV, and JANS only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS	JANTX and JANTXV levels
(1) 3c	Thermal impedance method 3131 of MIL-STD-750. See 4.3.2.	Thermal impedance method 3131 of MIL-STD-750. See 4.3.2.
9	I_{CES1} and h_{FE1} .	Not applicable.
10	48 hours minimum.	48 hours minimum.
11	I_{CES1} ; h_{FE1} ; ΔI_{CES1} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE1} = ± 15 percent.	I_{CES1} and h_{FE1} .
12	See 4.3.1.	See 4.3.1.
13	Subgroups 2 and 3 of table I herein; ΔI_{CES1} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE1} = ± 15 percent.	Subgroup 2 of table I herein; ΔI_{CES1} = 100 percent of initial value or 5 nA dc, whichever is greater; Δh_{FE1} = ± 15 percent.

(1) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 - 30 V dc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum, T_A ambient rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J , and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval. Use method 3100 of MIL-STD-750 to measure T_J .

4.3.2 Thermal impedance measurements. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} (and V_C where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See table III, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIa (JANS) of MIL-PRF-195000 and 4.4.2.1 herein. See 4.4.2.2 herein for JAN, JANTX, and JANTXV group B testing.

4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$V_{CB} = 10$ V dc, 2,000 cycles, adjust device current, or power, to achieve a minimum ΔT_J of $+100^\circ\text{C}$.
B5	1027	NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample. $V_{CB} = 10$ V dc, $P_D \geq 100$ percent of maximum rated P_T (see 1.3). Option 1: 96 hours minimum, sample size in accordance with MIL-PRF-19500, table E-VIa, adjust T_A or P_D to achieve $T_J = +275^\circ\text{C}$ minimum. Option 2: 216 hours minimum, sample size = 45, $c = 0$; adjust T_A or P_D to achieve $T_J = +225^\circ\text{C}$ minimum.
B5	2037	Test condition D.
B6		Not applicable.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1026	Steady-state life: 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3. $n = 45$ devices, $c = 0$. The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life: $T_A = +150^\circ\text{C}$, $V_{CB} = 80$ percent rated voltage, without exceeding max rated V_{CEO} . 48 hours minimum. $n = 45$ devices, $c = 0$.
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See [MIL-PRF-19500](#).
- b. Shall be chosen from an inspection lot that has been submitted to and passed [table I](#), group A, subgroup 2 conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test ([table E-VIa](#), subgroups B4 and B5 for JANS, and [table E-VIc](#), group B for JAN, JANTX and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in [table E-VII](#) of [MIL-PRF-19500](#), and in [4.4.3.1](#) herein (JANS). See [4.4.3.2](#) herein for JAN, JANTX, and JANTXV group C testing.

4.4.3.1 Group C inspection, table E-VII (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; not applicable for UB devices.
C5	3131	See 1.3 . $R_{\theta JC}$ is applicable for all devices except UB. $R_{\theta JA}$ is applicable for UB devices.
C6	1026	1,000 hours, $V_{CB} = 10$ V dc, power and ambient temperature shall be applied to the device to achieve $T_J = +150^\circ\text{C}$ minimum, and minimum power dissipation of 75 percent of max rated P_T (see 1.3 herein); $n = 45$, $c = 0$. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

4.4.3.2 Group C inspection, (JAN, JANTX, and JANTXV), table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; not applicable for UB devices.
C5	3131	See 1.3 , $R_{\theta JC}$ is applicable for all devices except UB. $R_{\theta JA}$ is applicable for UB devices.
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes [table I](#), group A tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS and JANTXV types shall include the group D tests specified in [table II](#) herein. These tests shall be performed as required in accordance with [MIL-PRF-19500](#) and method 1019 of [MIL-STD-750](#) for total ionizing dose, or method 1017 of [MIL-STD-750](#) for neutron fluence as applicable (see [6.2.e](#) herein), except group D, subgroup 2 may be performed separate from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) as specified in [table III](#) herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Collector-base time constant. This parameter may be determined by applying an rf signal voltage of 1.0 volt (rms) across the collector-base terminals, and measuring the ac voltage drop (V_{eb}) with a high-impedance rf voltmeter across the emitter-base terminals. With $f = 79.8$ MHz used for the 1.0 volt signal, the following computation applies:

$$r'_b, C_{c(ps)} = 2 X V_{eb} \text{ (millivolts)}$$

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TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination	2071					
Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles n = 22 devices, c = 0				
Hermetic seal <u>4/</u>	1071	n = 22 devices, c = 0				
Fine leak Gross leak						
Electrical measurements <u>4/</u>		Group A, subgroup 2				
Bond strength <u>3/ 4/</u>	2037	Precondition T _A = +250°C at t = 24 hrs or T _A = +300°C at t = 2 hrs, n = 11 wires, c = 0				
Decap internal visual (design verification) <u>4/</u>	2075	n = 4 devices, c = 0				
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.2	Z _{θJX}			°C/W
Collector to base cutoff current	3036	Bias condition D; V _{CB} = 140 V dc	I _{CB01}		10	μA dc
Emitter to base cutoff current	3061	Bias condition D; V _{EB} = 7 V dc	I _{EBO1}		10	μA dc
Collector to emitter breakdown voltage	3011	Bias condition D; I _C = 30 mA dc pulsed (see 4.5.1)	V _{(BR)CEO}	80		V dc
Collector to emitter cutoff current	3041	Bias condition C; V _{CE} = 90 V dc	I _{CES1}		10	nA dc
Emitter to base cutoff current	3061	Bias condition D; V _{EB} = 5 V dc	I _{EBO2}		10	nA dc
Forward current transfer ratio	3076	V _{CE} = 10 V dc; I _C = 150 mA dc; pulsed (see 4.5.1)	h _{FE1}	100	300	
Forward current transfer ratio	3076	V _{CE} = 10 V dc; I _C = 0.1 mA dc; pulsed (see 4.5.1)	h _{FE2}	50	300	

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/ <u>Subgroup 2</u> - Continued	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Forward current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE3}	90		
Forward current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 500 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE4}	50	300	
Forward current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 1 \text{ A dc};$ pulsed (see 4.5.1)	h_{FE5}	15		
Collector to emitter voltage (saturated)	3071	$I_C = 150 \text{ mA dc}; I_B = 15 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.2	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 500 \text{ mA dc}; I_B = 50 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)2}$		0.5	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 150 \text{ mA dc};$ $I_B = 15 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)}$		1.1	V dc
<u>Subgroup 3</u>						
High-temperature operation		$T_A = +150^\circ\text{C}$				
Collector to emitter cutoff current	3041	Bias condition C; $V_{CE} = 90 \text{ V dc}$	I_{CES2}		5	$\mu\text{A dc}$
Low-temperature operation		$T_A = -55^\circ\text{C}$				
Forward current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc};$ pulsed (see 4.5.1)	h_{FE6}	40		
<u>Subgroup 4</u>						
Small-signal short-circuit forward-current transfer ratio	3206	$V_{CE} = 5 \text{ V dc}; I_C = 1 \text{ mA dc},$ $f = 1 \text{ kHz}$	h_{fe}	80	400	
Magnitude of small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 10 \text{ V dc}; I_C = 50 \text{ mA dc};$ $f = 20 \text{ MHz}$	$ h_{fe} $	5	20	
Input capacitance (output open circuited)	3240	$V_{EB} = 0.5 \text{ V dc}; I_C = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{ibo}		60	pF
Open circuit output capacitance	3236	$V_{CB} = 10 \text{ V dc}; I_E = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}		12	pF
Noise figure	3246	$V_{CE} = 10 \text{ V dc}; I_C = 100 \mu\text{A dc};$ $R_g = 1 \text{ k}\Omega;$ power bandwidth = 200 Hz $f = 1 \text{ kHz}$	NF		4	dB

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> - Continued						
Collector to base time constant		$V_{CB} = 10 \text{ V dc}; I_C = 10 \text{ mA dc};$ $f = 79.8 \text{ MHz}$ (see 4.5.2)	$r'_{b,Cc}$		400	ps
Pulse response		See figure 21	$t_{on} + t_{off}$		30	ns
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = +25^\circ\text{C}; t = 10 \text{ ms}, 1 \text{ cycle}$ (See figure 22)				
<u>Test 1</u>		$V_{CE} = 10 \text{ V dc};$				
2N3019, 2N3019S		$I_C = 500 \text{ mA dc}$				
2N3057A, 2N3700, 2N3700UB		$I_C = 180 \text{ mA dc}$				
<u>Test 2</u>		$V_{CE} = 40 \text{ V dc};$				
2N3019, 2N3019S		$I_C = 130 \text{ mA dc}$				
2N3057A, 2N3700, 2N3700UB		$I_C = 50 \text{ mA dc}$				
<u>Test 3</u>		$V_{CE} = 80 \text{ V dc};$				
2N3019, 2N3019S		$I_C = 60 \text{ mA dc}$				
2N3057A, 2N3700, 2N3700UB		$I_C = 30 \text{ mA dc}$				
Electrical measurements		See table I , subgroup 2 herein				
<u>Subgroups 6 and 7</u>						
Not applicable						

1/ For sampling plan see [MIL-PRF-19500](#).

2/ For resubmission of failed test in subgroup A1, double the sample size of the failed test or sequence of tests. A failure in [table I](#), group A, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for JANS devices.

5/ Not required for laser marked devices.

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TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 4/</u>						
Neutron irradiation	1017	Neutron exposure $V_{CES} = 0$ V				
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 140$ V dc	I_{CBO1}		20	μ A dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 7$ V dc	I_{EBO1}		20	μ A dc
Collector to emitter breakdown voltage	3011	Bias condition D; $I_C = 30$ mA dc pulsed (see 4.5.1)	$V_{(BR)CEO}$	80		V dc
Collector to emitter cutoff current	3041	Bias condition C; $V_{CE} = 90$ V dc	I_{CES1}		20	nA dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 5$ V dc	I_{EBO2}		20	nA dc
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 150$ mA dc	$[h_{FE1}]$ <u>5/</u>	[50]	300	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 0.1$ mA dc	$[h_{FE2}]$ <u>5/</u>	[25]	300	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 10$ mA dc	$[h_{FE3}]$ <u>5/</u>	[45]		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 500$ mA dc	$[h_{FE4}]$ <u>5/</u>	[25]	300	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 1$ A dc	$[h_{FE5}]$ <u>5/</u>	[7.5]		
Collector-emitter saturation voltage	3071	$I_C = 150$ mA dc; $I_B = 15$ mA dc (see 4.5.1)	$V_{CE(sat)1}$.23	V dc
Collector-emitter saturation voltage	3071	$I_C = 500$ mA dc; $I_B = 50$ mA dc (see 4.5.1)	$V_{CE(sat)2}$.58	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 150$ mA dc; $I_B = 15$ mA dc; pulsed (see 4.5.1)	$V_{BE(sat)}$		1.27	V dc

See footnotes at end of table.

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TABLE II. Group D inspection - Continued.

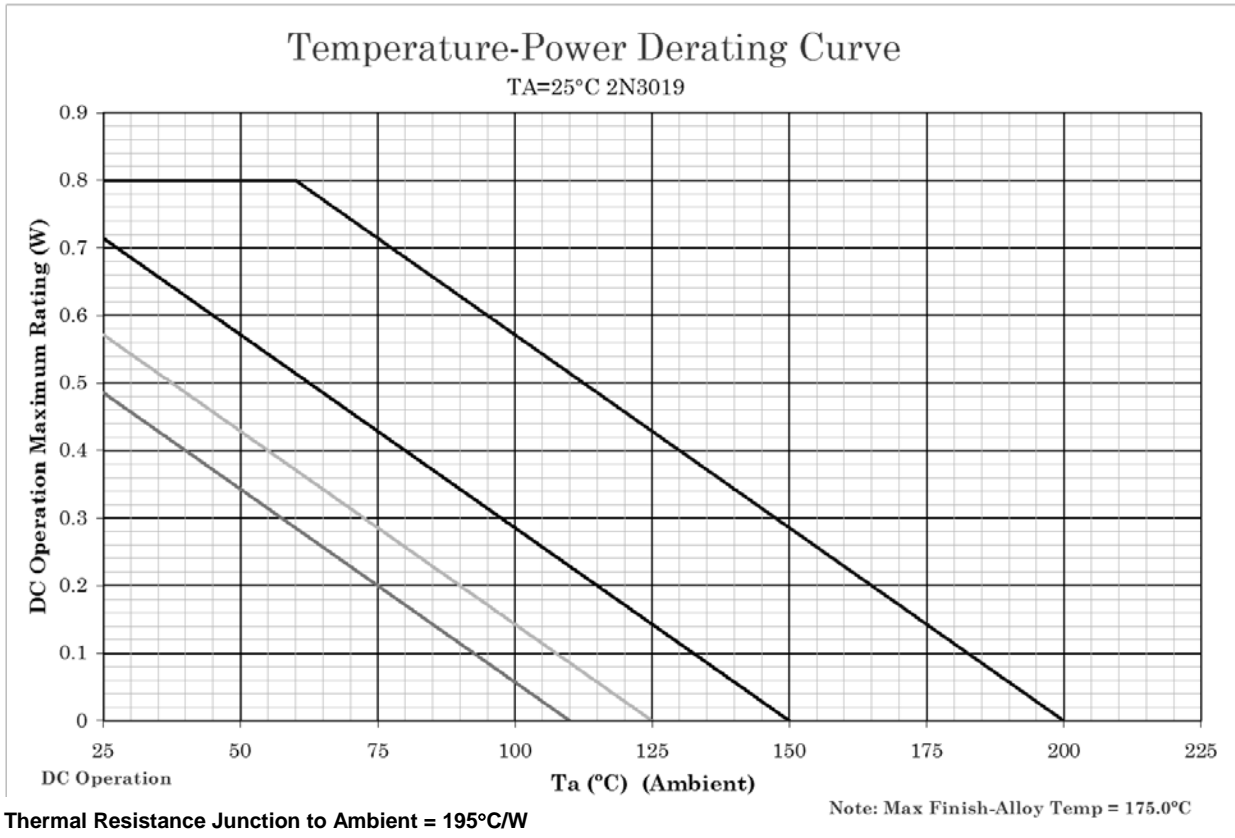
Inspection <u>1/</u> <u>2/</u> <u>3/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u>						
Total dose irradiation	1019	Gamma exposure $V_{CES} = 64$ V				
Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 140$ V dc	I_{CBO1}		20	μ A dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 7$ V dc	I_{EBO1}		20	μ A dc
Collector to emitter breakdown voltage	3011	Bias condition D; $I_C = 30$ mA dc pulsed (see 4.5.1)	$V_{(BR)CEO}$	80		V dc
Collector to emitter cutoff current	3041	Bias condition C; $V_{CE} = 90$ V dc	I_{CES1}		20	nA dc
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 5$ V dc	I_{EBO2}		20	nA dc
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 150$ mA dc	$[h_{FE1}]$ <u>5/</u>	[50]	300	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 0.1$ mA dc	$[h_{FE2}]$ <u>5/</u>	[25]	300	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 10$ mA dc	$[h_{FE3}]$ <u>5/</u>	[45]		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 500$ mA dc	$[h_{FE4}]$ <u>5/</u>	[25]	300	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 1$ A dc	$[h_{FE5}]$ <u>5/</u>	[7.5]		
Collector-emitter saturation voltage	3071	$I_C = 150$ mA dc; $I_B = 15$ mA dc; (see 4.5.1)	$V_{CE(sat)1}$.23	V dc
Collector-emitter saturation voltage	3071	$I_C = 500$ mA dc; $I_B = 50$ mA dc; (see 4.5.1)	$V_{CE(sat)2}$.58	V dc
Base to emitter voltage (saturated)	3066	Test condition A; $I_C = 150$ mA dc; $I_B = 15$ mA dc; pulsed (see 4.5.1)	$V_{BE(sat)}$		1.27	V dc

- 1/ Tests to be performed on all devices receiving radiation exposure.
- 2/ For sampling plan, see MIL-PRF-19500.
- 3/ Electrical characteristics apply to the corresponding UB, suffix versions unless otherwise noted.
- 4/ See 6.2.e herein.
- 5/ See method 1019 of MIL-STD-750 for how to determine $[h_{FE}]$ by first calculating the delta ($1/h_{FE}$) from the pre- and post-radiation h_{FE} . Notice the $[h_{FE}]$ is not the same as h_{FE} and cannot be measured directly. The $[h_{FE}]$ value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

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TABLE III. Group E inspection (all quality levels) - for qualification and re-qualification only.

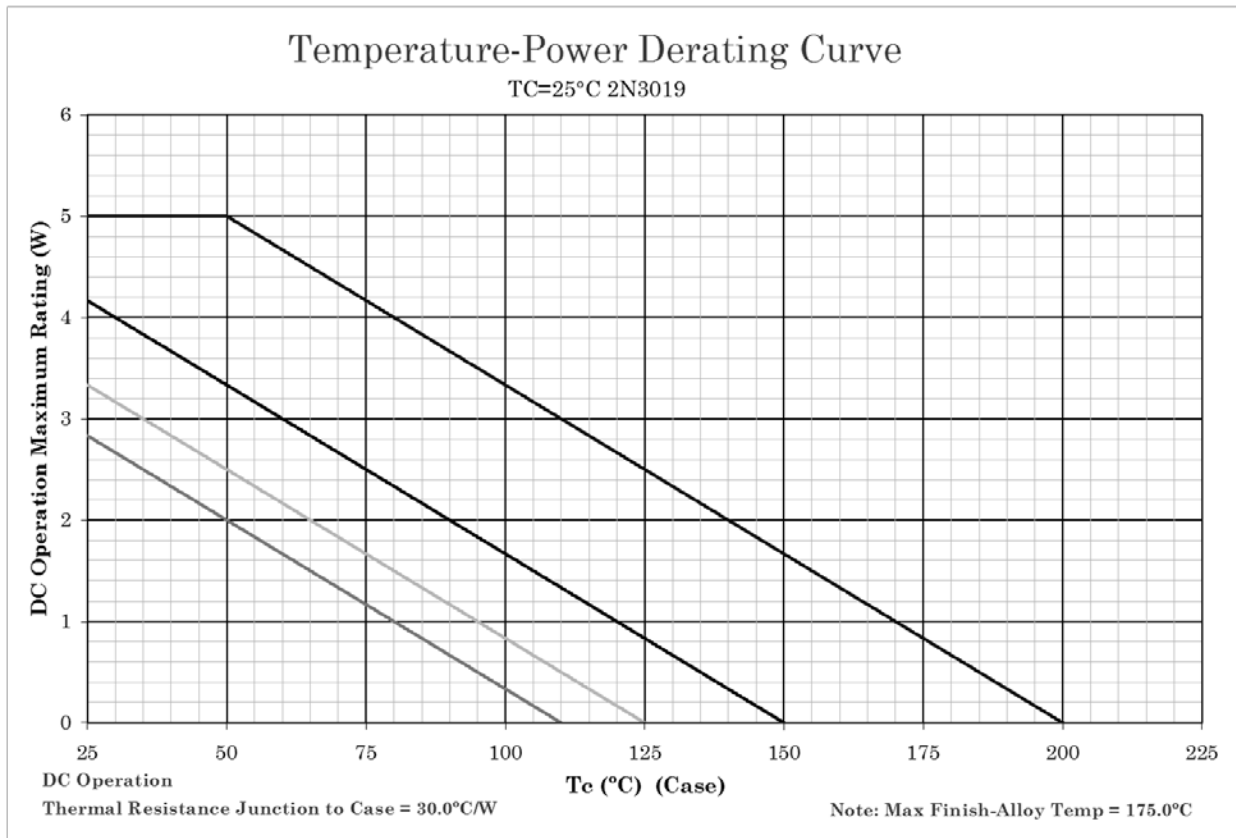
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles.	
Hermetic seal			
Fine leak Gross leak	1071		
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	V _{CB} = 10 V dc, 6,000 cycles.	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroups 4</u>			15 devices, c = 0
Thermal resistance	3131	R _{θJSP(IS)} can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets). R _{θJSP(AM)} need be calculated only.	
Thermal impedance curves		See table E-IX of MIL-PRF-19500 , subgroup 4.	Sample size N/A
<u>Subgroups 5</u>			
Not applicable			
* <u>Subgroup 6</u>			11 devices c = 0
ESD	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

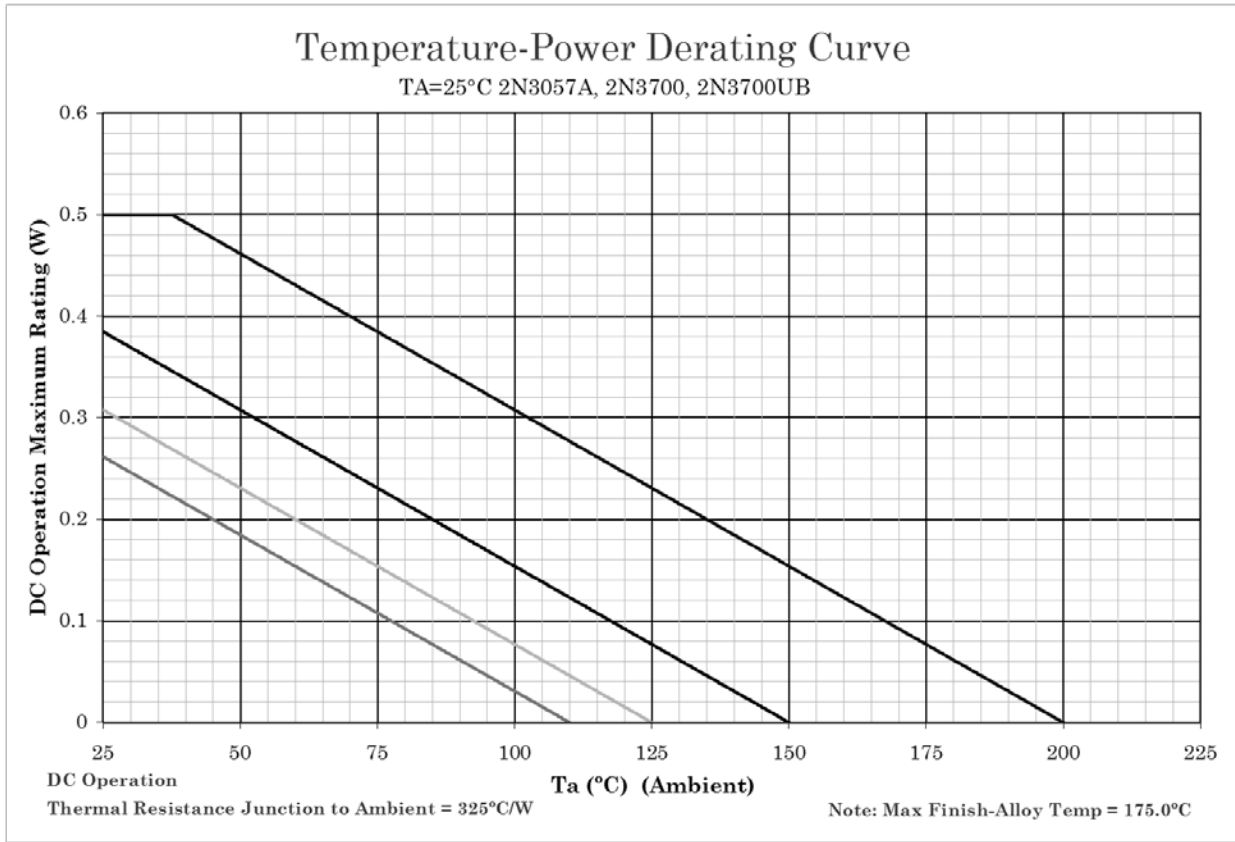
FIGURE 8. Derating for 2N3019 ($R_{\theta JA}$) PCB (TO-5 and TO-39).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

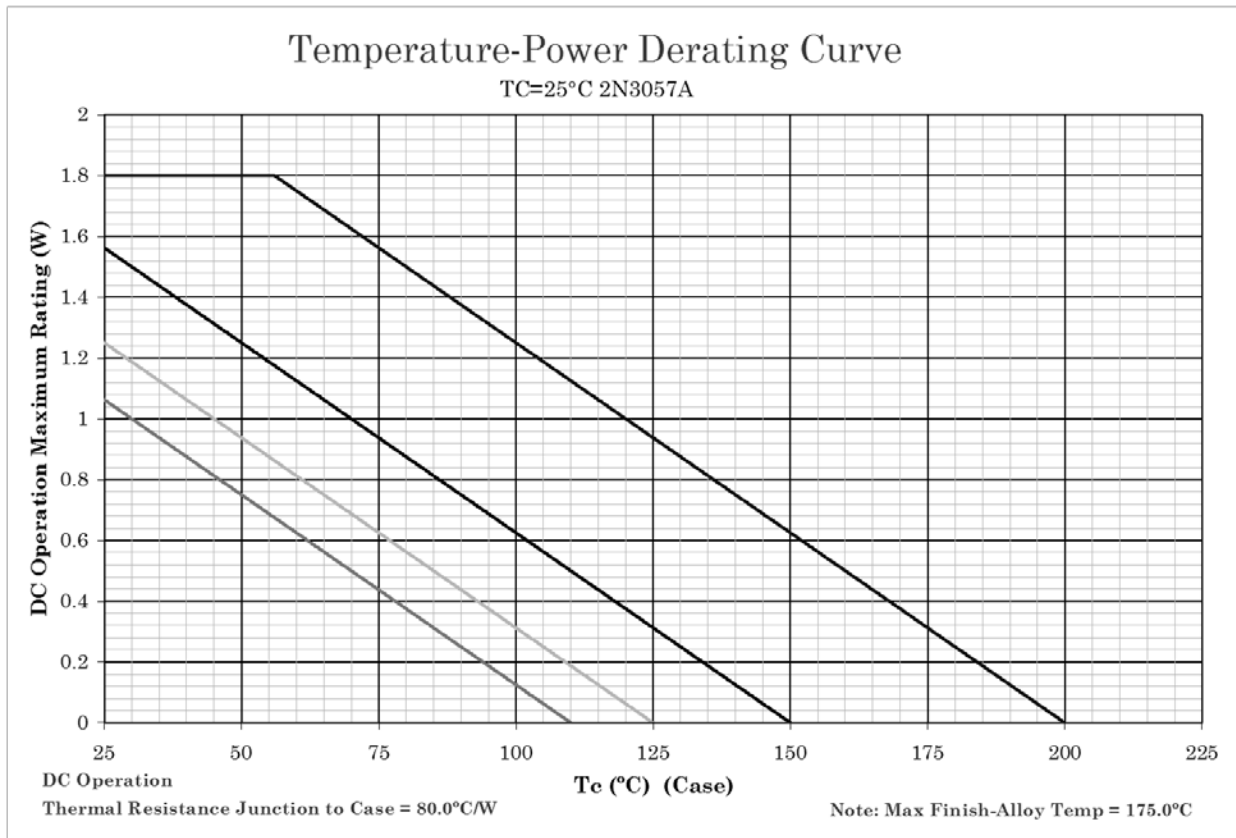
FIGURE 9. Derating for 2N3019 ($R_{\theta JC}$), base case mounted (TO-5 and TO-39).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

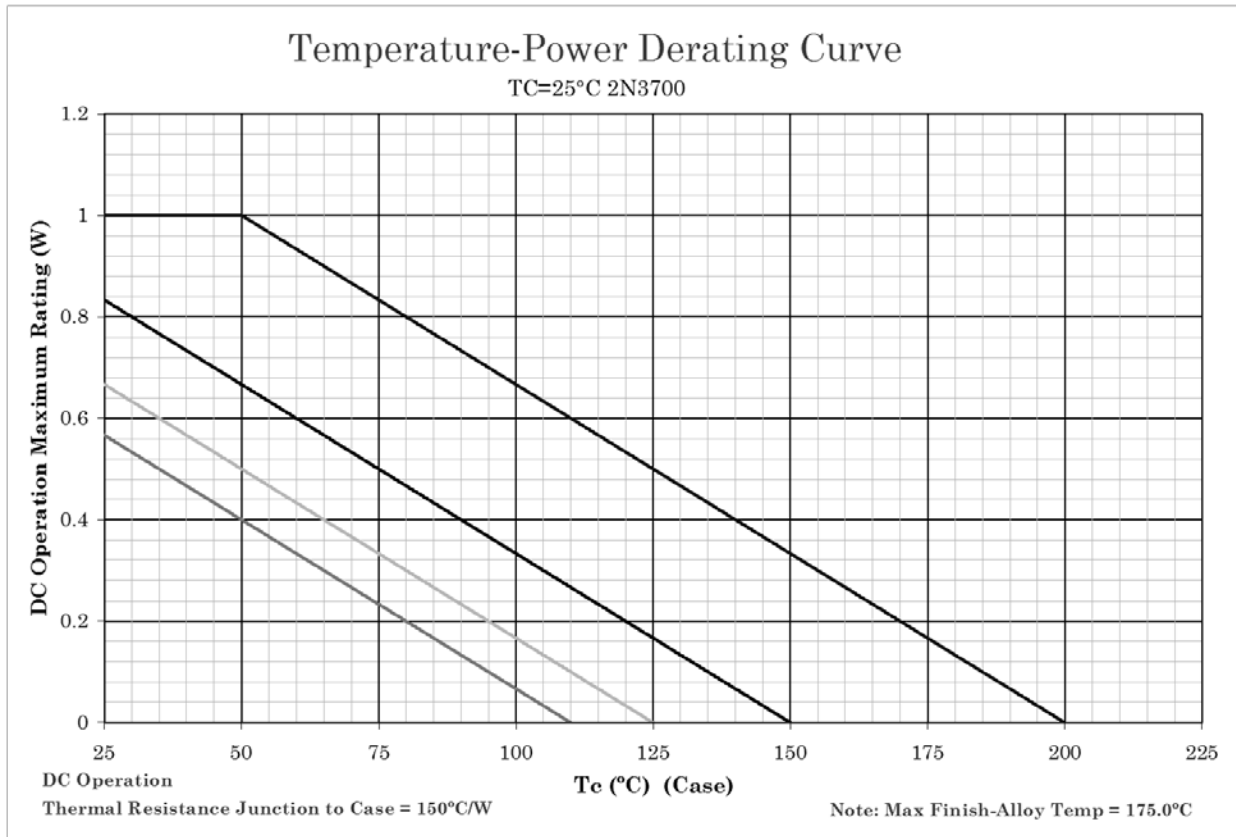
FIGURE 10. Derating for 2N3057A, 2N3700, and 2N3700UB ($R_{\theta JA}$) leads .125 inch (3.175 mm).



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

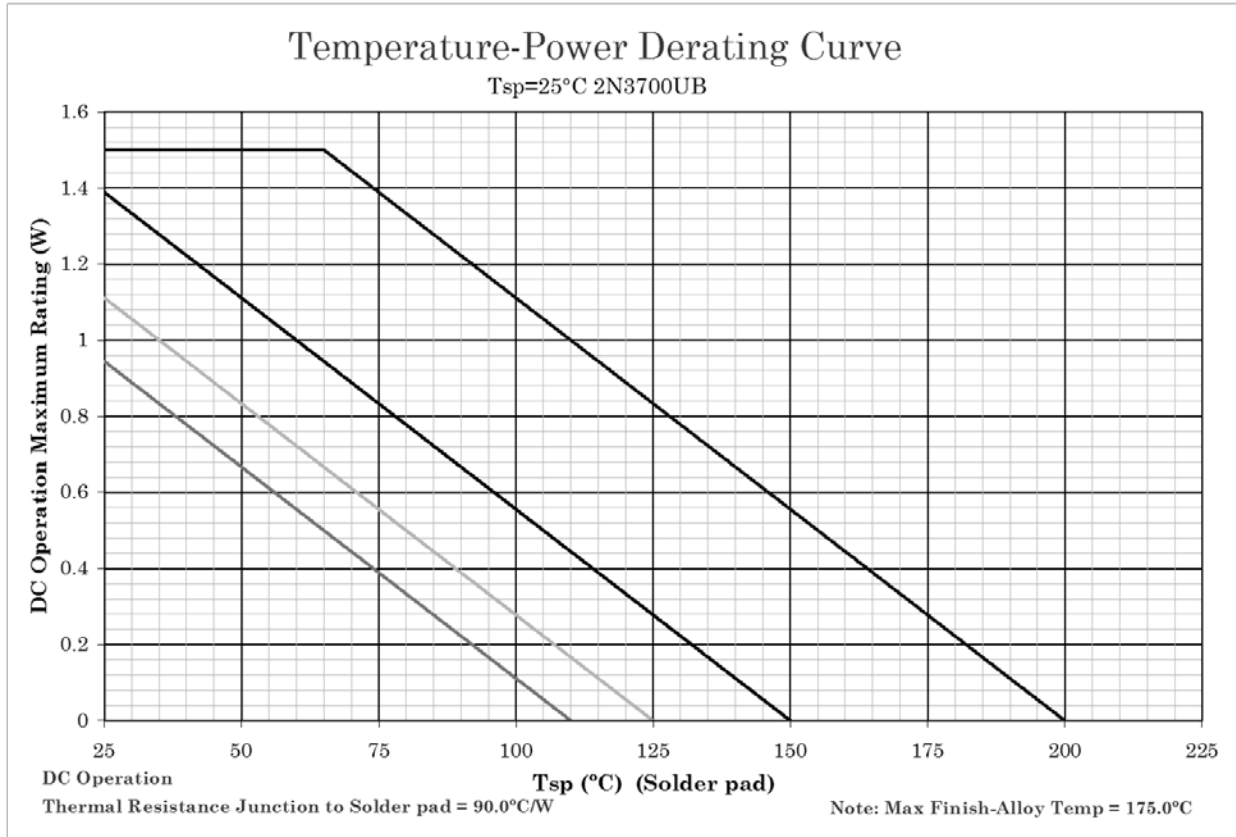
FIGURE 11. Derating for 2N3057A ($R_{\theta Jc}$) (TO-46), base case mounted.



NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

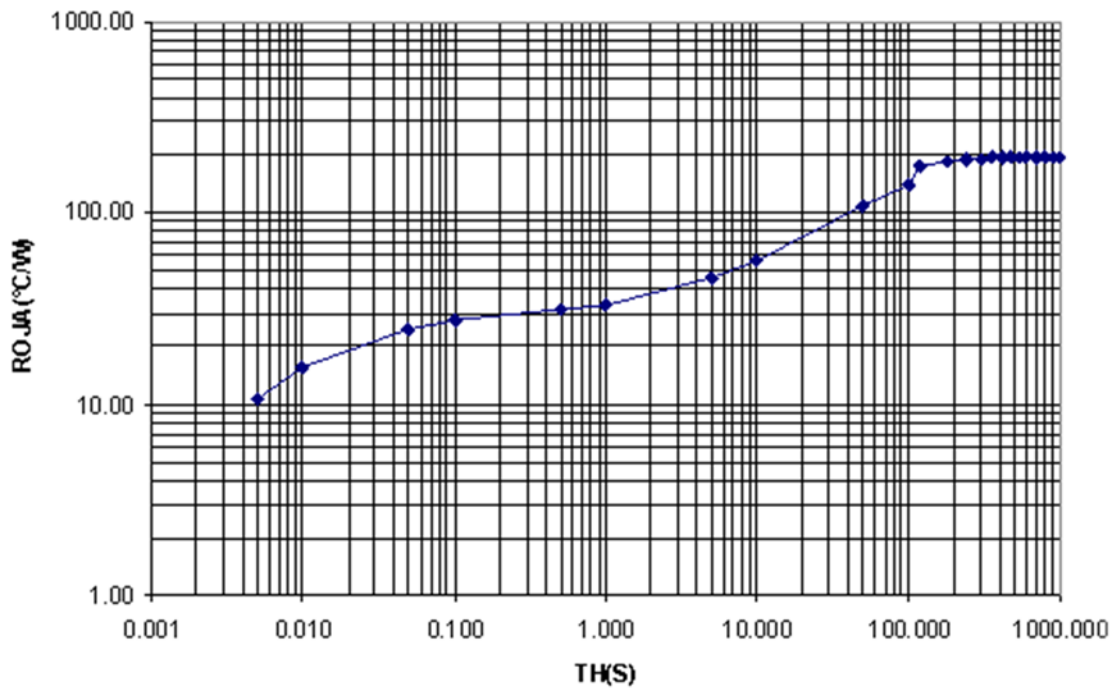
FIGURE 12. Derating for 2N3700 ($R_{\theta JC}$) (TO-18), base case mounted.

**NOTES:**

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 13. Derating for 2N3700UB ($R_{\theta_{JSP(S)}}$), infinite sink 3-points.

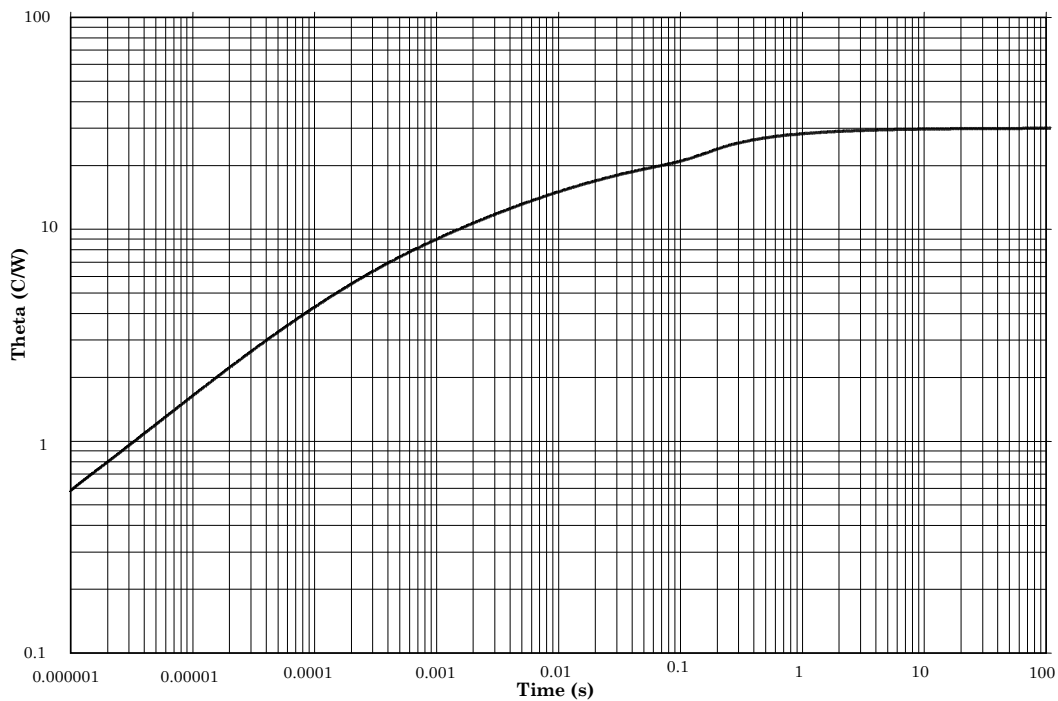
Maximum Thermal Impedance



$R_{\theta JA} = 195^{\circ}\text{C/W}$

FIGURE 14. Thermal impedance graph ($R_{\theta JA}$) for 2N3019 (TO-5 and TO-39).

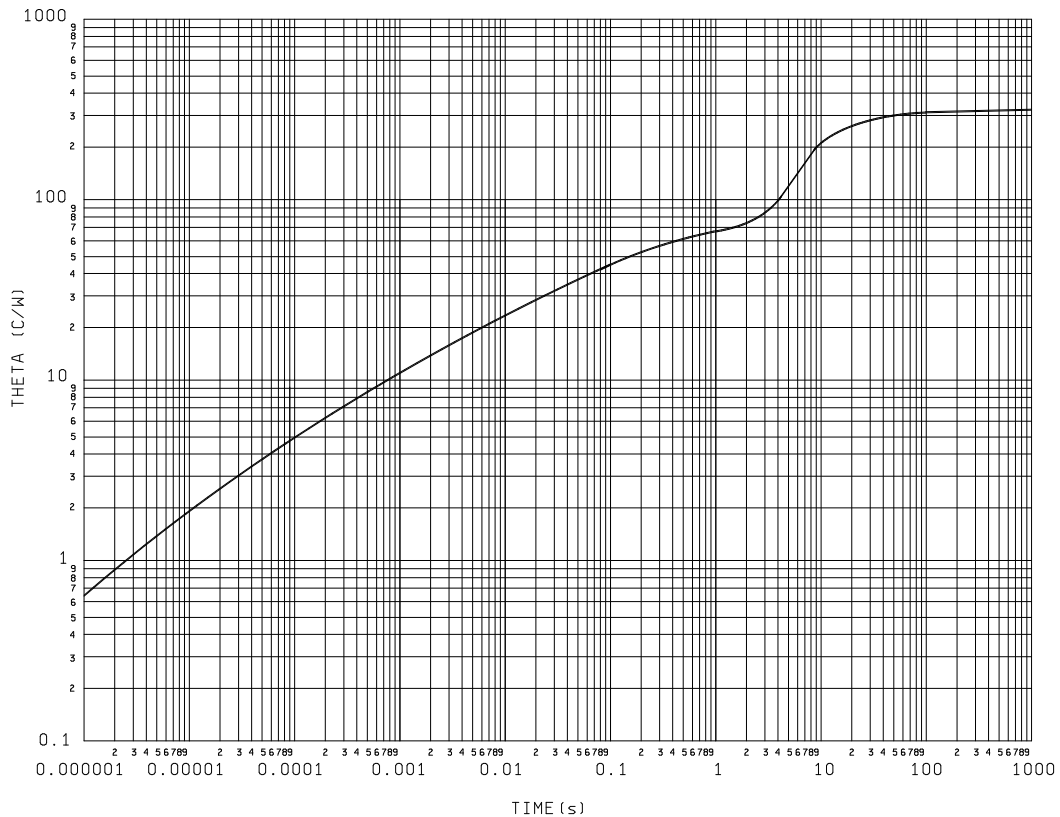
Maximum Thermal Impedance



$R_{\theta JC} = 30^{\circ}\text{C/W}$

FIGURE 15. Thermal impedance graph ($R_{\theta JC}$) for 2N3019 (TO-5 and TO-39).

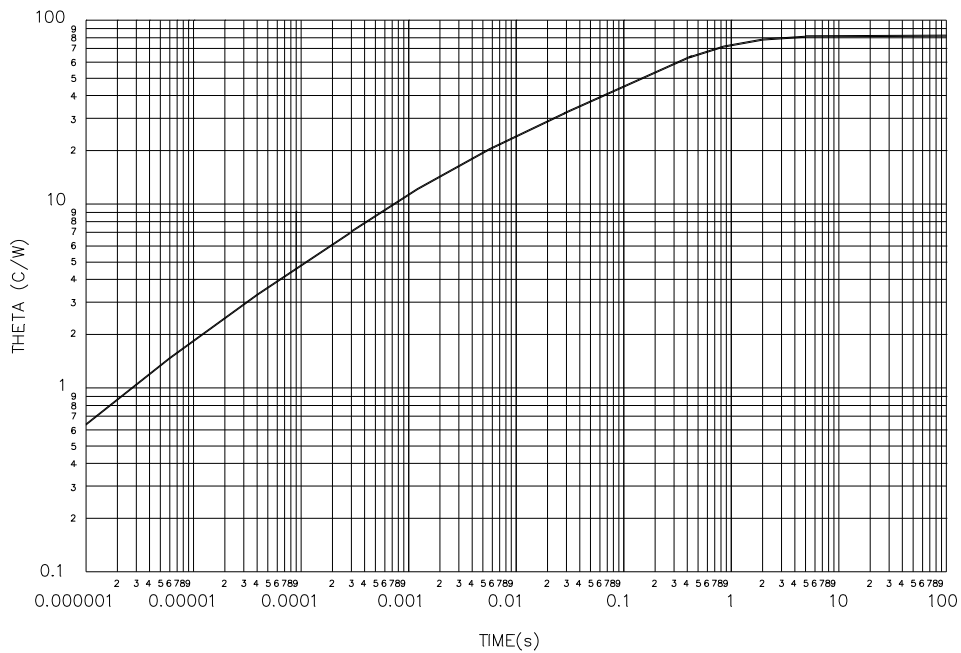
Maximum Thermal Impedance



$R_{\theta JA} = 325^{\circ}\text{C/W}$

FIGURE 16. Thermal impedance graph ($R_{\theta JA}$) 2N3057A (TO-46).

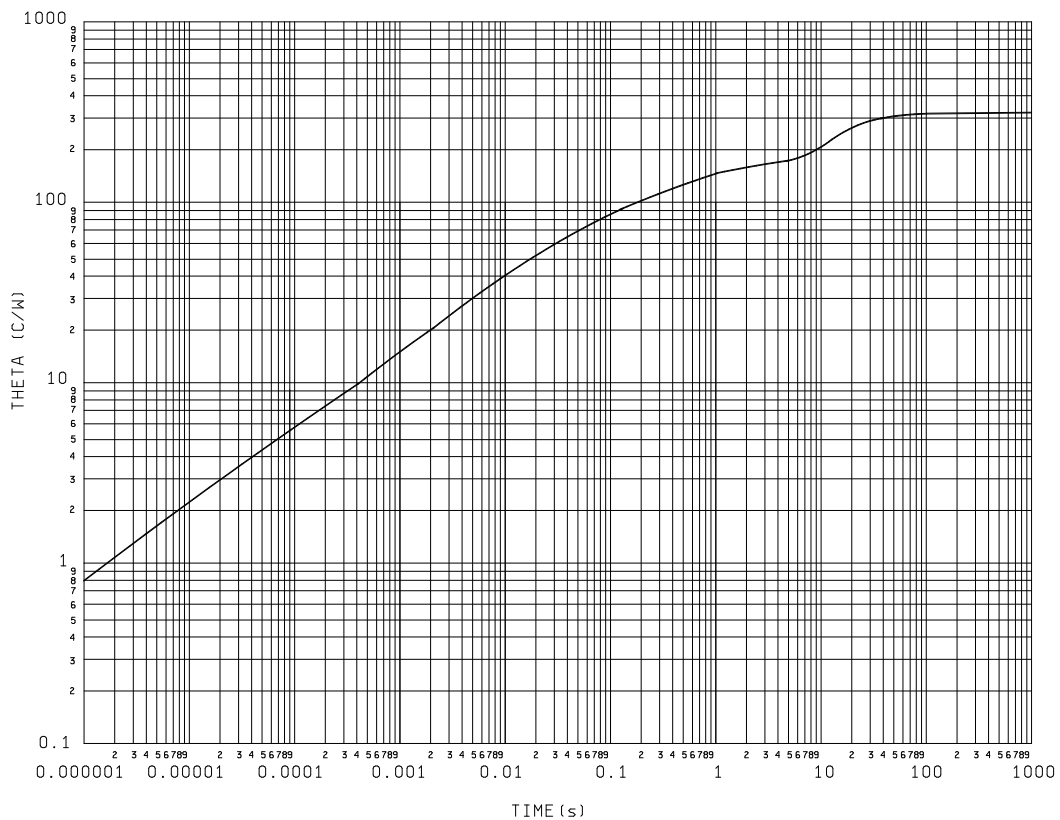
Maximum Thermal Impedance



$R_{\theta JC} = 80^{\circ}\text{C/W}$

FIGURE 17. Thermal impedance graph ($R_{\theta JC}$) for 2N3057A (TO-46).

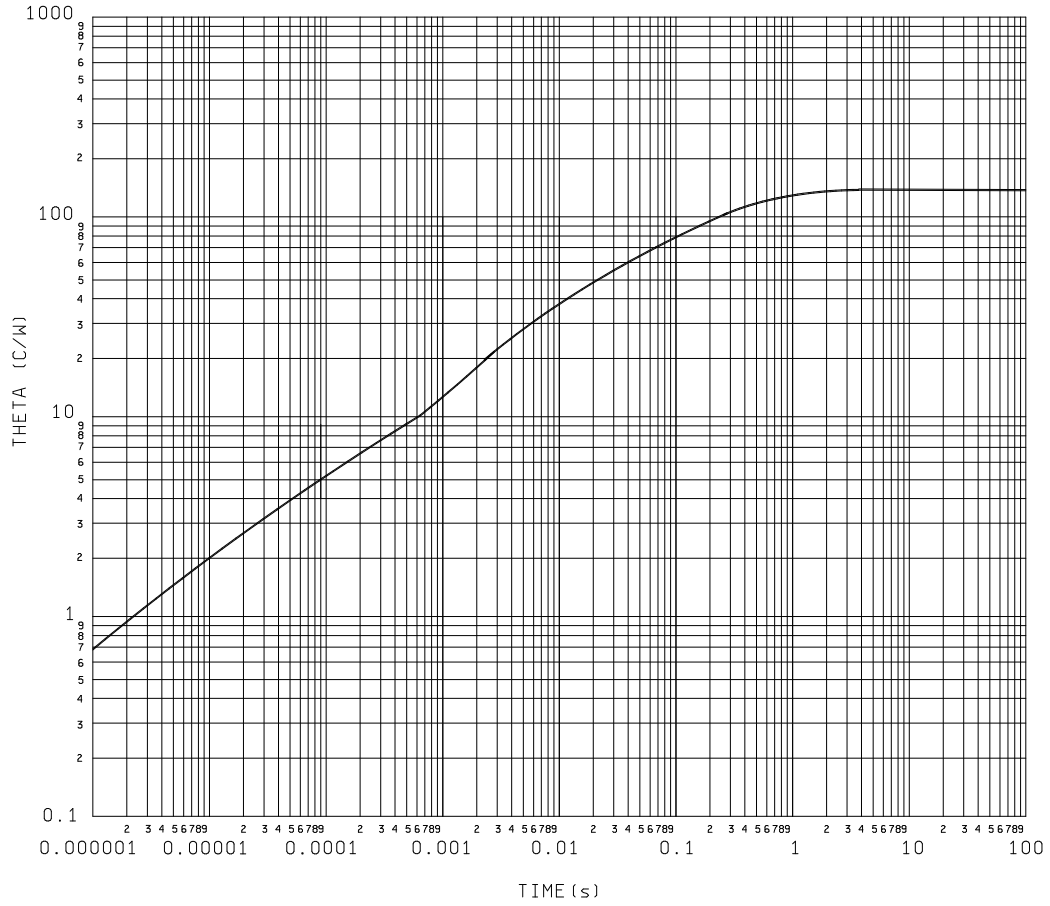
Maximum Thermal Impedance



$R_{\theta JA} = 325^{\circ}\text{C/W}$

FIGURE 18. Thermal impedance graph ($R_{\theta JA}$) for 2N3700 (TO-18).

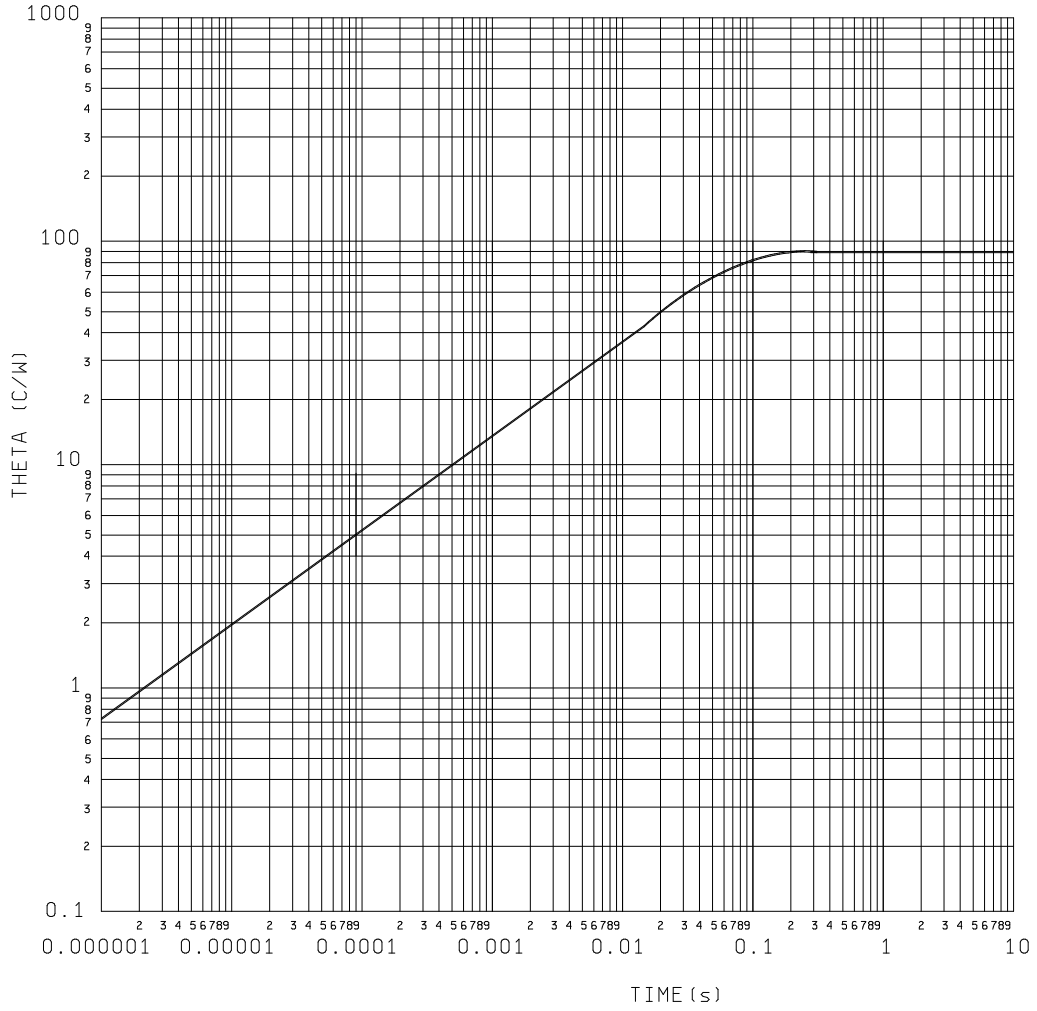
Maximum Thermal Impedance



$R_{\theta JC} = 150^{\circ}\text{C/W}$

FIGURE 19. Thermal impedance graph ($R_{\theta JC}$) for 2N3700 (TO-18).

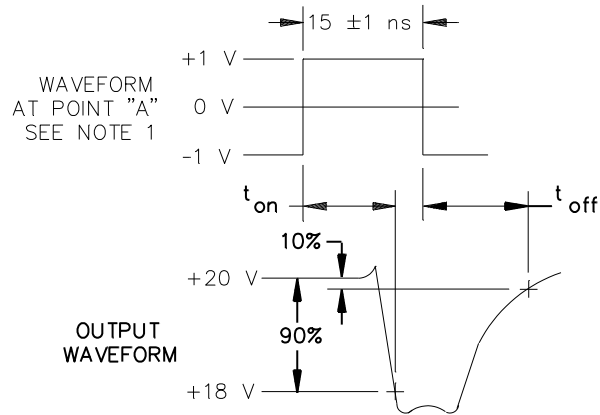
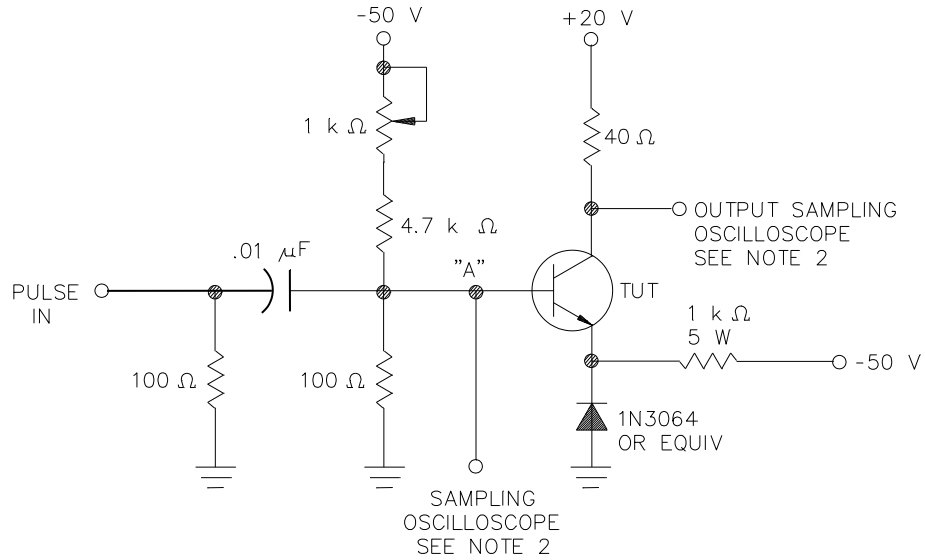
Maximum Thermal Impedance



$R_{\theta JSP(1S)} = 90^{\circ}\text{C/W}$

FIGURE 20. Thermal impedance graph ($R_{\theta JSP(1S)}$) for 2N3700 (UB).

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NOTES:

1. The rise time (t_r) of the applied pulse shall be ≤ 2.0 ns, duty cycle ≤ 2 percent and the generator source impedance shall be 50 ohms.
2. Sampling oscilloscope: $Z_{IN} \geq 100$ k Ω , $C_{IN} \leq 12$ pF, rise time ≤ 2.0 ns.

FIGURE 21. Non-saturated switching-time test circuit.

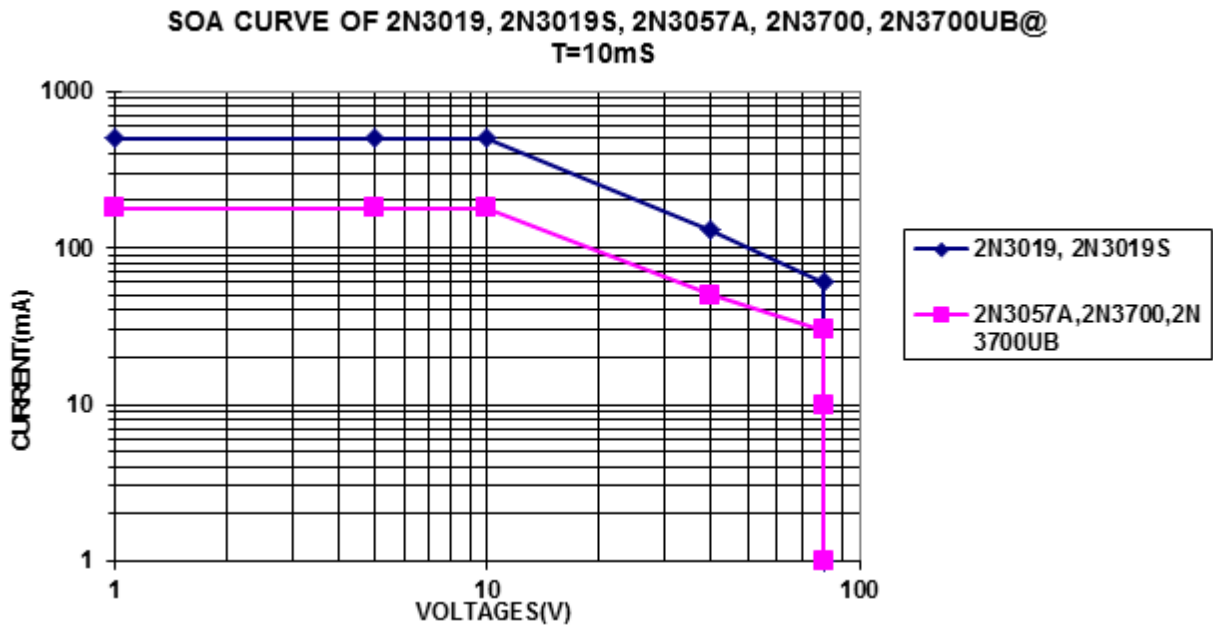


FIGURE 22. Maximum safe operating graph (10 ms).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

* d. The complete PIN, see 1.5.

e. For acquisition of RHA designed devices, [table II](#), subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it must be specified in the contract.

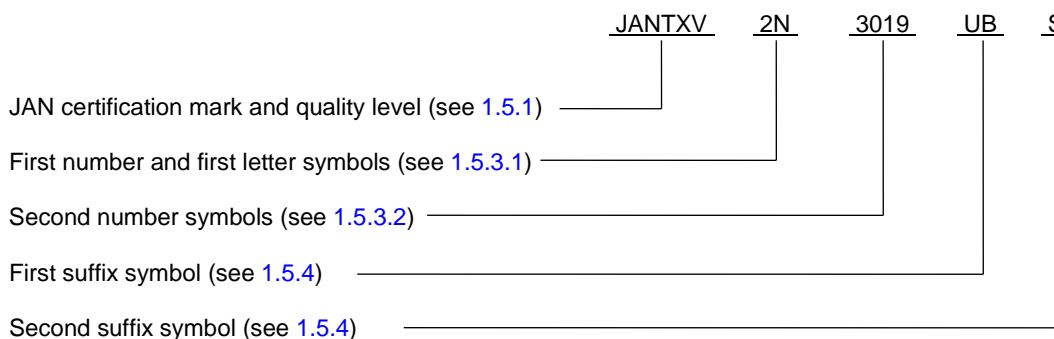
6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QML 19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

* 6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA2N3700) will be identified on the QML.

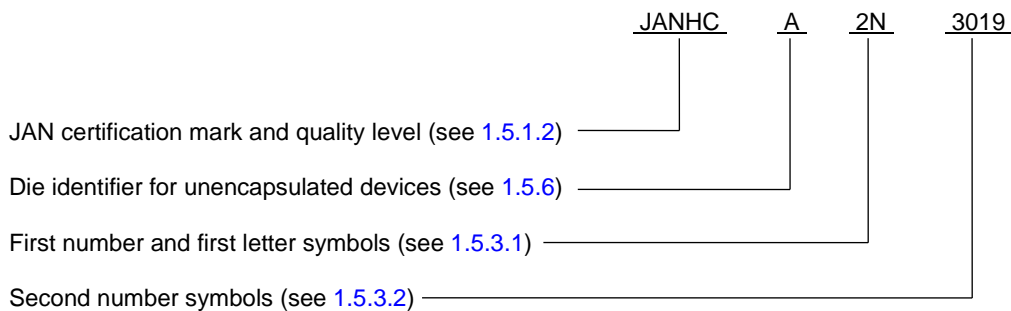
Die ordering information			
PIN	Manufacturer		
	34156	43611	52GC4
2N3700	JANHCA2N3700 JANKCA2N3700	JANHCB2N3700 JANKCB2N3700	JANHCC2N3700 JANKCC2N3700
2N3019	JANHCA2N3019 JANKCA2N3019		

* 6.5 PIN construction example.

* 6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.5.2 Un-encapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



* 6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for types 2N3019 (1)	PINs for types 2N3019S (1)	PINs for types 2N3057A (1)	PINs for types 2N3700 (1)	PINs for types 2N3700UB (1)
JAN2N3019	JAN2N3019S	JAN2N3057A	JAN2N3700	JAN2N3700UB
JANTX2N3019	JANTX2N3019S	JANTX2N3057A	JANTX2N3700	JANTX2N3700UB
JANTXV2N3019	JANTXV2N3019S	JANTXV2N3057A	JANTXV2N3700	JANTXV2N3700UB
JANS2N3019	JANS2N3019S	JANS2N3057A	JANS2N3700	JANS2N3700UB
JANTXVR2N3019	JANTXVR2N3019S	JANTXVR2N3057A	JANTXVR2N3700	JANTXVR2N3700UB
JANTXVF2N3019	JANTXVF2N3019S	JANTXVF2N3057A	JANTXVF2N3700	JANTXVF2N3700UB
JANS#2N3019	JANS#2N3019S	JANS#2N3057A	JANS#2N3700	JANS#2N3700UB

(1) The number sign (#) represents one of eight RHA designators available (M, D, P, L, R, F, G, or H).

* 6.6.1 PINs for unencapsulated devices (die). The following is a list of possible PINs for unencapsulated devices available on this specification sheet.

PINs for types 2N3019 (1)	PINs for types 2N3700 (1)		
JANHCA2N3019	JANHCA2N3700	JANHCB2N3700	JANHCC2N3700
JANKCA2N3019	JANKCA2N3700	JANKCB2N3700	JANKCC2N3700
JANHCA#2N3019	JANHCA#2N3700	JANHCB#2N3700	JANHCC#2N3700
JANKCA#2N3019	JANKCA#2N3700	JANKCB#2N3700	JANKCC#2N3700

(1) The number sign (#) represents one of eight RHA designators available (M, D, P, L, R, F, G, or H).

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC

(Project 5961-2015-016)

Review activities:
 Army - AR, MI, SM
 Navy - AS, MC
 Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.

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[NSBC123TF3T5G](#) [NSBC143TF3T5G](#) [NSVMUN2212T1G](#) [NSVMUN5111DW1T3G](#) [NSVMUN5314DW1T3G](#) [NSVUMC2NT1G](#)

[SMMUN2134LT1G](#) [SMUN2212T1G](#) [SMUN5235T1G](#) [SMUN5330DW1T1G](#) [SSVMUN5312DW1T2G](#) [2SC3650-TD-E](#) [RN1303\(TE85L,F\)](#)

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[SMMUN2111LT3G](#) [SMMUN2113LT1G](#) [SMMUN2114LT1G](#) [SMMUN2211LT3G](#) [SMUN2214T3G](#) [SMUN5113DW1T1G](#)

[SMUN5335DW1T1G](#) [NSBA114YF3T5G](#) [NSBC114TF3T5G](#)