The documentation and process conversion measures necessary to comply with this document shall be completed by 5 September 2015.

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MIL-PRF-19500/382K
5 June 2015
SUPERSEDING
MIL-PRF-19500/382J
18 April 2012

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, PNP, SILICON, LOW-POWER, ENCAPSULATED (THROUGH-HOLE AND SURFACE MOUNT), AND UNENCAPSULATED, RADIATION HARDNESS ASSUARANCE, DEVICE TYPES 2N2944A, 2N2945A, 2N2946A, QUALITY LEVELS: JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL–PRF–19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for low-power, PNP, silicon 2N2944A, 2N2945A, 2N2946A transistors for use in high-speed, switching and general purpose amplifier applications. A 'M' and UB'M' suffix will indicate a matched pair. Four levels of product assurance are provided for each encapsulated device type as specified in MIL–PRF–19500, and two levels of product assurance are provided for each unencapsulated device type. Provisions for radiation hardness assurance (RHA) to eight radiation levels is provided for quality levels JANTX, JANS, JANHC, and JANKC. RHA level designators "M", "D", "P", "L", "R", "F", "G", and "H" are appended to the device prefix to identify devices, which have passed RHA requirements.

* 1.2 Package and die outlines. The device package for the encapsulated device type are as follows: TO-46 in accordance with figure 1 and surface mount in accordance with figure 2. The dimensions and topography for JANHC and JANKC unencapsulated die are in accordance with figure 3.

1.3 Maximum ratings, unless otherwise specified T_A = +25°C.

Types	P_T T_A = +25°C (1) (2)	P_T T_{SP} = +25°C (1) (2)	V_{EBO}	V_{CBO}	V_{CEO}	V_{ECO}	I_C	T_J and T_{STG}	$R_{\theta JA}$ (3) (4)	$R_{\theta JSP}$
	mW	mW	V dc	V dc	V dc	V dc	mA dc	°C	°C/W	°C/W
2N2944A	400	N/A	-15	-15	-10	-10	-100	-65 to	435	N/A
2N2945A, AM	400	N/A	-25	-25	-20	-20	-100	+200	435	N/A
2N2946A	400	N/A	-40	-40	-35	-35	-100		435	N/A
2N2944AUB	400	800	-15	-15	-10	-10	-100	-65 to	435 (5)	90
2N2945AUB	400	800	-25	-25	-20	-20	-100	+200	435 (5)	90
2N2945AUBM	400	800	-25	-25	-20	-20	-100		435 (5)	90
2N2946AUB	400	800	-40	-40	-35	-35	-100		435 (5)	90

(1) For derating, see figures 4 and 5.
(2) See 3.3 for abbreviations.
(3) For thermal curves, see figures 6 and 7.

* Comments, suggestions, or questions on this document should be to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil .

1.3 Maximum ratings, unless otherwise specified T_A = +25°C. - Continued.

(4) For non-thermal conductive PCB or unknown PCB surface mount conditions in free air, substitute figure 6 for the UB package and use $R_{\theta JA}$.

(5) T_A = +55°C for UB on printed circuit board (PCB), PCB = FR4 .0625 inch (1.59 mm) 1 - layer 1 Oz Cu, horizontal, still air, pads (UB) = .034 inch (0.86 mm) x .048 inch (1.22 mm), $R_{\theta JA}$ with a defined thermal resistance condition included is measured at P_T = 400 mW.

1.4 Primary electrical characteristics unless otherwise specified T_A = +25°C.

Limits	h_{FE1} V_{CE} = -0.5 V dc I_C = -1 mA dc				h_{FE} (inv)$_1$ V_{EC} = -0.5 V dc I_E = -200 µA dc			r_{ec} (on)$_2$ I_B = -1 mA dc I_e = 100 µA ac(rms) I_E = 0; f = 1 kHz	
	2N2944A	2N2945		2N2946A	2N2944A	2N2945A	2N2946A	2N2944A	2N2945A
		A, UB	AM, AUBM						
Min	100	70	70	50	50	30	20	ohms	ohms
Max			200					4	6

Limits	r_{ec} (on)$_2$ I_B = -1 mA dc I_e = 100 µA ac(rms) I_E = 0; f = 1 kHz	V_{EC} (ofs)					
		I_B = -200 µA dc I_E = 0			I_b = -1.0 mA dc I_E = 0		
	2N2946A	2N2944A	2N2945A	2N2946A	2N2944A	2N2945A	2N2946A
Min	ohms	mV dc	mV dc	mV dc	mV dc	mV dc	mV dc
Max	8	-0.3	-0.5	-0.8	-0.6	-1.0	-2.0

Limits	$\lvert h_{fe} \rvert$ f = 1 MHz V_{CE} = -6 V dc I_C = -1 mA dc			C_{obo} V_{CB} = -6 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	C_{ibo} V_{EB} = -6 V dc I_C = 0 100 kHz ≤ f ≤1 MHz
	2N2944A	2N2945A	2N2946A	2N2945A	
Min	15	10	5	pF	pF
Max	55	55	55	10	6

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL–PRF–19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.

* 1.5.1 JAN brand and quality level designators.

* 1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", “JANTX", "JANTXV", and "JANS".

* 1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANHC" and "JANKC".

* 1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "M", "D", "P", "L", "R", "F", "G", and "H").

* 1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "2944", “2945”, and "2946".

* 1.5.4 Suffix symbols. The following suffix symbols are incorporated in the PIN as applicable.

* 1.5.4.1 First suffix symbol. The first suffix symbol "A" indicates that the switching transistor is a modified version of the approved device type.

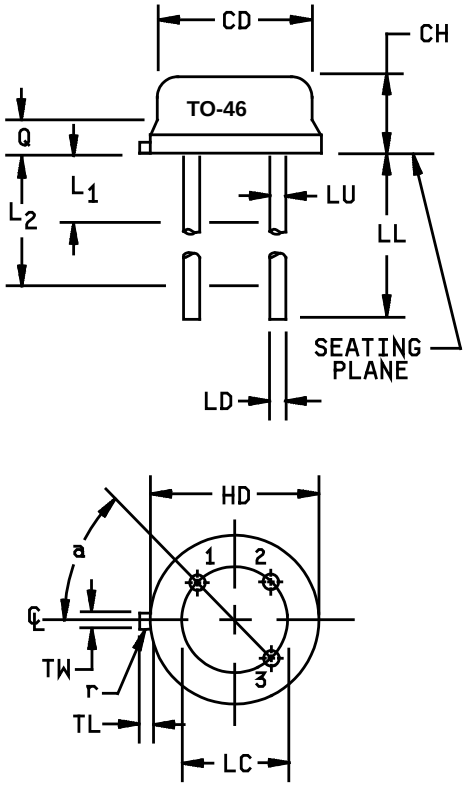
* 1.5.4.2 Following suffix symbols. The following suffix symbols are incorporated in the PIN for this specification sheet:

A	indicates a through-hole mount package similar to a TO–46 metal can (see figure 1).
AM	Indicates a matched pair through-hole mount package similar to a TO–46 metal can (see figure 1).
AUB	Indicates a 4 pad surface mount package (see figure 2).
AUBM	Indicates a matched pair 4 pad surface mount package. (see figure 2).

* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

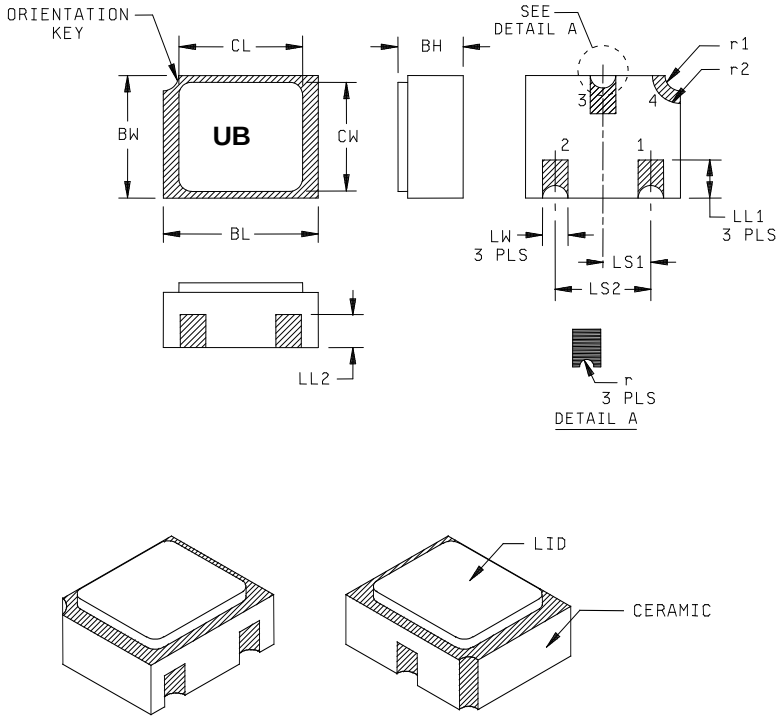
* 1.5.6 Die identifiers for unencapsulated devices (manufacturers and critical interface identifiers). The manufacturer die identifier that is applicable for this specification sheet is "A" (see figure 3 and 6.5).

Ltr.	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.065	.085	1.65	2.16	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		5
LD	.016	.021	0.41	0.53	
LL	.500	1.750	12.70	44.45	6
LU	.016	.019	0.41	0.48	6
L1		.050		1.27	6
L2	.250		6.35		6
Q		.040		1.02	3
TL	.028	.048	0.71	1.22	8
TW	.036	.046	0.91	1.17	4
r		.010		0.25	9
α	45° TP		45° TP		5



NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Symbol TL is measured from HD maximum.
4. Details of outline in this zone are optional.
5. Leads at gauge plane .054 inch (1.37 mm) +.001 inch (0.03 mm) -.000 inch (0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of TP relative to tab. Device may be measured by direct methods or by gauge.
6. Symbol LU applies between L_1 and L_2. Dimension LD applies between L_2 and LL minimum.
7. Lead number three is electrically connected to case.
8. Beyond r maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
9. Symbol r applied to both inside corners of tab.
10. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
11. Lead 1 is emitter, lead 2 is base, and lead 3 is collector.

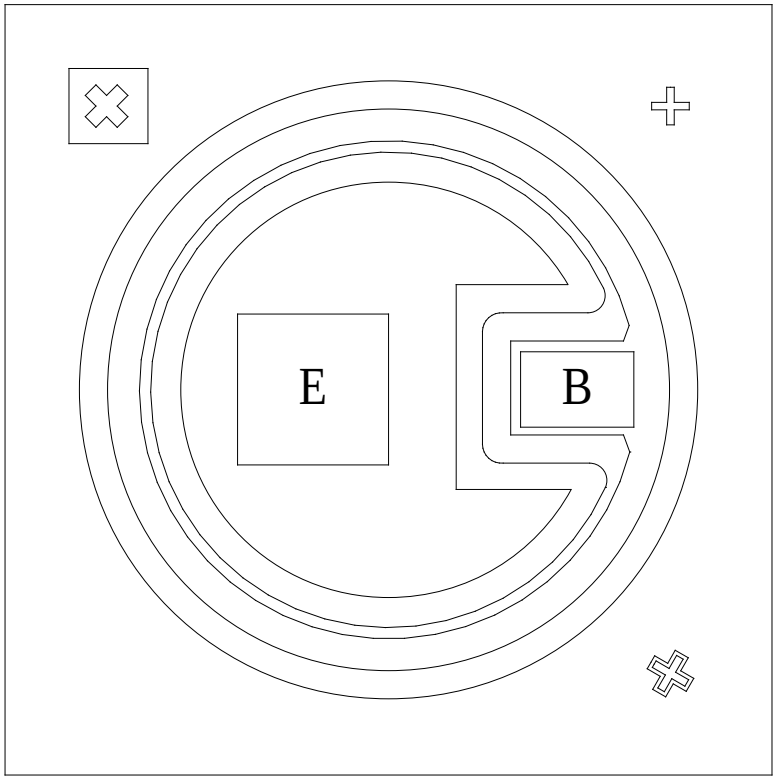
FIGURE 1. Physical dimensions (similar to TO-46).



Symbol	Dimensions				Note	Symbol	Dimensions				Note
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
BH	.046	.056	1.17	1.42		LS1	.035	.039	0.89	0.99	
BL	.115	.128	2.92	3.25		LS2	.071	.079	1.80	2.01	
BW	.085	.108	2.16	2.74		LW	.016	.024	0.41	0.61	
CL		.128		3.25		r		.008		0.20	
CW		.108		2.74		r1		.012		0.31	
LL1	.022	.038	0.56	0.97		r2		.022		0.56	
LL2	.017	.035	0.43	0.89							

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions, surface mount (UB version).



Die size:	.020 x .020 inch (0.508 mm x 0.508 mm).
Die thickness:	.008 ±.0016 inch (0.203 mm ±0.041 mm).
Base pad:	.002 x .003 inch (0.051 mm x 0.076 mm).
Emitter pad:	.004 x .004 inch (0.102 mm x 0.102 mm).
Back metal:	Gold, 6,500 ±1,950 Ang.
Top metal:	Aluminum, 14,500 ±2,500 Ang.
Back side:	Collector.
Glassivation:	SiO_2, 7,500 ±1,500 Ang.

FIGURE 3. Physical dimensions, JANKCA2N2944A through 2N2946A die (also valid for JANHCA2N2944A through 2N2946A).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL–PRF–19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL–STD–750 – Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL–PRF–19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL–PRF–19500 and as follows.

h_{FE} (inv)	Forward-current transfer ratio except that the collector and emitter shall be interchanged in the test circuit, i.e., I_E / I_B.
I_e	Emitter current (rms).
M	Matched pair.
r_{ec}(on)	Small-signal emitter-collector on-state resistance.
$R_{\theta JSP}$	Thermal resistance junction to solder pads.
$V_{(BR)ECO}$	Breakdown voltage, emitter to collector, with base open-circuited.
V_{EC}(ofs)	Emitter to collector offset voltage, i.e., open-circuit voltage between emitter collector when the base-collector junction is forward-biased.
V_{ec}	Emitter to collector voltage (rms).

* 3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL–PRF–19500, and herein. The device package styles shall be as follows: Three pin metal can (similar to TO-46) in accordance with figure 1, four pad surface mount case outline in accordance with figure 2, and unencapsulated die in accordance with figure 3 for device types JANHC and JANKC.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL–PRF–19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Radiation hardness assurance (RHA). Radiation hardness assurance requirements and test levels shall be as defined in MIL–PRF–19500.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

* 3.7 Marking.

* 3.7.1 Through hole mount packages. Marking shall be in accordance with MIL–PRF–19500.

* 3.7.2 Surface mount packages. Marking shall be in accordance with MIL–PRF–19500. The marking on the UB and UBM packages shall consist of an abbreviated part number, the date code, and the manufacturer's symbol or logo. The prefixes JAN, JANTX, JANTXV and JANS can be abbreviated as J, JX, JV, and JS respectively. The "2N" prefix and the "UB" suffix can also be omitted. The radiation hardened designator shall immediately precede (or replace) the device "2N" identifier (depending upon degree of abbreviation required).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL–PRF–19500 and as specified herein.

4.2.1. JANHC and JANKC qualification. JANHC and JANKC qualification inspection shall be in accordance with MIL–PRF–19500.

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening.

* 4.3.1 Screening of encapsulated devices (quality levels JANS, JANTX, and JANTXV only). Screening of encapsulated devices shall be in accordance with table E-IV of MIL–PRF–19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement	
	JANS	JANTX and JANTXV
(1) 3c	Required, method 3131 of MIL-STD-750. (see 4.3.1.2)	Required, method 3131 of MIL-STD-750. (see 4.3.1.2)
9	I_{CBO1} and h_{FE} $(inv)_1$	Not applicable
11	I_{CBO1}; h_{FE} $(inv)_1$; ΔI_{CBO1} = 100 percent of initial value or 0.2 nA dc for 2N2944 and 2N2945, 0.5 nA dc for 2N2946 Δh_{FE} $(inv)_1$ = 25 percent of initial value.	I_{CBO1} and h_{FE} $(inv)_1$
12	See 4.3.1.2.	See 4.3.1.2.
13	Subgroups 2 and 3 of table I herein; ΔI_{CBO1} = 100 percent of initial value or 0.2 nA dc for 2N2944 and 2N2945, 0.5 nA dc for 2N2946; Δh_{FE} $(inv)_1$ = 25 percent of initial value.	Subgroups 2 of table I herein; ΔI_{CBO1} = 100 percent of initial value or 0.2 nA dc for 2N2944A, 2N2945A, 2N2945AM, 2N2945AUB, and 2N2945AUBM. 0.5 nA dc for 2N2946A; Δh_{FE} $(inv)_1$ = 25 percent of initial value.

(1) Shall be performed any time after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1.1 Power burn-in conditions. Power burn-in conditions are as follows: V_{CB} = 10 to 30 V dc. Power shall be applied to achieve T_J = +135°C minimum using a minimum P_D = 75 percent of P_T maximum rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions, T_J, and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval. Use method 3100 of MIL-STD-750 to measure T_J.

4.3.1.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD}, (and V_C where appropriate).

* 4.3.2 Screening of unencapsulated die (JANHC and JANKC). Screening of JANHC and JANKC unencapsulated die shall be in accordance with appendix G of MIL–PRF–19500. The burn-in duration of the JANKC level shall follow the JANS requirements, the JANHC level shall follow the JANTX requirements of table I-IV of MIL–PRF–19500.

* 4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL–PRF–19500 and table I herein.

* 4.4.2 Group B inspection.

* 4.4.2.1 Quality level JANS, table E-Via of MIL-PRF-19500. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIA (JANS) of MIL-PRF-19500. Delta requirements only apply to subgroups B4 and B5 and shall be in accordance with 4.5.3 herein.

Subgroup	Method	Condition
B3	2037	Condition A.
B4	1037	2,000 cycles. No heat sink or forced air cooling on the devices shall be permitted. V_{CB} = 10 V dc. $t_{on} = t_{off}$ = 3 minutes, power = 400 mW.
B5	1027	V_{CB} = 10 V dc. $P_D \geq$ 100 percent of maximum rated P_T (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample). Option 1: 96 hours minimum, sample size in accordance with table VIa of MIL-PRF-19500, adjust T_A or P_D to achieve T_J = +275°C minimum. Option 2: 216 hours, sample size = 45, c = 0; adjust T_A or P_D to achieve T_J = +225°C minimum.

* 4.4.2.2 (Quality levels JAN, JANTX, and JANTXV), table E-VIb of MIL-PRF-19500. Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during CI (conformance inspection) shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and/or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure~~s~~ mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode. Delta requirements for JAN, JANTX, and JANTXV shall be after each step and shall be in accordance with 4.5.6 herein.

Step	Method	Condition
1	1026	Steady-state life: 1,000 hours, V_{CB} = 10 V dc, power shall be applied and ambient temperature adjusted to achieve T_J = +150°C minimum, and a minimum of P_D = 75 percent of P_T as defined in 1.3. n = 45, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, T_A = +150°C, V_{CB} = 80 percent of rated voltage, 48 hours minimum. n = 45 devices, c = 0.
3	1032	High- temperature life (non-operating), T_A = +200°C, t = 340 hours, n = 22, c = 0.

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See MIL-PRF-19500.

b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VII of MIL–PRF–19500, and 4.4.3.1 (JANS), and 4.4.3.2 (JAN, JANTX, and JANTXV) herein for group C testing. delta requirements shall be in accordance with table I, subgroup 2 and 4.5.6 herein.

* 4.4.3.1 Quality level JANS, table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E (not applicable to UB).
C5	3131	$R_{\theta JA}$ only, as applicable (see 1.3) and in accordance thermal impedance curves on figures 6 and 7.
C6	1026	Steady-state life: 1,000 hours, V_{CB} = 10 V dc; power shall be applied to achieve T_J = +150°C minimum and a minimum of P_D = 75 percent of maximum rated P_T as defined in 1.3 n = 45, c = 0. The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.

* 4.4.3.2 Quality levels (JAN, JANTX, and JANTXV), table E-VII of MIL-PRF-19500.

Subgroup	Method	Condition
C2	2036	Test condition E (not applicable to UB).
C5	3131	$R_{\theta JA}$ only, as applicable (see 1.3) and in accordance thermal impedance curves on figures 6 and 7.
C6	1037	Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group D inspection. Conformance inspection for hardness assured JANS, and JANTXV types shall include the group D tests specified in table II herein. These tests shall be performed as required in accordance with MIL–PRF–19500 and method 1019 of MIL-STD-750, for total ionizing dose or method 1017 of MIL-STD-750 for neutron fluence as applicable (see 6.2 herein), except group D, subgroup 2 may be performed separate from other subgroups. Alternate package options may also be substituted for the testing provided there is no adverse effect to the fluence profile.

* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-IX of MIL–PRF–19500 and as specified herein. Delta requirements shall be in accordance with table I, subgroup 2 and 4.5.6 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Input capacitance. This test shall be conducted in accordance with method 3240 of MIL-STD-750, except the output capacitor shall be omitted.

4.5.2 Emitter to collector breakdown voltage. Method of test shall be in accordance with method 3011 of MIL-STD-750, test condition D, except that all references to the collector and the emitter of the transistor shall be interchanged.

4.5.3 Forward-current transfer ratio (inverted connection). Method of test shall be in accordance with method 3076 of MIL-STD-750, except that all references to the collector and the emitter of the transistor shall be interchanged in the test circuit. Then: h_{FE} (inv) = I_E / I_B

4.5.4 Emitter to collector offset voltage. The transistor shall be tested in the circuit of figure 8. The base current shall be adjusted to the specified value. The voltage between the emitter and collector shall then be measured using a voltmeter with an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement.

4.5.5 Small-signal emitter-collector on-state resistance. The transistor shall be tested in the circuit of figure 9. The base current shall be adjusted to the specified value and an ac sinusoidal signal current, I_e, of the specified rms value shall be applied between the emitter and collector. The rms voltage, V_{ec}, between the emitter and collector shall be measured using an ac voltmeter with an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement. The small-signal emitter-collector on-state resistance shall then be determined as follows:

$$r_{ec}\ (on) = V_{ec} / I_e$$

Where V_{ec} is the rms voltage between the emitter and collector.

* 4.5.6 Delta requirements. Delta requirements shall be as specified below. (1) (2) (3) (4)

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector to base cutoff current 2N2944A 2N2945A, 2N2946A	3036	Bias condition D: $I_E = 0$ V_{CB} = -15 V dc V_{CB} = -25 V dc V_{CB} = -40 V dc	ΔI_{CBO1}	100 percent of initial value or .2 nA .2 nA .5 nA	
2	Forward-current transfer ratio (inverted connection)	3076	V_{EC} = -0.5 V dc; I_E = 200 µA dc; (see 4.5.3)	$\Delta h_{FE}(inv)_1$	25 percent of initial value.	

(1) The electrical measurements for table E-VIa (JANS) of MIL-PRF-19500 are as follows: Subgroup 5, see 4.5.6, steps 1 and 2.
(2) The electrical measurements for 4.4.2.2 are as follows: See 4.5.6, steps 1 and 2.
(3) The electrical measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, step 1 and step 2 (JANS).
(4) Group E table III herein, see 4.5.6, steps 1 and 2.

TABLE I. Group A inspection.

Inspection 1/	MIL–STD–750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 2/						
Visual and mechanical 3/ examination	2071					
Solderability 3/ 4/	2026	n = 15 leads, c = 0				
Resistance to 3/ 4/ 5/ solvent	1022	n = 15 devices, c = 0				
Temp cycling 3/ 4/	1051	Test condition C, 25 cycles, n = 22 devices, c = o				
Electrical measurements 4/		Table I, subgroup 2 herein				
Heremetic seal 4/ 6/	1071	n = 22 devices, c = 0				
Fine leak Gross leak						
Bond strength 3/ 4/	2037	Precondition T_A = +250°C at t = 24 hrs or T_A = +300°C at t = 2 hrs, n = 11 wires, c = 0				
Decap internal visual (design verification) 4/	2075	n = 4 devices, c = 0				
Subgroup 2						
Thermal impedance	3131	See 4.3.3	$Z_{\theta JX}$			°C/W
Breakdown voltage collector to emitter 7/	3011	Bias condition D; I_C = -10 μA dc	$V_{(BR)CEO}$			
2N2944A 2N2945A 2N2946A				-10 -20 -35		V dc V dc V dc
Collector to base cutoff current 7/	3036	Bias condition D	I_{CBO1}			
2N2944A 2N2945A 2N2946A		V_{CB} = -15 V dc V_{CB} = -25 V dc V_{CB} = -40 V dc			10 10 10	μA dc μA dc μA dc

See footnotes at the end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL–STD–750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - continued.						
Emitter to base cutoff current 7/	3061	Bias condition D	I_{EBO1}		10	µA dc
2N2944A 2N2945A 2N2946A		V_{EB} = -15 V dc V_{EB} = -25 V dc V_{EB} = -40 V dc				
Breakdown voltage, emitter to collector 7/	3011	Bias condition B; I_E = -10 µA dc; I_B = 0; (see 4.5.2)	$V_{(BR)ECO}$			
2N2944A 2N2945A 2N2946A				-10 -20 -35		V dc V dc V dc
Collector to base cutoff current 7/	3036	Bias condition D	I_{CBO2}			
2N2944A 2N2945A 2N2946A		V_{CB} = -12 V dc V_{CB} = -20 V dc V_{CB} = -32 V dc			-0.1 -0.2 -0.5	nA dc nA dc nA dc
Emitter to base cutoff current 7/	3061	Bias condition D	I_{EBO2}			
2N2944A 2N2945A 2N2946A		V_{EB} = -12 V dc V_{EB} = -20 V dc V_{EB} = -32 V dc			-0.1 -0.2 -0.5	nA dc nA dc nA dc
Forward-current transfer ratio 7/	3076	V_{CE} = -0.5 V dc; I_C = -1.0 mA dc	h_{FE1}			
2N2944A 2N2945A 2N2945AM 2N2946A				100 70 70 50	 200 	
Forward-current transfer ratio (inverted connection) 7/	3076	V_{EC} = -0.5 V dc; I_E = -200 µA dc (see 4.5.3)	h_{FE} (inv)$_1$			
2N2944A 2N2945A 2N2946A				50 30 20		

See footnotes at the end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL–STD–750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - continued.						
Emitter to collector offset voltage 7/		I_B = -200 µA dc; I_E = 0; (see 4.5.4 and figure 8)	V_{EC} (ofs)$_1$			
2N2944A					-0.3	mV dc
2N2945A					-0.5	mV dc
2N2946A					-0.8	mV dc
Emitter to collector offset voltage 7/		I_B = -1 mA dc; I_E = 0; (see 4.5.4 and figure 8)	V_{EC} (ofs)$_2$			
2N2944A					-0.6	mV dc
2N2945A					-1.0	mV dc
2N2946A					-2.0	mV dc
Emitter to collector offset voltage 7/		I_B = -2 mA dc; I_E = 0; (see 4.5.4 and figure 8)	V_{EC} (ofs)$_3$			
2N2944A					-1.0	mV dc
2N2945A					-1.6	mV dc
2N2946A					-2.5	mV dc
Subgroup 3						
High-temperature operation:		T_A = +100°C				
Collector to base cutoff current 7/	3036	Bias condition D; I_C = 0	I_{CBO3}			
2N2944A		V_{CB} = -15 V dc			10	nA dc
2N2945A		V_{CB} = -25 V dc			20	nA dc
2N2946A		V_{CB} = -40 V dc			25	nA dc
Emitter to base cutoff current 7/	3061	Bias condition D; I_C = 0	I_{EBO3}			
2N2944A		V_{CB} = -15 V dc			10	nA dc
2N2945A		V_{CB} = -25 V dc			15	nA dc
2N2946A		V_{CB} = -40 V dc			20	nA dc

See footnotes at the end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL–STD–750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3 – continued.						
Low-temperature operation:		T_A = -55°C				
Forward-current transfer ratio 7/	3076	V_{CE} = -0.5 V dc; I_C = -1 mA dc	h_{FE2}			
2N2944A				35		
2N2945A				25		
2N2946A				20		
Forward-current transfer ratio (inverted connection) 7/	3076	V_{EC} = -0.5 V dc; I_E = -200 μA dc (see 4.5.3)	h_{FE} (inv)$_2$			
2N2944A				25		
2N2945A				15		
2N2946A				10		
Subgroup 4						
Small-signal emitter-collector on-state resistance 7/		I_B = -100 μA dc; I_E = 0; I_e = 100 μA ac (rms) f = 1 kHz (see 4.5.5 and figure 9)	r_{ec} (on)$_1$			
2N2944A					10	ohm
2N2945A					12	ohm
2N2946A					14	ohm
Small-signal emitter-collector on-state resistance 7/		I_B = -1 mA dc; I_E = 0; I_e = 100 μA ac (rms) f = 1 kHz (see 4.5.5 and figure 9)	r_{ec} (on)$_2$			
2N2944A					4	ohm
2N2945A					6	ohm
2N2946A					8	ohm

See footnotes at the end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL–STD–750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4 – continued.						
Magnitude of common-emitter small-signal short-circuit forward-current transfer ratio 7/		V_{CE} = -6 V dc; I_C = -1 mA dc; f = 1 MHz	$\lvert h_{fe} \rvert$			
2N2944A				15	55	
2N2945A				10	55	
2N2946A				5	55	
Open circuit output capacitance	3236	V_{CB} = -6 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		10	pF
Input capacitance (output open-circuited)	3240	V_{EB} = -6 V dc; I_C = 0; 100 kHz ≤ f ≤ 1 MHz (see 4.5.1)	C_{ibo}		6.0	pF
Pulse response:						
Delay time	3251	Test condition B (see figure 10)	t_d		50	ns
Rise time	3251	Test condition B (see figure 10	t_r		100	ns
Storage time	3251	Test condition B (see figure 10)	t_s		350	ns
Fall time	3251	Test condition B (see figure 10)	t_f		100	ns
Subgroups 5, and 6						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.
2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests.
3/ Separate samples may be used.
4/ Not required for JANS.
5/ Not required for laser marked devices.
6/ Hermetic seal test is an end-point to temperature cycling in addition to electrical measurements.
7/ 2N2945AM and 2N2945AUBM shall meet all other requirements as specified in accordance with table I for 2N2945A and 2N2945AUB.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/						
Neutron irradiation	1017	Neutron exposure V_{CES} = 0 V				
Breakdown voltage collector to emitter	3011	Bias condition D I_C = -10 µA dc	$V_{(BR)CEO}$			
2N2944A				-10		V dc
2N2945A				-20		V dc
2N2946A				-35		V dc
Collector to base cutoff current	3036	Bias condition D	I_{CBO1}			
2N2944A		V_{CB} = -15 V dc			20	µA dc
2N2945A		V_{CB} = -25 V dc			20	µA dc
2N2946A		V_{CB} = -40 V dc			20	µA dc
Emitter to base cutoff current	3061	Bias condition D	I_{EBO1}			
2N2944A		V_{BE} = -15 V dc			20	µA dc
2N2945A		V_{BE} = -25 V dc			20	µA dc
2N2946A		V_{BE} = -40 V dc			20	µA dc
Breakdown voltage emitter to collector	3011	Bias condition ~~D~~ B; I_E = -10 µA dc; I_B = 0 mA dc, pulsed (see 4.5.2)	$V_{(BR)ECO}$			
2N2944A				-10		V dc
2N2945A				-20		V dc
2N2946A				-35		V dc
Collector to base cutoff current	3036	Bias condition D;	I_{EBO2}			
2N2944A		V_{CB} = -12 V dc			-0.2	ηA dc
2N2945A		V_{CB} = -20 V dc			-0.4	ηA dc
2N2946A		V_{CB} = -32 V dc			-1.0	ηA dc
Emitter to base cutoff current	3061	Bias condition D;	I_{CBO2}			
2N2944A		V_{CB} = -12 V dc			-0.2	ηA dc
2N2945A		V_{CB} = -20 V dc			-0.4	ηA dc
2N2946A		V_{CB} = -32 V dc			-1.0	ηA dc
Forward-current transfer ratio	3076	V_{CE} = -0.5 V dc, I_C = -1.0 mA dc	$[h_{FE1}]$			
2N2944A				5/ [50]		
2N2945AB				5/ [35]		
2N2945AM, UBM				5/ [35]	200	
2N2946A				5/ [25]		
Forward-current transfer ratio	3076	V_{EC} = -0.5 V dc, I_C = -200 µA dc; pulsed (see 4.5.1)	$[h_{FE}(inv)_1]$			
2N2944A				5/ [25]		
2N2945A				5/ [15]		
2N2946A				5/ [10]		

See footnotes at end of table.

TABLE II. Group D inspection. - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1 4/ - Continued						
Emitter to collector offset voltage	3071	I_B = -200 µA dc, I_E = 0, pulsed (see 4.5.4 and figure 8)	$V_{EC(ofs)1}$			
2N2944A					-0.5	mV dc
2N2945A					-0.8	mV dc
2N2946A					-1.2	mV dc
Emitter to collector offset voltage	3071	I_B = -1.0 mA dc, I_E = 0 pulsed (see 4.5.4 and figure 8)	V_{EC} $(ofs)_2$			
2N2944A					-0.9	mV dc
2N2945A					-1.5	mV dc
2N2946A					-3.0	mV dc
Emitter to collector offset voltage	3071	I_B = -2.0 mA dc, I_E = 0 pulsed (see 4.5.4 and figure 8)	$V_{EC\ (ofs)3}$			
2N2944A					-1.5	mV dc
2N2945A					-2.4	mV dc
2N2946A					-3.8	mV dc
Subgroup 2 4/						
Steady-state total dose irradiation	1019					
2N2944A		Gamma exposure V_{ECS} = -8 V				
2N2945A		Gamma exposure V_{ECS} = -16 V				
2N2946A		Gamma exposure V_{ECS} = -28 V				
Breakdown voltage collector to emitter	3011	Bias condition D I_C = -10 µA dc	$V_{(BR)CEO}$			
2N2944A				-10		V dc
2N2945A				-20		V dc
2N2946A				-35		V dc
Collector to base cutoff current	3036	Bias condition D	I_{CBO1}			
2N2944A		V_{CB} = -15 V dc			20	µA dc
2N2945A		V_{CB} = -25 V dc			20	µA dc
2N2946A		V_{CB} = -40 V dc			20	µA dc
Emitter to base cutoff current	3061	Bias condition D	I_{EBO1}			
2N2944A		V_{BE} = -15 V dc			20	µA dc
2N2945A		V_{BE} = -25 V dc			20	µA dc
2N2946A		V_{BE} = -40 V dc			20	µA dc
Breakdown voltage emitter to collector	3011	Bias condition B; I_E = -10 µA dc; I_B = 0 mA dc, pulsed (see 4.5.2)	$V_{(BR)ECO}$			
2N2944A				-10		V dc
2N2945A				-20		V dc
2N2946A				-35		V dc

See footnotes at end of table.

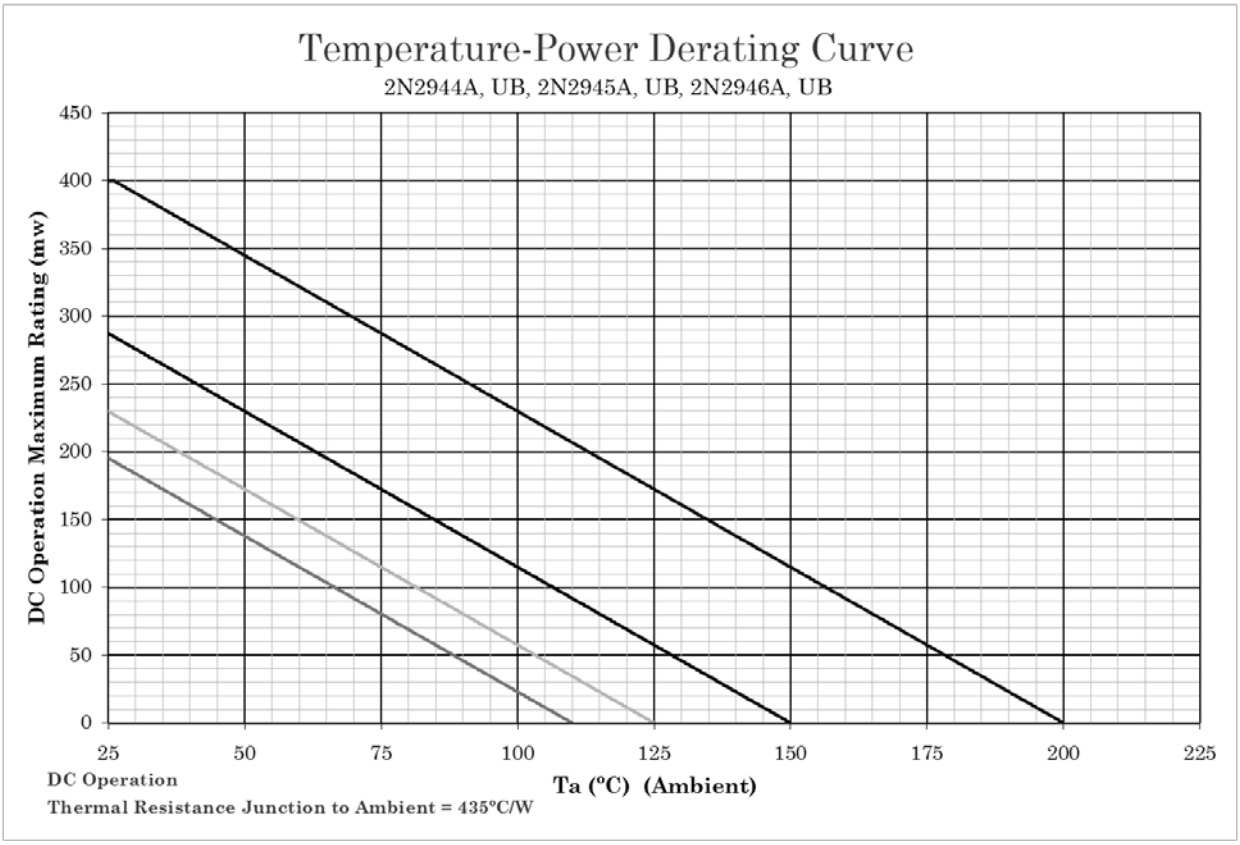
TABLE II. Group D inspection. - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 4/ - Continued.						
Collector to base cutoff current	3036	Bias condition D	I_{CBO2}			
2N2944A		V_{CB} = -12 V dc			-0.2	ηA dc
2N2945A		V_{CB} = -20 V dc			-0.4	ηA dc
2N2946A		V_{CB} = -32 V dc			-1.0	ηA dc
Emitter to base cutoff current	3061	Bias condition D	I_{EBO2}			
2N2944A		V_{CB} = -12 V dc			-0.2	ηA dc
2N2945A		V_{CB} = -20 V dc			-0.4	ηA dc
2N2946A		V_{CB} = -32 V dc			-1.0	ηA dc
Forward-current transfer ratio	3076	V_{CE} = -0.5 V dc, I_C = -1.0 mA dc	$[h_{FE1}]$			
2N2944A				5/ [50]		
2N2945A				5/ [35]		
2N2945AM, UBM				5/ [35]	200	
2N2946A				5/ [25]		
Forward-current transfer ratio	3076	V_{EC} = -0.5 V dc, I_C = -200 µA dc; pulsed (see 4.5.1)	$[h_{FE}(inv)_1]$			
2N2944A				5/ [25]		
2N2945A				5/ [15]		
2N2946A				5/ [10]		
Emitter to collector offset voltage		I_B = -200 µA dc, I_E = 0, pulsed (see 4.5.4 and figure 8)	$V_{EC(ofs)1}$			
2N2944A					-0.5	mV dc
2N2945A					-0.8	mV dc
2N2946A					-1.2	mV dc
Emitter to collector offset voltage		I_B = -1.0 mA dc, I_E = 0 pulsed (see 4.5.4 and figure 8)	$V_{EC(ofs)2}$			
2N2944A					-0.9	mV dc
2N2945A					-1.5	mV dc
2N2946A					-3.0	mV dc
Emitter to collector offset voltage		I_B = -2.0 mA dc, I_E = 0 pulsed (see 4.5.4 and figure 8)	$V_{EC(ofs)3}$			
2N2944A					-1.5	mV dc
2N2945A					-2.4	mV dc
2N2946A					-3.8	mV dc

1/ Tests to be performed on all devices receiving radiation exposure.
2/ For sampling plan, see MIL-PRF-19500.
3/ Electrical characteristics apply to all device types unless otherwise noted.
4/ See 6.2.e herein.
5/ See method 1019 of MIL-STD-750, for how to determine $[h_{FE}]$ by first calculating the delta($1/h_{FE}$) from the pre- and post-radiation h_{FE}. Notice that $[h_{FE}]$ is not the same as h_{FE} and cannot be measured directly. The $[h_{FE}]$ value can never exceed the pre-radiation minimum h_{FE} that it is based upon.

TABLE III. Group E inspection (all quality levels) – for qualification or re-qualification only.

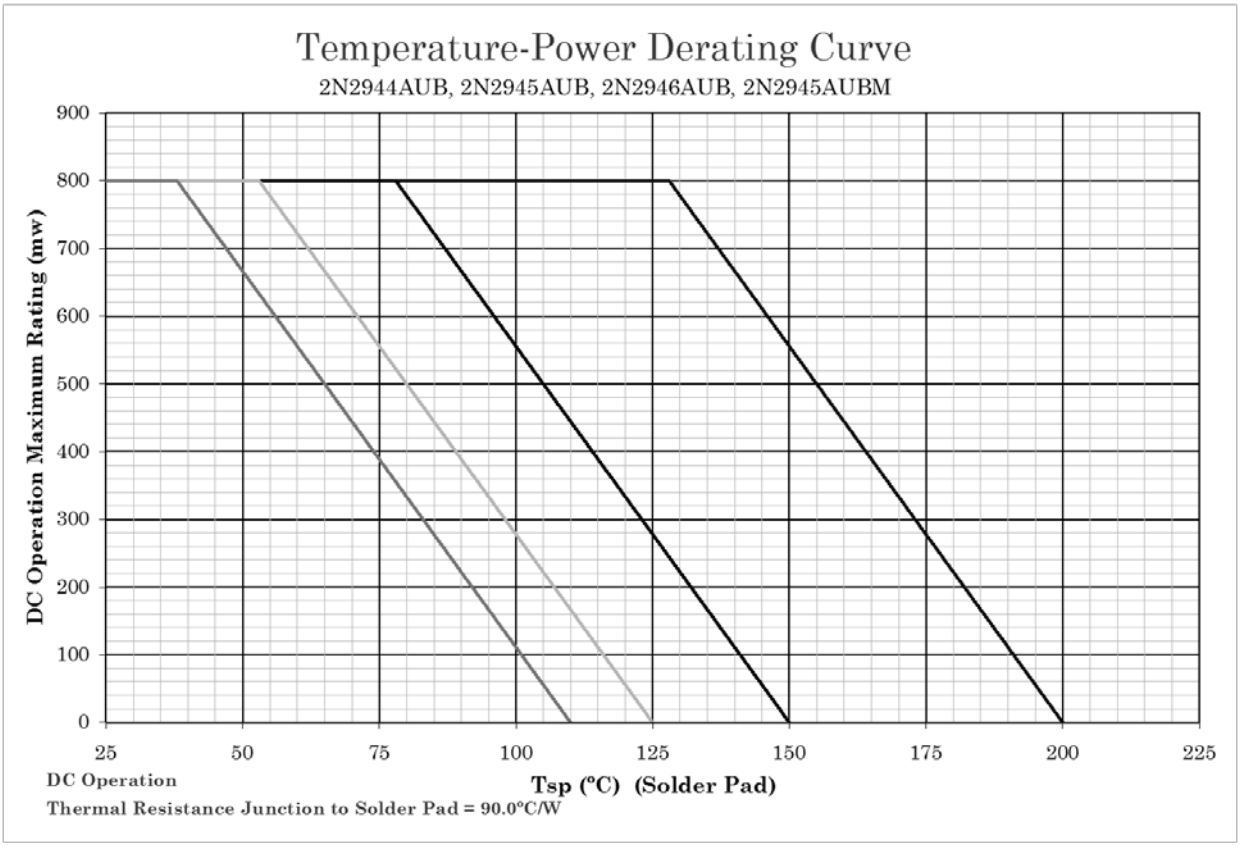
Inspection	MIL–STD–750		Qualification
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2 and 4.5.6 herein.	
Subgroup 2			45 devices c = 0
Intermittent life	1037	V_{CB} = 10 V dc, t_{on} = t_{off} = 3 minutes minimum P_t = 400 mW, 6,000 cycles.	
Electrical measurements		See table I, subgroup 2 and 4.5.6 herein.	
Subgroup 4			15 devices c = 0
Thermal resistance	3131	$R_{\theta JSP}$ can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets).	
Thermal resistance curves		See MIL–PRF–19500.	Sample size N/A
Subgroup 5			
Not applicable			
Subgroup 6			
ESD	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq$, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 4. Derating for 2N2944A, 2N2944AUB, 2N2945A, 2N2945AUB, 2N2946A, and 2N2946AUB ($R_{\theta JA}$), base case mounted (TO-46 and UB).

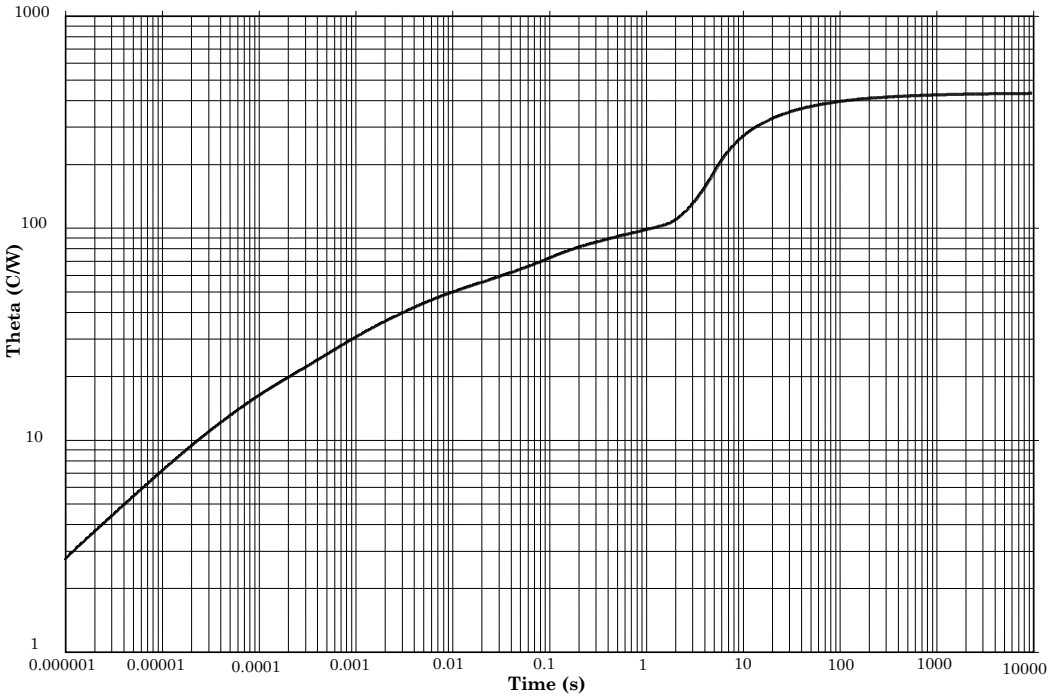


NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200°C$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150°C$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq$, 125°C, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 5. Derating for 2N2944AUB, 2N2945AUB, 2N2945AUBM, and 2N2946AUB ($R_{\theta JSP}$), base case mounted (UB).

Maximum Thermal Impedance

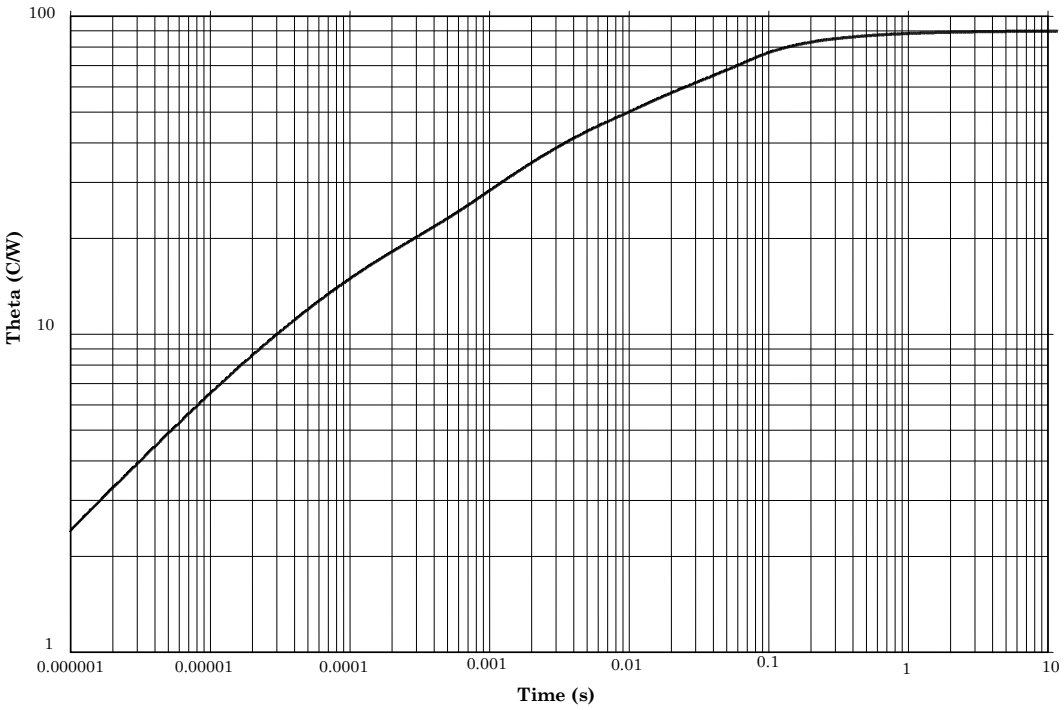


TO-46 free air T_A = +25°C with 16 x 23 mil chip.

T_A = +25°C, Pdiss = 400 mW, 435°C/W (ambient thermal resistance varies with power).

FIGURE 6. Thermal impedance graph ($R_{\theta JA}$) for (TO-46).

Maximum Thermal Impedance



Thermal resistance = 90°C/W

Solder mounted to heavy copper clad PCB at T_C = +25°C.

FIGURE 7. Thermal impedance graph (UB).

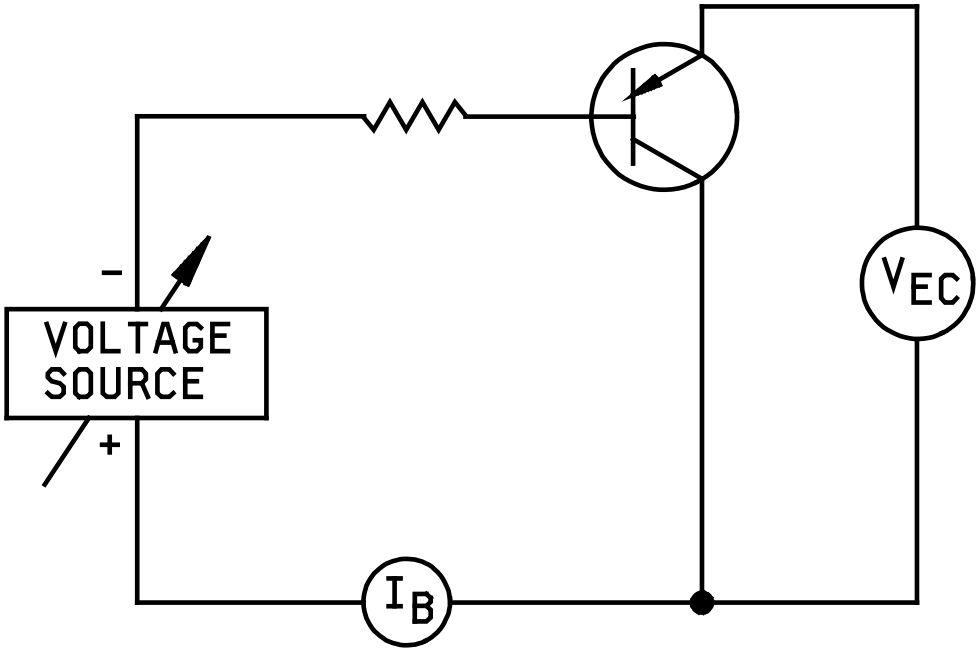


FIGURE 8. Emitter to collector offset voltage test circuit.

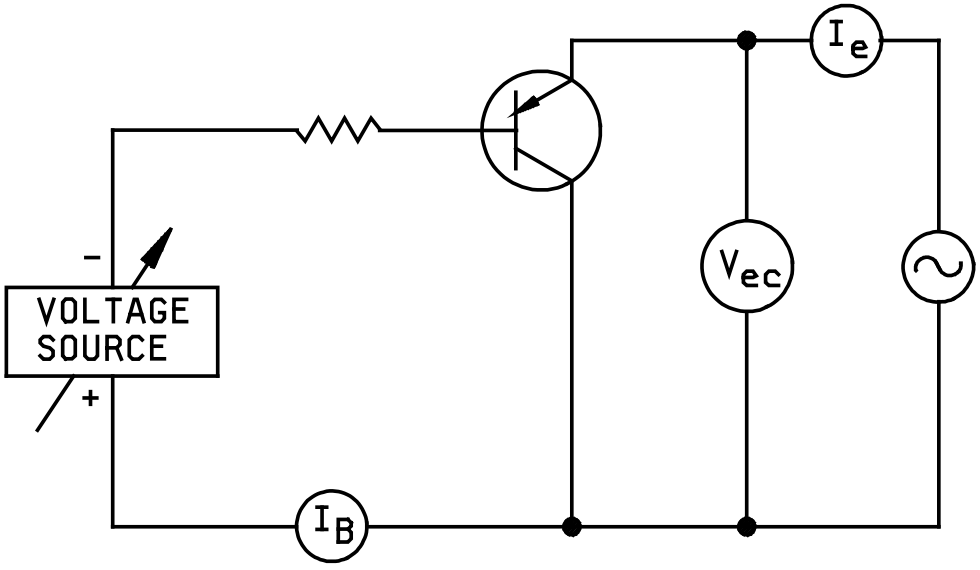
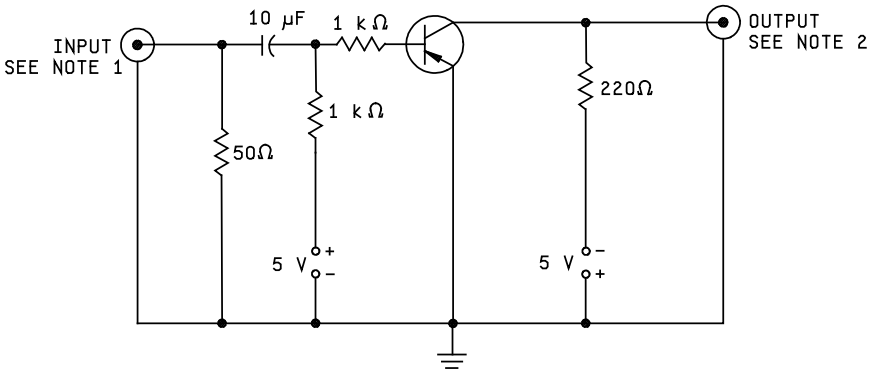
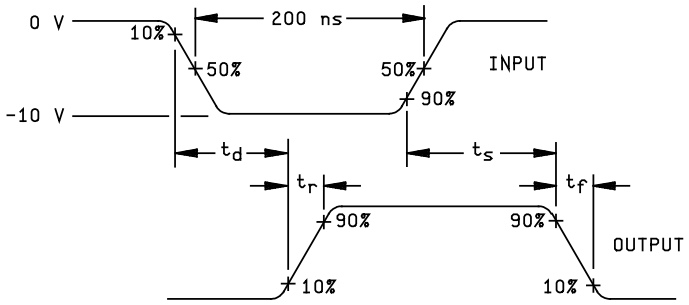


FIGURE 9. Small-signal emitter to collector on set voltage test circuit.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be ≤ 10 ns, duty cycle ≤ 2 percent. The input pulse width shall be 200 ns.
2. Output monitored with an oscilloscope with the following characteristics: Z_{in} ≤ 1 MΩ, t_r ≤ 1 ns.

FIGURE 10. Pulse response test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN (see 1.2 and 6.5).

e. For acquisition of RHA designed devices, table II, subgroup 1 testing of group D is optional. If subgroup 1 testing is desired, it should be specified in the contract.

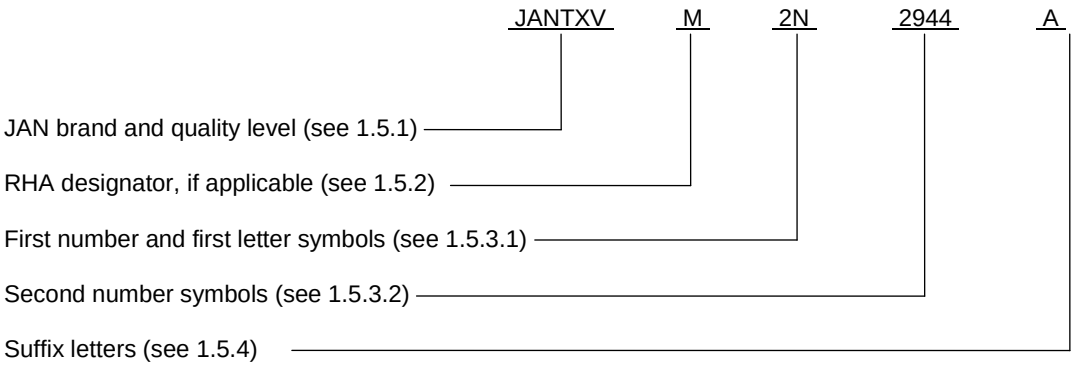
* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil .

6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCA2N2945) will be identified on the QML.

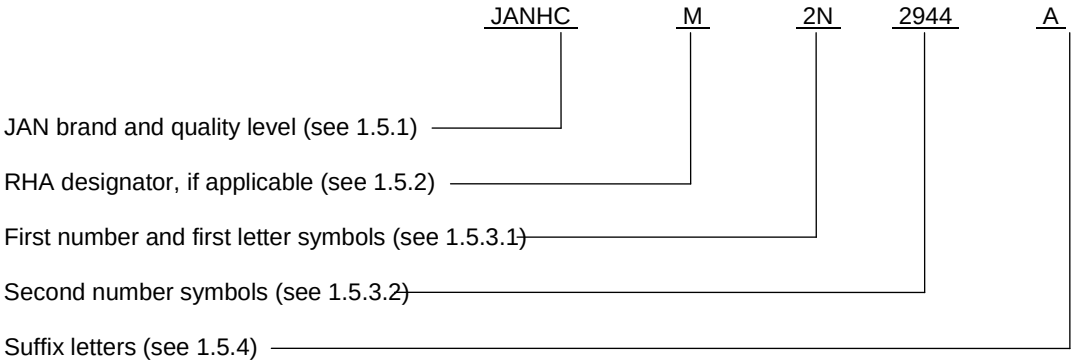
Die ordering information	
PIN	Manufacturer
	34156
2N2944A	JANHCA2N2944A, JANKCA2N2944A
2N2945A	JANHCA2N2945A, JANKCA2N2945A
2N2946A	JANHCA2N2946A, JANKCA2N2946A

* 6.5 PIN construction examples.

* 6.5.1 Encapsulated devices. The PIN for encapsulated devices are constructed using the following form:



6.5.2 Un-encapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



6.6 List of PINs.

6.6.1 Encapsulated devices. The following is a list of possible PINs available for encapsulated devices covered by this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)
JAN2N2944A	JANTX2N2944A	JANTXV2N2944A	JANTXV#2N2944A
JAN2N2944AM	JANTX2N2944AM	JANTXV2N2944AM	JANTXV#2N2944AM
JAN2N2944AUB	JANTX2N2944AUB	JANTXV2N2944AUB	JANTXV#2N2944AUB
JAN2N2944AUBM	JANTX2N2944AUBM	JANTXV2N2944AUBM	JANTXV#2N2944AUBM
JAN2N2945A	JANTX2N2945A	JANTXV2N2945A	JANTXV#2N2945A
JAN2N2945AM	JANTX2N2945AM	JANTXV2N2945AM	JANTXV#2N2945AM
JAN2N2945AUB	JANTX2N2945AUB	JANTXV2N2945AUB	JANTXV#2N2945AUB
JAN2N2945AUBM	JANTX2N2945AUBM	JANTXV2N2945AUBM	JANTXV#2N2945AUBM
JAN2N2946A	JANTX2N2946A	JANTXV2N2946A	JANTXV#2N2946A
JAN2N2946AM	JANTX2N2946AM	JANTXV2N2946AM	JANTXV#2N2946AM
JAN2N2946AUB	JANTX2N2946AUB	JANTXV2N2946AUB	JANTXV#2N2946AUB
JAN2N2946AUBM	JANTX2N2946AUBM	JANTXV2N2946AUBM	JANTXV#2N2946AUBM

6.6.1 Encapsulated devices - continued.

PINs for devices of the “S” quality level	PINs for devices of the “S” quality leve with RHA (1)l
JANS2N944A	JANS#2N2944A
JANS2N944AM	JANS#2N2944AM
JANS2N944AUB	JANS#2N2944AUB
JANS2N944AUBM	JANS#2N2944AUBM
JANS2N945A	JANS#2N2945A
JANS2N945AM	JANS#2N2945AM
JANS2N944AUBM	JANS#2N2945AUB
JANS2N944AUBM	JANS#2N2945AUBM
JANS2N945A	JANS#2N2946A
JANS2N946AM	JANS#2N2946AM
JANS2N946AUB	JANS#2N2946AUB
JANS2N946AUMB	JANS#2N2946AUBM

(1) The number sign (#) represents one of eight RHA designators available (“M”, “D”, “P”, “L”, “R”, “F”, “G”, or “H”).

6.6.2 Unencapsulated devices. The following is a list of possible PINs available for unencapsulated devices covered by this specification sheet.

JANHCA#2N944A	JANHCA#2N945A	JANHCA#2N946A
JANKCA#2N944A	JANKCA#2N945A	JANKCA#2N2946A

(1) The number sign (#) represents one of eight RHA designators available (“M”, “D”, “P”, “L”, “R”, “F”, “G”, or “H”).

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - AV, MI
Air Force - 19, 71, 99

Preparing activity:
DLA - CC

(Project 5961-2015-044)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.

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