GS12141

12G UHD-SDI Retiming Adaptive Cable Equalizer

Key Features

- 75Ω cable input interface with on-chip termination
- SMPTE ST 2082-1, ST 2081-1, ST 424, ST 292-1 and ST 259 compliant input/output
- Multi-standard operation from 1Mb/s to 11.88Gb/s
- In addition to standard SMPTE rates, the device also supports re-timing of DVB-ASI at 270Mb/s, and MADI at 125Mb/s
- Automatic cable equalization. Typical equalized cable lengths of Belden 1694A cable:
  - 70m at 11.88Gb/s
  - 90m at 5.94Gb/s
  - 180m at 2.97Gb/s
  - 240m at 1.485Gb/s
  - 400m at 270Mb/s
- Cable equalizer mode features:
  - Programmable carrier detect with squelch threshold adjustment
  - Manual and automatic cable equalizer bypass
- Trace driver features:
- Integrated 100Ω, differential output termination
  - DC-coupling from 1.2V to 2.5V CML logic
  - Trace driver data output pre-emphasis to compensate for up to 20" FR4 at 11.88Gb/s
  - Manual or automatic re-timer bypass
  - Manual or automatic Mute or disable on LOS
- CDR features:
  - Manual or automatic rate modes
  - Wide Loop bandwidth control
  - Re-timing at the following data rates: 125Mb/s, 270Mb/s, 1.485Gb/s, 2.97Gb/s, 5.94Gb/s, 11.88Gb/s. This includes the f/1.001 rates.
- Single 1.8V power supply for analog and digital core
- 1.2V, 1.8V, or 2.5V for trace driver output supply
- GSPI serial control and monitoring interface
- Four configurable GPIO pins for control or status monitoring
- Wide operating temperature range: -40ºC to +85ºC
- Small 6mm x 4mm 40-pin QFN
- Pb-free/Halogen-free/RoHS and WEEE compliant package

Applications

Next Generation 3D / 2D HFR HDTV and 2K D-Cinema, UHDTV1 and 4K D-Cinema end-equipment: Cameras, Monitors, Switchers, etc.

Next Generation 3G, 6G, and 12G UHD-SDI infrastructures designed in support of UHDTV1, UHDTV2, 4K D-Cinema and 3D HFR and HDR production image formats.

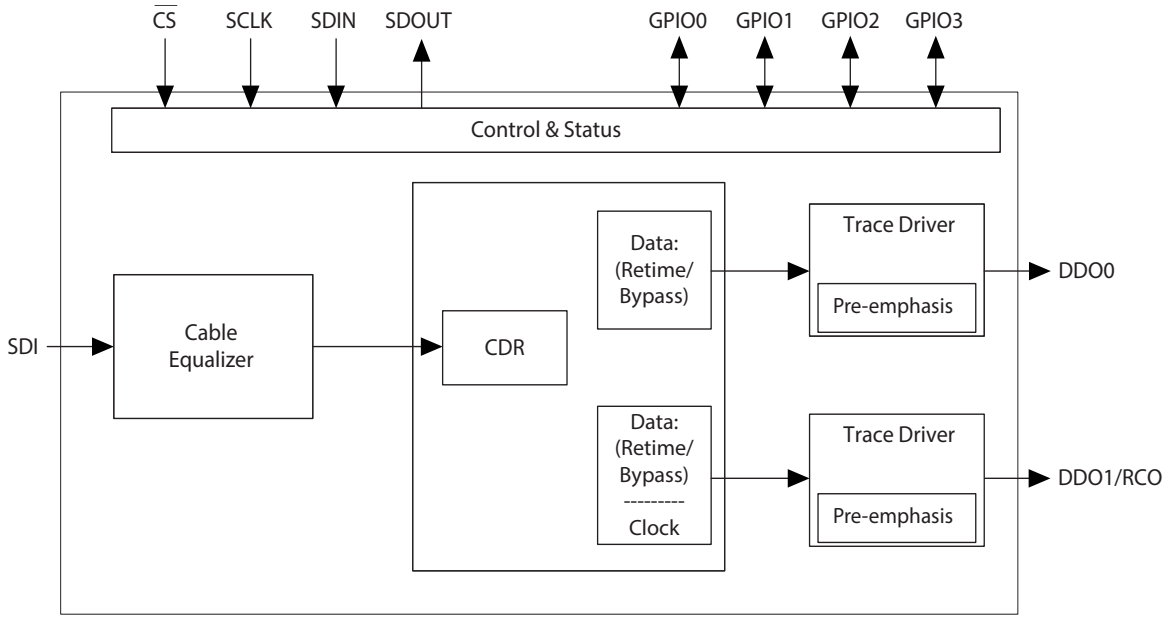
Description

The GS12141 is a low-power, multi-rate re-timing Cable Equalizer supporting rates up to 12G UHD-SDI. It is designed to equalize and restore signals received over 70m coaxial cable at 12G, compensate for DC content of SMPTE pathological signals, and re-time the incoming data. The device supports SMPTE ST 2082-1 (12G UHD-SDI), ST 2081-1 (6G UHD-SDI), ST 424 (3G SDI), ST 292-1 (HD-SDI), and ST 259 (SD-SDI) signals and is optimized for performance at 11.88Gb/s. In addition to standard SMPTE rates, the device also supports re-timing of DVB-ASI at 270Mb/s, and MADI at 125Mb/s.

The two trace drivers have highly configurable pre-emphasis and swing controls to compensate for long trace and connector losses.

Since the GS12141 is a re-timing equalizer, extremely low output jitter is achievable even at extended cable lengths. Typical jitter performance versus cable length is as follows:

- 70m at 11.88Gb/s: <0.2UI output jitter
- 90m at 5.94Gb/s: <0.15UI output jitter
- 180m at 2.97Gb/s: <0.1UI output jitter
- 240m at 1.485Gb/s: <0.1UI output jitter
- 400m at 270Mb/s: <0.1UI output jitter



GS12141 Functional Block Diagram

Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
8	041683	—	June 2018	Updated environmental declaration and Table 7-2: Ordering Information.
7	033520	—	October 2016	PLL_LOOP_ BANDWIDTH_ SD_MADI had CFG_PLL_LBW_SD parameter's reset value updated from "8" to "1C".
6	033432	—	September 2016	Removed External Reference Clock section. Updated schematic and block diagrams.
5	032340	—	July 2016	Minor formatting updates performed throughout document.
4	030855	—	June 2016	Updated from Draft to Preliminary Data Sheet.
3	028156	—	October 2015	Correction to document referenced in Section 5. Updated Figure 4-6 and Figure 4-7. Minor updates throughout.
2	026806	—	July 2015	Removed all references to Eye Monitor and PRBS Generator/Checker throughout document.
1	025089	—	May 2015	Many changes throughout document.
0	022342	—	February 2015	New Document.

Contents

1. Pin Out

1.1 GS12141 Pin Assignment

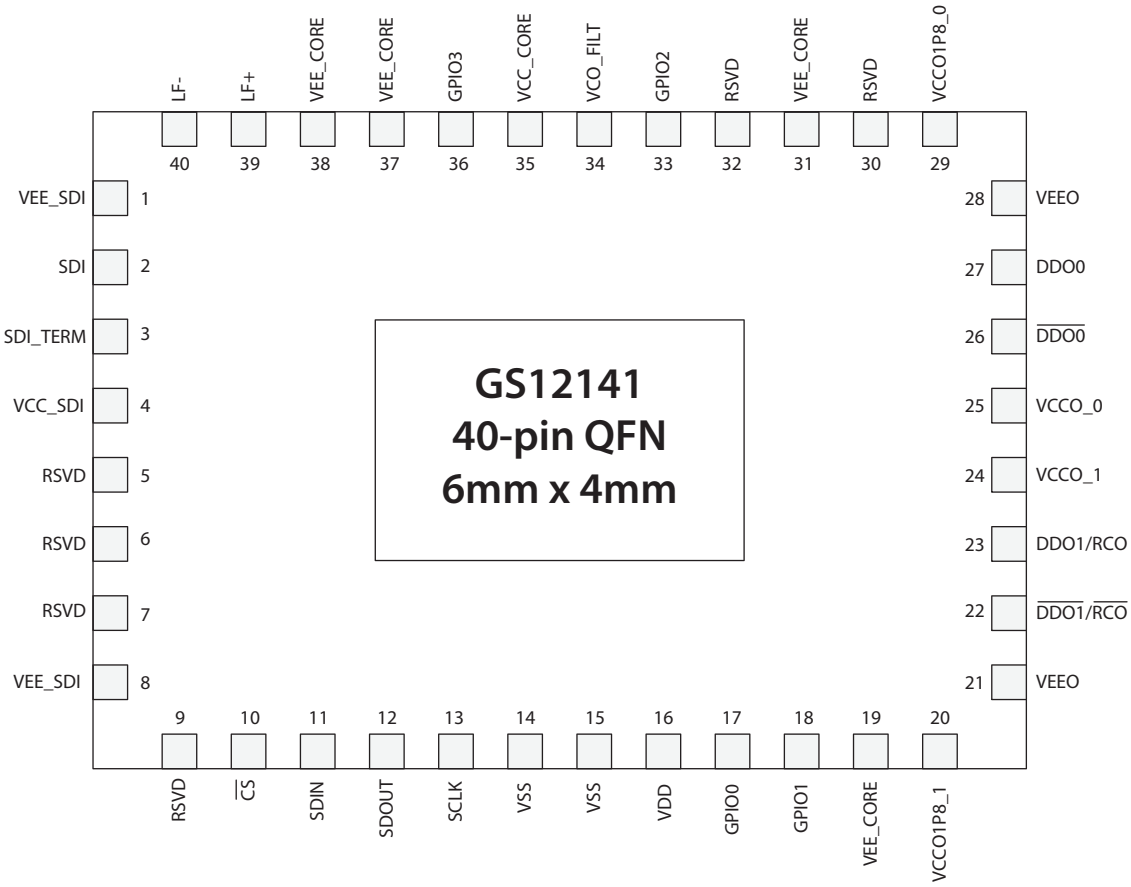


Figure 1-1: GS12141 Pin Assignment

1.2 GS12141 Pin Descriptions

Table 1-1: GS12141 Pin Descriptions

Pin Number	Name	Type	Description
1, 8	VEE_SDI	Power	Most negative power supply connection for the Cable Equalizer. Connect to GND.
2	SDI	Input	Single-ended CML input with internal 75Ω termination on SDI.
3	SDI_TERM	—	Input Common Mode termination. Decouple to GND through 2Ω resistor and 4.7uF capacitor.
4	VCC_SDI	Power	Most positive power supply connection for the Cable Equalizer. Connect to 1.8V.

Table 1-1: GS12141 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
5, 6, 7, 9, 30, 32	RSVD	—	These pins may be left floating or connected to GND. Contact FAE for additional information on circuit compatibility with the GS12241 and GS12242.
10	$\overline{CS}$	Digital Input	Chip Select input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-up. Active-LOW input. Refer to Section 4.5.1 for more details.
11	SDIN	Digital Input	Serial digital data input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.5.2 for more details.
12	SDOUT	Digital Output	Serial digital data output for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS output. Active-HIGH output. Refer to Section 4.5.3 for more details.
13	SCLK	Digital Input	Burst-mode clock input for the Gennum Serial Peripheral Interface (GSPI) host control/status port. 1.8V CMOS input with 100kΩ pull-down. Refer to Section 4.5.4 for more details.
14, 15	VSS	Power	Most negative power supply for digital core logic. Connect to GND.
16	VDD	Power	Most positive power supply connection for digital core logic. Connect to 1.8V.
17	GPIO0	Digital Input/Output	Multi-function Control/Status Input/Output 0. Default function: Direction = Output Signal = High indicates LOS (Loss of Signal, inverse of Carrier Detect) Pin is 1.8V CMOS I/O, please refer to GPIO0_CFG for more information on how to configure GPIO0.
18	GPIO1	Digital Input/Output	Multi-function Control/Status Input/Output 1. Default function: Direction = Output Signal = High indicates PLL is locked Pin is 1.8V CMOS I/O, please refer to GPIO1_CFG for more information on how to configure GPIO1.
19, 31, 37, 38	VEE_CORE	Power	Most negative power supply connection for the analog core. Connect to GND.
20, 29, 35	VCC_CORE, VCCO1P8_0, VCCO1P8_1	Power	Most positive power supply connection for the analog core. Connect to 1.8V.

Table 1-1: GS12141 Pin Descriptions (Continued)

Pin Number	Name	Type	Description
21, 28	VEEO	Power	Most negative power supply connection for the output drivers. Connect to GND.
22, 23	$\overline{\text{DDO1}}$/$\overline{\text{RCO}}$, DDO1/RCO	Output	Second differential output or differential clock output divided by 2. Differential CML output with two internal 50Ω pull-ups. If both outputs are unused, they can be left floating and disabled through the host interface.
24	VCCO_1	Power	Most positive power supply connection for the DDO1/RCO/ $\overline{\text{DDO1}}$/$\overline{\text{RCO}}$ output driver. Connect to 1.2V – 2.5V.
25	VCCO_0	Power	Most positive power supply connection for the DDO0/$\overline{\text{DDO0}}$ output driver. Connect to 1.2V – 2.5V.
26, 27	$\overline{\text{DDO0}}$, DDO0	Output	Differential serial digital outputs. Differential CML output with two internal 50Ω pull-ups. If both outputs are unused, they can be left floating and disabled through the host interface.
33	GPIO2	Digital Input/Output	Multi-function Control/Status Input/Output 2. **Note:** The default signal option is not active on this version of the device, but will be Sleep control on future devices. Pin is 1.8V CMOS I/O, please refer to GPIO2_CFG for more information on how to configure GPIO2.
34	VCO_FILT	Passive	VCO filter capacitor connection. Decouple to ground through 1uF capacitor.
36	GPIO3	Digital Input/Output	Multi-function Control/Status Input/Output 3. Default function: Direction = Input Signal = Set high to disable DDO1 Pin is 1.8V CMOS I/O, please refer to GPIO3_CFG for more information on how to configure GPIO3.
39	LF+	Passive	Loop filter capacitor connection. Connect to pin 40 through 470nF capacitor.
40	LF-	Passive	Loop filter capacitor connection. Connect to pin 39 through 470nF capacitor.
Tab	—	—	Central paddle can be connected to ground or left unconnected. Its purpose is to provide increased mechanical stability. It is not required for thermal dissipation.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value
Supply Voltage - Core (VCC_SDI, VCC_CORE, VDD)	-0.5V to +2.2V
Supply Voltage - Output Driver (VCCO_0, VCCO_1)	-0.5V to +2.8V
Input ESD Voltage (any pin)	2kV HBM
Storage Temperature Range (T_S)	-50°C to +125°C
Input Voltage Range (SDI, $\overline{SDI}$)	-0.3 to (VCC_SDI +0.3)V
Input Voltage Range (GPIO2, GPIO3)	-0.3 to (VCC_CORE +0.3)V
Input Voltage Range ($\overline{CS}$, SDIN, SCLK, VSS, VDD, GPIO0, GPIO1)	-0.3 to (VDD +0.3)V
Solder Reflow Temperature	260°C

Note: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation outside of the ranges shown in the AC/DC electrical characteristics tables is not guaranteed.

2.2 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

VCC_SDI, VCC_CORE, VDD, VCCO_0, VCCO_1, VCCO_0, VCCO_1 = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	VCC_SDI, VCC_CORE, VDD		1.71	1.8	1.89	V	—
Supply Voltage - Output Driver	VCCO_0, VCCO_1		1.14	1.2	1.26	V	—
			1.71	1.8	1.89	V	—
			2.38	2.5	2.63	V	—
Power	P_D	VCCO = 1.2V, Output Swing = 400mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ enabled, DDO1/$\overline{\text{DDO1}}$ disabled	—	348	—	mW	1
		VCCO = 1.8V, Output Swing = 400mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ enabled, DDO1/$\overline{\text{DDO1}}$ disabled	—	355	—	mW	1
		VCCO = 1.8V, Output Swing = 800mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ enabled, DDO1/$\overline{\text{DDO1}}$ disabled	—	373	—	mW	1
		VCCO = 2.5V, Output Swing = 400mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ enabled, DDO1/$\overline{\text{DDO1}}$ disabled	—	362	—	mW	1
		VCCO = 2.5V, Output Swing = 800mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ enabled, DDO1/$\overline{\text{DDO1}}$ disabled	—	387	—	mW	1
		VCCO = 1.2V, Output Swing = 400mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ and DDO1/$\overline{\text{DDO1}}$ enabled	—	398	—	mW	1
		VCCO = 1.8V, Output Swing = 400mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ and DDO1/$\overline{\text{DDO1}}$ enabled	—	410	—	mW	1
		VCCO = 1.8V, Output Swing = 800mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ and DDO1/$\overline{\text{DDO1}}$ enabled	—	446	—	mW	1

Table 2-2: DC Electrical Characteristics (Continued)

VCC_SDI, VCC_CORE, VDD, VCCO_0, VCCO_1, VCCO_0, VCCO_1 = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Power	P_D	VCCO = 2.5V, Output Swing = 400mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ and DDO1/$\overline{\text{DDO1}}$ enabled	—	424	—	mW	1
		VCCO = 2.5V, Output Swing = 800mV$_{ppd}$, DDO0/$\overline{\text{DDO0}}$ and DDO1/$\overline{\text{DDO1}}$ enabled	—	474	—	mW	1
		DDO0/$\overline{\text{DDO0}}$ and DDO1/$\overline{\text{DDO1}}$ disabled	—	214	—	mW	—
Supply Current - Trace Driver	I_{CCO_0}, I_{CCO_1}	VCCO = 1.2V, Output Swing = 400mV$_{ppd}$,	—	10	16	mA	1
		VCCO = 1.8V, Output Swing = 400mV$_{ppd}$,	—	10	16	mA	1
		VCCO = 1.8V, Output Swing = 800mV$_{ppd}$,	—	20	30	mA	1
		VCCO = 2.5V, Output Swing = 400mV$_{ppd}$,	—	10	16	mA	1
		VCCO = 2.5V, Output Swing = 800mV$_{ppd}$,	—	20	30	mA	1
Supply Current – Analog Core	I_{CC_CORE}	DDO0/$\overline{\text{DDO0}}$ and DDO1/$\overline{\text{DDO1}}$ disabled	—	106	123	mA	—
		DDO0/$\overline{\text{DDO0}}$ enabled and DDO1/$\overline{\text{DDO1}}$ disabled	—	127	151	mA	—
		DDO0/$\overline{\text{DDO0}}$ and DDO1/$\overline{\text{DDO1}}$ enabled	—	148	173	mA	—
Supply Current - Cable Equalizer	I_{CC_SDI}		—	45	58	mA	—
Supply Current - Digital Logic	I_{DD}		—	15	17	mA	—
Serial Input Common Mode Voltage	V_{CMIN}		1.4	—	1.6	V	—
Serial Output Common Mode Voltage	V_{CMOUT}		—	$V_{CMOUT} = V_{CCO} - \Delta V_{DDO}/2$	—	—	—
Serial Output Termination		Differential	—	100	—	Ω	—
Serial Input Termination		Between SDI and $\overline{\text{SDI}}$ pins	—	75	—	Ω	—
Input Voltage - Digital Pins ($\overline{\text{CS}}$, SDIN, SCLK, GPIO[0:3])	V_{IH}		0.65* VDD	—	VDD	V	—
	V_{IL}		0	—	0.35* VDD	V	—

Table 2-2: DC Electrical Characteristics (Continued)

VCC_SDI, VCC_CORE, VDD, VCCO_0, VCCO_1, VCCO_0, VCCO_1 = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output Voltage - Digital Pins (SDOUT, GPIO[0:3])	V_{OH}	I_{OH} = -5mA	VDD - 0.45	—	—	V	—
	V_{OL}	I_{OL} = +5mA	—	—	0.45	V	—

Notes:

1. Pre-emphasis is disabled.

2.3 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

VCC_SDI, VCC_CORE, VDD, VCCO_0, VCCO_1, VCCO_0, VCCO_1 = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial Input Data Rate	DR_{SDI}	—	0.001	—	11.88	Gb/s	—
Upstream Launch Swing	ΔV_{SDI}	1.485Gb/s	720	800	960	mV_{ppd}	—
		270Mb/s, 270Mb/s, 2.97Gb/s, 5.94Gb/s, 11.88Gb/s	720	800	880	mV_{ppd}	4
Output Voltage Swing	ΔV_{DDO}		200	—	800	mV_{ppd}	—
Intrinsic Input Jitter Tolerance	IIJT	12G	0.7	0.85	—	UI	5
		MADI/SD/HS/3G/6G	0.8	0.95	—	UI	5
PLL Lock Time – Asynchronous	t_{ALOCK}		—	75	—	ms	1
PLL Lock Time – Synchronous	t_{SLOCK}	SD	—	—	10	µs	—
		HD/3G/UHD	—	—	2	µs	—
DDO0, $\overline{DDO0}$, DDO1/RCO, $\overline{DDO1/RCO}$ Rise/Fall Time	$t_{riseDDO0}$, $t_{riseDDO1/RCO}$	20% – 80% rising edge into 50Ω load	—	—	40	ps	—
	$t_{fallDDO0}$, $t_{fallDDO1/RCO}$	20% – 80% falling edge into 50Ω load	—	—	40	ps	—
Mismatch in Rise/Fall Time			—	—	5	ps	—
Duty Cycle Distortion (DDO0, $\overline{DDO0}$, DDO1/RCO, $\overline{DDO1/RCO}$)			—	—	8	ps	—
Input Return Loss		5MHz to 1.485GHz	—	—	-15	dB	2
		1.485GHz to 2.97GHz	—	—	-10	dB	2
		2.97GHz to 5.94GHz	—	—	-7	dB	2
		5.94GHz to 11.88GHz	—	—	-4	dB	2
Serial Data Output Jitter	t_{OJ}	270Mb/s Belden 1694A: 400m	—	0.04	0.2	UI_{pp}	6
		1.485Gb/s Belden 1694A: 240m	—	0.07	0.18	UI_{pp}	3
		2.97Gb/s Belden 1694A: 180m	—	0.07	0.2	UI_{pp}	3
		5.94Gb/s Belden 1694A: 80m	—	0.07	0.15	UI_{pp}	3
		5.94Gb/s Belden 1694A: 90m	—	0.15	—	UI_{pp}	3
		11.88Gb/s Belden 1694A: 70m	—	—	0.2	UI_{pp}	3

Table 2-3: AC Electrical Characteristics (Continued)

VCC_SDI, VCC_CORE, VDD, VCCO_0, VCCO_1, VCCO_0, VCCO_1 = +1.8V ±5%, T_A = -40°C to +85°C, unless otherwise shown.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
PLL Loop Bandwidth	$BW_{LOOP(125Mb/s)}$	Setting 0.0625x	—	5	—	kHz	—
		Setting 0.125x	—	10	—	kHz	—
		Setting 0.25x	—	19	—	kHz	—
		Setting 0.5x (Default)	—	38	—	kHz	—
		Setting 1.0x	—	75	—	kHz	—
	$BW_{LOOP(270Mb/s)}$	Setting 0.0625x	—	10	—	kHz	—
		Setting 0.125x	—	20	—	kHz	—
		Setting 0.25x	—	40	—	kHz	—
		Setting 0.5x	—	80	—	kHz	—
		Setting 1.0x (Default)	—	158	—	kHz	—
	$BW_{LOOP(1.485Gb/s)}$	Setting 0.0625x	—	55	—	kHz	—
		Setting 0.125x	—	110	—	kHz	—
		Setting 0.25x	—	220	—	kHz	—
		Setting 0.5x (Default)	—	438	—	kHz	—
		Setting 1.0x	—	875	—	kHz	—
	$BW_{LOOP(2.97Gb/s)}$	Setting 0.0625x	—	110	—	kHz	—
		Setting 0.125x	—	220	—	kHz	—
		Setting 0.25x	—	440	—	kHz	—
		Setting 0.5x (Default)	—	0.88	—	MHz	—
		Setting 1.0x	—	1.75	—	MHz	—
	$BW_{LOOP(5.94Gb/s)}$	Setting 0.0625x	—	220	—	kHz	—
		Setting 0.125x	—	440	—	kHz	—
		Setting 0.25x	—	0.88	—	MHz	—
		Setting 0.5x (Default)	—	1.75	—	MHz	—
		Setting 1.0x	—	3.5	—	MHz	—
	$BW_{LOOP(11.88Gb/s)}$	Setting 0.0625x	—	440	—	kHz	—
		Setting 0.125x	—	0.88	—	MHz	—
		Setting 0.25x	—	1.75	—	MHz	—
		Setting 0.5x (Default)	—	3.5	—	MHz	—
		Setting 1.0x	—	7.0	—	MHz	—

Notes:

1. Asynchronous lock time with MADI disabled.
2. Values achieved with Semtech evaluation board and connector.
3. Measured using a clean input source.
4. Default value for **CFG_EQ_INPUT_LAUNCH_SWING_COMP** parameter in control register 0x18. The default parameter value is 80d (50h).
5. Square-wave modulated jitter.
6. Max Output jitter as low as 0.12UI can be achieved by setting the low SD output jitter mode in register 0x737D.

3. Input/Output Circuits

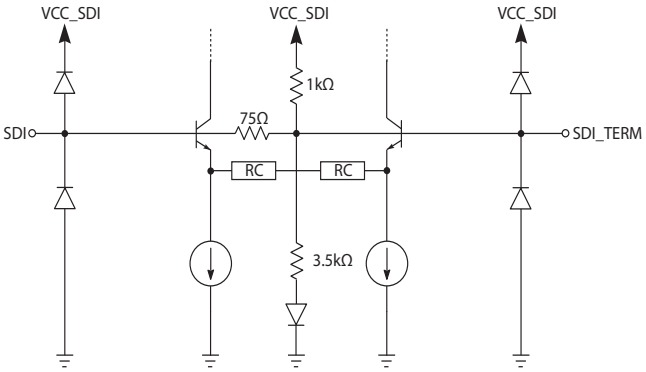


Figure 3-1: SDI, $\overline{\text{SDI}}$

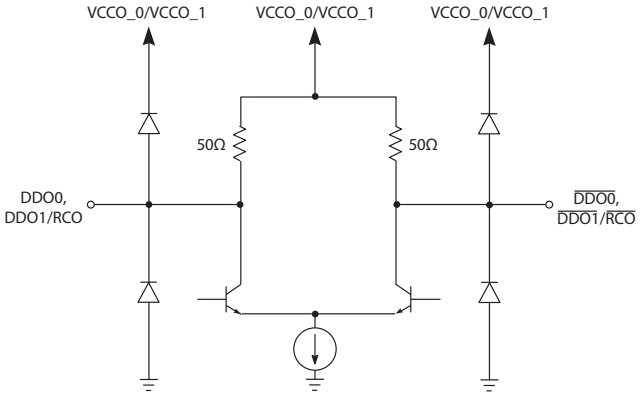


Figure 3-2: DDO0, $\overline{\text{DDO0}}$, DDO1/RCO, $\overline{\text{DDO1}}$/$\overline{\text{RCO}}$ Serial Data Output

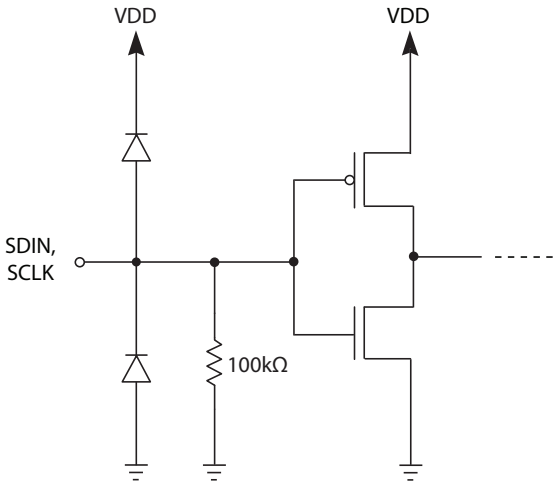


Figure 3-3: SDIN, SCLK

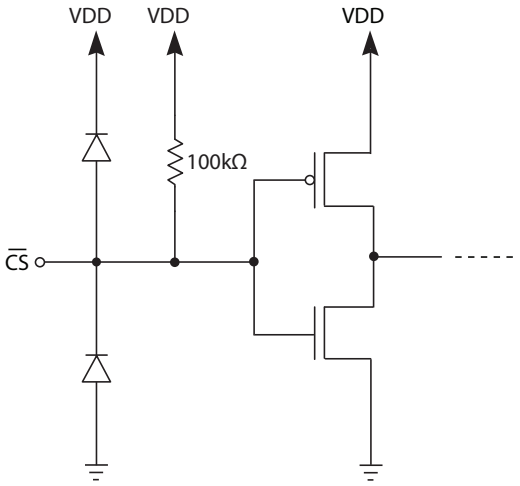


Figure 3-4: $\overline{\text{CS}}$

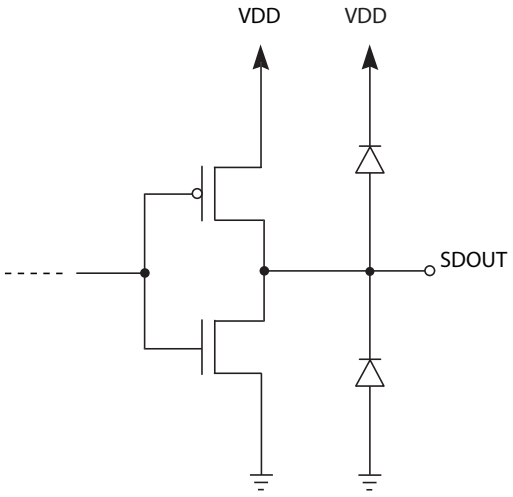


Figure 3-5: SDOUT

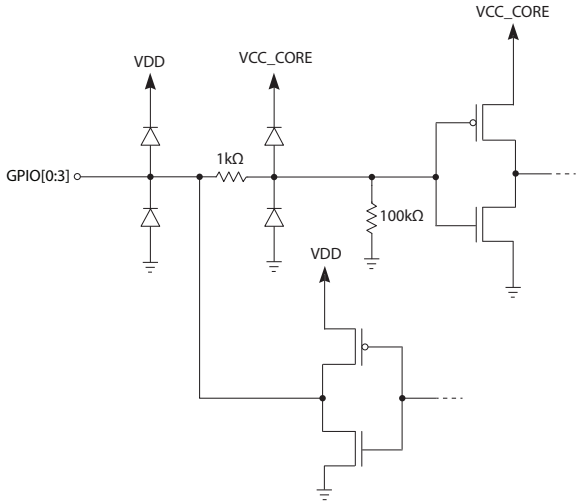


Figure 3-6: GPIO[0:3]

4. Detailed Description

4.1 Cable Equalizer

The GS12141 features internal 75Ω on-chip termination (see Figure 3-2) and can automatically adjust its gain to equalize and restore SMPTE compliant signals received over different lengths of coaxial cable having loss characteristics similar to Belden 8281 or 1694A. With the default settings, the device will automatically equalize MADI at 125Mb/s and most common SMPTE compliant signal between SD at 270Mb/s and UHD-SDI at 11.88Gb/s and bypass signals below 125Mb/s.

The GS12141 features programmable Launch Swing Compensation, squelch threshold adjust, and bypass, all of which can be set through the device's host interface.

The equalized or bypassed signal is then routed to the serial digital re-timer (CDR) block.

4.1.1 Cable Equalizer Bypass

With the default settings, the device will automatically bypass signals below 125Mb/s. During EQ-bypass mode, the device supports low data rate and slow edge signals such as SMPTE310 and AES3id. These signals will not be re-timed by the CDR block.

The following two methods allow the user to force the signal to bypass the equalization and DC restoration stages:

1. Via the host interface, by setting **CTRL_CEQ_AUTO_ BYPASS** to 0_b, and **CTRL_CEQ_MANUAL_ BYPASS** to 1_b in register 0x7317.
2. Via the GPIO[0:3] pin (see Section 4.4).

4.1.2 Upstream Launch Swing Compensation

The GS12141 has an automatic gain control circuit, that is optimized on the assumption that the Cable Driver in the upstream device is SMPTE compliant and has a launch swing of $800mV_{pp}$ ±10%. When the source amplitude is known to be non-SMPTE compliant, a compensation adjustment can be made in the GS12141. The GS12141 can adjust for launch swings in the range of 250mV to 1V in approximately $50mV_{ppd}$ increments. Upstream launch swing compensation can be adjusted through the **CFG_EQ_INPUT_LAUNCH_SWING_COMP** parameter in control register 0x7318. The default parameter value is 80_d (50_h), which corresponds to a nominal launch swing of $800mV_{ppd}$.

4.1.3 Carrier Detect, Squelch Control, and Loss of Signal

The GS12141 has highly configurable carrier detection and squelching capability. The carrier detection can be made more robust against spurious noise at the inputs and the squelch control can be configured and enabled to reduce false outputs to low level signals such as crosstalk.

The GS12141 reports two separate carrier detects in the **STAT_PRI_CD** and **STAT_SEC_CD** parameters in register 0x7387. The **STAT_PRI_CD** parameter is the filtered carrier detect of the analog carrier detect signal, and when HIGH indicates a valid signal that meets the configured settings. The **STAT_SEC_CD** parameter can be further filtered by the squelch settings. LOS is the complement of the **STAT_SEC_CD** signal, and serves as the control signal for Mute on LOS and Disable on LOS, which will be covered in the output Section 4.3.5.

The stability of **STAT_PRI_CD** can be increased by filtering out longer transients or glitches. This can be achieved by increasing the sampling window over which the signal is sampled and the number of samples required to assert or de-assert it. There are three configuration parameters that provide control over the **STAT_PRI_CD** filter. The sampling window can be configured through the **CFG_CD_FILTER_SAMPLE_WIN** parameter in register 0x7321. The default power-up value of **CFG_CD_FILTER_SAMPLE_WIN** is the minimum allowed value of 3_d. The number of samples to assert or de-assert can be set through the **CFG_CD_FILTER_DEASSERT_CNT** and **CFG_CD_FILTER_ASSERT_CNT** parameters in register 0x7321 and 0x7322. The default power-up values are 15_d and 1023_d respectively. With the default power-up values, the **STAT_PRI_CD** de-assert time is ~200µs and the **STAT_PRI_CD** assert time is ~6.6µs.

To determine the **STAT_PRI_CD** assert and de-assert times, use the following equations:

The **STAT_PRI_CD** de-assert time is:

~100µs + (1.6µs) * (**CFG_CD_FILTER_SAMPLE_WIN** + 1) * **CFG_CD_FILTER_DEASSERT_CNT**

The STAT_PRI_CD assert time is:

(1.6µs) * (**CFG_CD_FILTER_SAMPLE_WIN** + 1) * **CFG_CD_FILTER_ASSERT_CNT**

As previously mentioned, the **STAT_SEC_CD** parameter can be further filtered by the squelch settings. The squelch settings can be set in the **CFG_CLI_SQUELCH_THRESHOLD** and **CFG_CLI_SQUELCH_HYSTERESIS** parameters in register 0x7316.

The squelch level can adjusted through the **CFG_CLI_SQUELCH_THRESHOLD** parameter to any value between 0_d and 64_d, where 64_d is the default value, and results in max cable reach. The hysteresis can be adjusted through the **CFG_CLI_SQUELCH_HYSTERESIS** parameter to any value between 0_d and 30_d, where 2_d is the default value, and 0_d means minimum hysteresis.

With the squelch threshold set in the **SQUELCH_PARAMETERS** register and secondary carrier detect gating enabled in the **CFG_SEC_CD_INCL_CLI_SQUELCH** register, the secondary carrier detect will be set to 0_b and the LOS will be set to 1b whenever the signal at the input does not pass the threshold. The result is that the device will not indicate lock, and the outputs will mute, assuming Mute on LOS is left to its default value in the **CONTROL_OUTPUT_MUTE** register (0x7349). See Section 4.3 for more details.

4.1.4 Equalizer Control and Status Parameters Summary

Table 4-1 and Table 4-2 list the most commonly used control and status parameters of the Equalizer block. For a complete list of registers and functions, please see Section 5.

Table 4-1: Equalizer Block Control Parameters

$Address_h$	Bit Slice	Parameter Name	Description
0x7315	0:0	CFG_SEC_CD_INCL_CLI_SQUELCH	When set HIGH, enables gating of LOS by the **SQUELCH_PARAMETERS** in register 0x7316.
0x7316	14:8	CFG_CLI_SQUELCH_THRESHOLD	Sets the Squelch threshold.
	6:0	CFG_CLI_SQUELCH_HYSTERSIS	Sets the Squelch threshold Hysteresis.
0x7317	1:1	CTRL_CEQ_MANUAL_BYPASS	Enables manual bypass of Equalizer Core when **CTRL_CEQ_AUTO_BYPASS** is 0_b.
	0:0	CTRL_CEQ_AUTO_BYPASS	Sets or disables the automatic bypass mode of the Equalizer Block.
0x7318	6:0	CFG_EQ_INPUT_LAUNCH_SWING_COMP	Sets the Launch Swing Compensation of the Equalizer.
0x7320	7:0	CFG_CD_FILTER_SAMPLE_WIN	Carrier Detect sample window period. (value+2)*1.6µs
0x7321	9:0	CFG_CD_FILTER_DEASSERT_CNT	Number of samples for detecting carrier detection de-assertion.
0x7322	9:0	CFG_CD_FILTER_ASSERT_CNT	Number of samples for detecting carrier detection assertion.

Table 4-2: Equalizer Block Status Registers

$Address_h$	Bit Slice	Parameter Name	Description
0x7384	15:8	STAT_CNT_PRI_CD_CHANGES	A counter showing the number of times the primary Carrier Detect signal changed.
	7:0	STAT_CNT_SEC_CD_CHANGES	A counter showing the number of times the secondary Carrier Detect signal changed.
0x7386	8:8	STAT_CLI_SQUELCH	The Squelch status.
0x7387	9:9	STAT_SEC_CD	The secondary Carrier Detect status.
	8:8	STAT_PRI_CD	The primary Carrier Detect status.

4.2 Serial Digital Re-timer (CDR)

The GS12141 includes an integrated CDR, whose purpose is to lock to a valid incoming signal from the cable equalizer stage and produce a lower jitter signal at the trace driver outputs DDO0 and DDO1. The CDR will attempt to lock to any of the following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), 3G-SDI (2.97Gb/s), 6G-SDI (5.94Gb/s) and 12G-SDI (11.88Gb/s). This includes the f/1.001 rates.

The default settings of the re-timer block are optimal for most applications. However, the following controls allow the user to customize the behaviour of the re-timer: LBW control, Automatic and Manual Rate Detection.

4.2.1 PLL Loop Bandwidth Control

The ratio of output peak-to-peak jitter to input peak-to-peak jitter of the CDR can be represented by a low-pass jitter transfer function, with a bandwidth equal to the PLL LBW. Although the default LBW settings for the GS12141 CDR are ideal for most SDI signals, the GS12141 allows the user to adjust the LBW for each MADI and SMPTE compliant rate.

Registers 0x730A through 0x730C contain the following parameters which allow the user to configure rate dependent LBW: **CFG_PLL_LBW_12G**, **CFG_PLL_LBW_6G**, **CFG_PLL_LBW_3G**, **CFG_PLL_LBW_HD**, **CFG_PLL_LBW_SD**, and **CFG_PLL_LBW_MADI**. The LBW settings are defined in terms of ratios of the nominal LBW. For each rate, where '1.0x' is the nominal LBW, the following ratios are available: 0.0625x, 0.125x, 0.25x, 0.5x, and 1.0x. Table 2-3 provides the specific loop bandwidths for each data rate and LBW setting. Lowering the LBW will lower the jitter amplitude above the LBW frequency. Although lower output jitter is desirable, the lower LBW may reduce the device's IJT to very high jitter that may be present outside the LBW.

4.2.2 Automatic and Manual Rate Detection

With the default rate detect setting, the CDR will automatically attempt to lock to any of following data rates: MADI (125Mb/s), SD-SDI (270Mb/s), HD-SDI (1.485Gb/s), 3G-SDI (2.97Gb/s), 6G-SDI (5.94Gb/s) and 12G-SDI (11.88Gb/s). This includes the f/1.001 rates. However, the CDR can be forced to only lock to a single rate by setting the **CFG_AUTO_RATE_DETECT_ENA** and **CFG_MANUAL_RATE** parameters in register 0x7306 to 0_b and 1_b respectively.

The **STAT_LOCK** parameter in register 0x7386 will indicate that the CDR is locked when its value is 1_b and unlocked when its value is 0_b. The lock status can also be monitored externally on GPIO1, which is the default power-up configuration for pin 18. The **STAT_DETECTED_RATE** parameter in register 0x7387 will indicate the data rate at which the CDR is locked to. A value of 0_d in the **STAT_DETECTED_RATE** parameter indicates that the device is not locked, while values between 1_d and 6_d will in indicate that the device is locked to one of the six available rates between MADI at 125Mb/s and UHD-SDI at 11.88Gb/s.

Table 4-3: Detected Data Rates

STAT_DETECTED_RATE [2:0]	Detected Data Rate
0	Unlocked
1	MADI (125Mb/s)
2	SD (270Mb/s)
3	HD (1.485Gb/s)
4	3G (2.97Gb/s)
5	6G (5.94Gb/s)
6	12G (11.88Gb/s)
7	Reserved

If the CDR cannot lock to any of the valid rates in automatic mode or the selected rate in manual mode, the signal will automatically be bypassed to the output. If the CDR does lock to the incoming signal, the re-timed and bypassed (if manual bypass control enabled) signals are available independently at each output. See the Output Driver Section 4.3.1 for more details.

4.2.3 Lock Time

4.2.3.1 Synchronous and Asynchronous Lock Time

Synchronous lock time is defined as the time it takes the device to re-lock to an existing signal that has been momentarily interrupted or to a new signal of the same data rate as the previous signal which has been quickly switched in.

Asynchronous lock time is defined as the time it takes the device to lock when a signal is first applied to the serial digital inputs, or when the signal rate changes.

The asynchronous and synchronous lock times are defined in Table 2-3.

Note: To ensure synchronous lock times are met, the maximum interruption time of the signal is 10µs for an SD SDI signal. HD, 3G, 6G, or 12G signals must have a maximum interruption time of 6µs. The new signal, after interruption, must have the same frequency as the original signal but may have an arbitrary phase.

4.2.3.2 CDR Control and Status Parameters Summary

Table 4-4 and Table 4-5 list the most commonly used control and status parameters of the CDR block. For a complete list of registers and functions, please see Section 5.

Table 4-4: CDR Control Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x7306	4:1	CFG_MANUAL_RATE	Select a single rate for CDR rate detection when **CFG_AUTO_RATE_DETECT_ENA** is 0_b.
	0:0	CFG_AUTO_RATE_DETECT_ENA	Sets or disables the automatic rate detection mode of the CDR.
0x730A	12:8	CFG_PLL_LBW_12G	Set the LBW for 12G signals.
	4:0	CFG_PLL_LBW_6G	Set the LBW for 6G signals.
0x730B	12:8	CFG_PLL_LBW_3G	Set the LBW for 3G signals.
	4:0	CFG_PLL_LBW_HD	Set the LBW for HD signals.
0x730C	12:8	CFG_PLL_LBW_SD	Set the LBW for SD signals.
	4:0	CFG_PLL_LBW_MADI	Set the LBW for MADI signals.
0x7311	8:8	CFG_GPIO1_OUTPUT_ ENA	Sets the GPIO pin as either an output or an input.
	7:0	CFG_GPIO1_FUNCTION	Lock Status (default)

Table 4-5: CDR Status Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x7385	15:8	STAT_CNT_RATE_CHANGES	Counter showing the number of times the PLL lock rate changed.
	7:0	STAT_CNT_PLL_LOCK_CHANGES	Counter showing the number of times the PLL lock status changed.
0x7386	12:12	STAT_LOCK	The status of the PLL. Locked, or unlocked.
0x7387	2:0	STAT_DETECTED_RATE	The rate at which the PLL is locked to.

4.3 Output Trace Drivers

The GS12141 features two independent 100Ω internally terminated differential trace drivers (see Figure 3-2), with data available on the first output, SDO0, while clock and data are available on the second output, SDO1. The trace drivers feature highly configurable amplitude and pre-emphasis control, which can compensate for up to 20 inches of 7-mil stripline in standard FR4 at 11.88Gb/s. The LOS (Loss of Signal) status from the equalizer stage and Loss of Lock status from the CDR block can both be used to automatically mute or disable the outputs when asserted.

4.3.1 Bypassed Re-timer Signal Output Control

With the default power-up settings, the GS12141 outputs will automatically switch to the bypassed signal (non-re-timed) whenever the PLL is unlocked. Alternatively, manual re-timer bypass may be configured by setting the **CTRL_OUTPUT<n>_RETIMER_AUTO_BYPASS** and **CTRL_OUTPUT<n>_RETIMER_MANUAL_BYPASS** parameters in register 0x734C to 0_b and 1_b respectively via the host interface, in which case the PLL will remain bypassed for all rates.

The re-timer bypass function, manual or automatic, does not affect the input equalization function of the device.

In manual bypass, the output signals of the device will not be retimed. Other features of the re-timer such as rate detect and lock detect are still accessible in this mode.

Please refer to Section 5. on how to change the re-timer bypass mode via the device's host interface.

Note: The <n> in the control parameter names refers to the output number.

4.3.2 Clock Out on DDO1

The GS12141 provides an optional clock output mode on DDO1. The clock is half of the detected data rate.

To set DDO1 to clock mode, write 1b to parameter **CTRL_OUTPUT1_SIGNAL_SEL** in register 0x7348. The default value of this bit is 0b (data mode).

4.3.3 Amplitude and Pre-emphasis Control

Each differential output can be configured in ≈45mV_{ppd} increments to drive up to 800mV_{ppd} into an external 100Ω differential load.

In some applications there may be significant HIGH frequency loss associated with long traces between the GS12141 output and a downstream device. With low-to-moderate loss, ISI jitter will be generated, which will reduce the system jitter budget. However, with HIGH loss, there may be complete eye closure at the downstream receiver.

At 11.88Gb/s, the pre-emphasis can compensate for up to 20" of 7-mil stripline in standard FR4. The default setting on power up can compensate for up to 3" of trace.

Most trace drivers that operate at HIGH data rates offer some amount of pre-emphasis to compensate for trace. However, the GS12141 allows the user to control the pre-emphasis pulse amplitude and the pre-emphasis pulse width. This extra flexibility provides a mechanism to better shape the pre-emphasis gain to match the frequency loss response of interconnect composed of trace, connector and via losses.

The output driver swing, pre-emphasis pulse amplitude, and pre-emphasis pulse width can be controlled through the **CFG_OUTPUT<n>_CD_SD_TD_DRIVER_SWING**, **CFG_OUTPUT<n>_CD_SD_TD_PREEMPH_AMPL**, and **CFG_OUTPUT<n>_CD_SD_TD_PREEMPH_WIDTH** parameters in registers 0x7328 through 0x732B, where <n> is the output number.

The DS (Driver Swing) parameter has 45 steps and the default value at power-up is 9 (approximately 450mV_{ppd}). To save power, the Driver Swing should be kept as low as possible while meeting the minimum sensitivity requirement of the downstream device. Also, the higher the swing, the less headroom there is for the pre-emphasis magnitude and width. For maximum output pre-emphasis settings, it is recommended that the device VCCO_0 and VCCO_1 supply pins be connected to a 2.5V supply.

Table 4-6 and Table 4-7 lists the required V_{cco} (Driver Supply voltage) and DS (Driver Swing) required to achieve three common nominal V_{DDOppd} (peak-to-peak differential output voltages) and their associated nominal V_{cmout} (output common mode voltage).

In the DC-coupled case, where V_{cco} is connected to the same supply as the input buffer supply voltage of the downstream device, V_{cmount} in Table 4-6 is the common mode voltage at the output of the GS12141 driver. For short low loss transmission lines, this will also be the common mode voltage created at the input termination of the downstream input buffer. However, for long and lossy transmission lines, the amplitude will be attenuated at the downstream receiver and therefore the common mode voltage created at the input termination will be higher and must be measured or simulated for accuracy. For proper link operation, the common mode voltage created at the input termination of the downstream input buffer must be within the V_{cmin} range specified by that device.

In the AC-coupled case, V_{cmout} is the common mode voltage at the driver side of the AC-coupling capacitor placed near the driver. In the AC-coupled case, Vcmout does not need to be within the V_{cmin} range specified by the downstream device. However, the capacitor should have a voltage rating that exceeds $|V_{cmout}-V_{cmin}|$. In addition to the voltage rating, the recommended value of the AC-coupling capacitor should be at least 4.7µF to meet the low cut-off frequency requirement of low transition density signals such as the check-field pattern defined in SMPTE RP-198. The capacitor should have a temperature rating that maintains the capacitance over the required operating range.

Table 4-6: ΔV_{DDO} (mV_{ppd}) and V_{CMOUT}(V) vs. DS Setting and V_{CCO}

	ΔV_{DDO} (mV_{ppd}) vs. DS Setting			DC-Coupled V_{CMOUT} (V) vs. DS Setting			AC-Coupled V_{CMOUT} (V) vs. DS Setting		
V_{cco} (V)	3	8	19	3	8	19	3	8	19
1.2	200	400	—	1.15	1.1	—	1.1	1	—
1.8	200	400	800	1.75	1.7	1.6	1.7	1.6	1.4
2.5	200	400	800	2.45	2.4	2.3	2.4	2.3	2.1

The PPA (pre-emphasis pulse amplitude) also has 55 steps, while the PPW (pre-emphasis pulse width) has 15 steps. Together, the PPA and PPW can be configured to provide optimum loss compensation, therefore minimizing ISI jitter at the downstream receiver.

It is well understood that for high-speed differential link where both trace equalization at the receiver and pre-emphasis at the transmitter are both available, it is preferred to maximize trace equalization before maximizing pre-emphasis. The exercise to do so is beyond the scope of this data sheet. The following section will provide a procedure of optimizing pre-emphasis setting on the GS12141 in the absence of any equalization at the receiver.

4.3.3.1 Pre-emphasis Optimization

The goal of pre-emphasis is to open the eye at the downstream receiver as much as possible. This means minimizing ISI jitter, while meeting sufficient inner eye amplitude to meet a receiver's input sensitivity.

The GS12141 has a HIGH level of precision for pre-emphasis control, which allows for fine optimization of any loss channel. Pre-emphasis compensation of the GS12141 output channel is a two step process. The first step is coarse optimization, while the second step is fine optimization. However the first step alone may meet the designers targets.

Coarse Optimization Procedure:

Given a differential trace length tl, where tl has a 5.94GHz loss profile of 0.7dB/Inch ±2%, the following equations provide a starting point for HD-3G and 6G-12G optimized pre-emphasis settings:

$$\mathbf{PPA_{HD}} = \mathbf{int}\left(\frac{\mathbf{tl}}{2}\right), \mathbf{tl} \leq 40$$

Equation 4-1: HD and 3G Pre-emphasis Amplitude Optimization Setting

$$\mathbf{PPW_{HD}} = \mathbf{int}\left(19 - \frac{100}{\mathbf{tl} + 5.5}\right), \mathbf{tl} \leq 40$$

Equation 4-2: HD and 3G Pre-emphasis Width Optimization Setting

$$\mathbf{PPA_{UHD}} = \mathbf{int}(2 \cdot \mathbf{tl}), \mathbf{tl} \leq 20$$

Equation 4-3: 6G and 12G Pre-emphasis Amplitude Optimization Setting

$$\mathbf{PPW_{UHD}} = \mathbf{int}\left(19 - \frac{100}{\mathbf{tl} + 4.5}\right), \mathbf{tl} \leq 20$$

Equation 4-4: 6G and 12G Pre-emphasis Width Optimization Setting

Note: int(x) is the integer of x

In most cases, where the downstream device has a CDR, these settings may be good enough. However, if the downstream device is a non-re-timed buffer or crosspoint, it may be required to further optimize the settings to minimize the jitter thereby maximizing the system jitter budget.

Fine Optimization Procedure:

The procedure is very straight forward and requires access to the signal at the downstream device input, or non-re-timed device output. If there are multiple stages between the initial downstream device input and final measurement point, it is still possible to perform optimization; however link settings within the other stages must be fairly optimized.

The procedure has two steps.

1. The first step is to set the PPA and PPW to the values obtained by solving the optimization equations, and then measure the downstream jitter. While keeping PPW constant, increment the PPA by 5. If the jitter is lower after the first increment, continue to increment by 5 until the jitter begins increasing or a setting of 55 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Amplitude setting: $PPA_{Optimal}$, and the PPA optimization procedure is complete.

   However, if the jitter increased after the first increment, decrement the setting by 5 below the initial value. If the jitter is lower after the first decrement, continue to decrement by 5 until the jitter begins increasing or a setting of 0 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Amplitude setting: $PPA_{Optimal}$, and the PPA optimization procedure is complete.

   If incrementing the PPA or decrementing the PPA did not result in a setting with lower jitter, then the initial setting derived from the equation is the PPA optimized Pre-emphasis Amplitude setting: $PPA_{Optimal}$.

2. The second step is to set the PPA to the optimized setting $PPA_{Optimal}$ determined in step 1 and PPW to the values obtained by solving the optimization equation, then measure the downstream jitter. While keeping PPA constant, increment the PPW by 1. If the jitter is lower after the first increment, continue to increment by 1 until the jitter begins increasing or a setting of 15 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Width setting: $PPW_{Optimal}$, and the optimization procedure is complete.

However, if the jitter increased after the first increment, decrement the setting by 1 below the initial value. If the jitter is lower after the first decrement, continue to decrement by 1 until the jitter begins increasing or a value of 0 is reached. If there was a setting which resulted in a lower jitter measurement than the initial setting, that is the Optimized Pre-emphasis Width setting: $PPW_{Optimal}$, and the optimization procedure is complete.

If incrementing the PPW or decrementing the PPW did not result in a setting with lower jitter, then the initial setting derived from the equation is the optimized Pre-emphasis Width setting: $PPW_{Optimal}$.

Steps 1 and 2 are illustrated in Figure 4-1: PPA Optimization Flow Chart and Figure 4-2: PPW Optimization Flow Chart below.

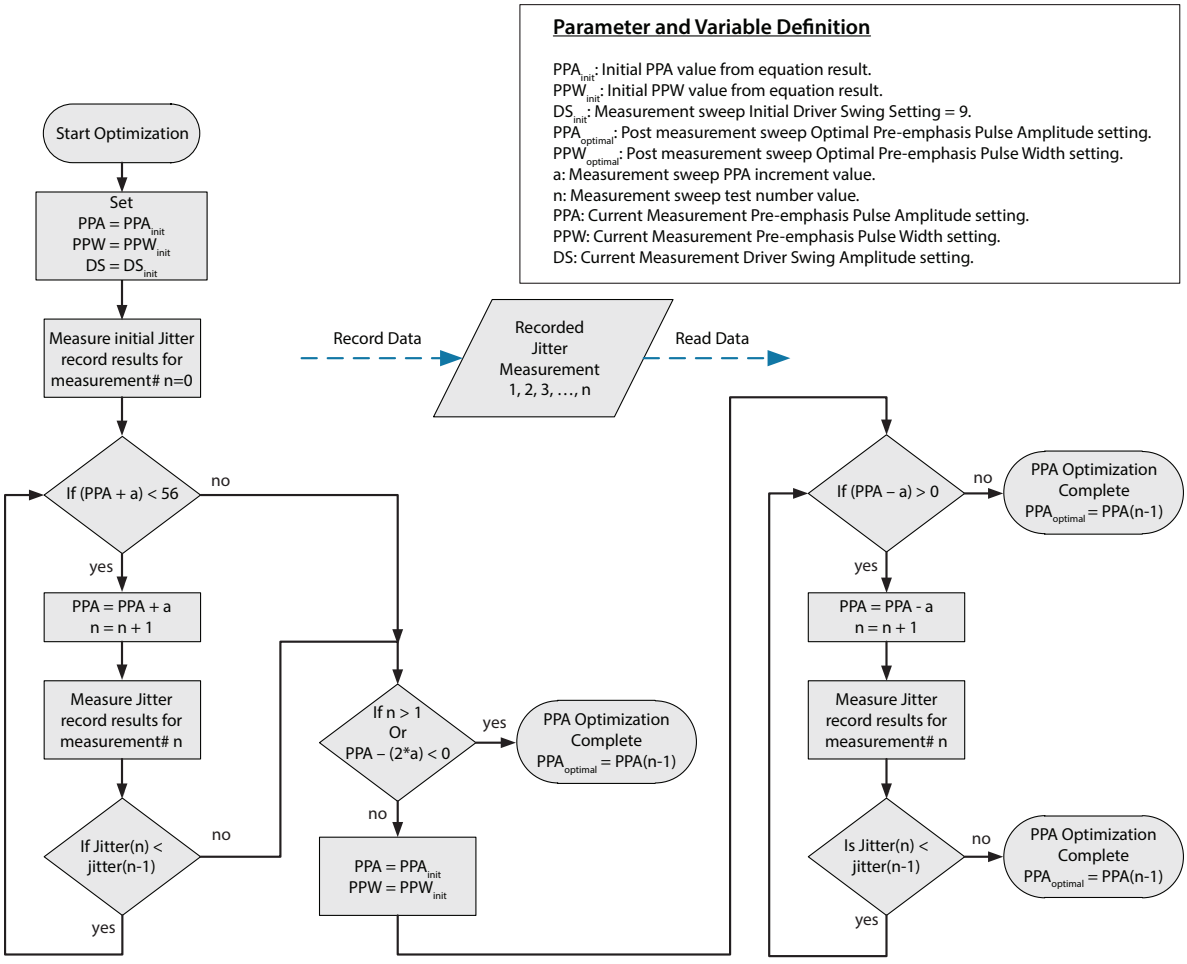


Figure 4-1: PPA Optimization Flow Chart

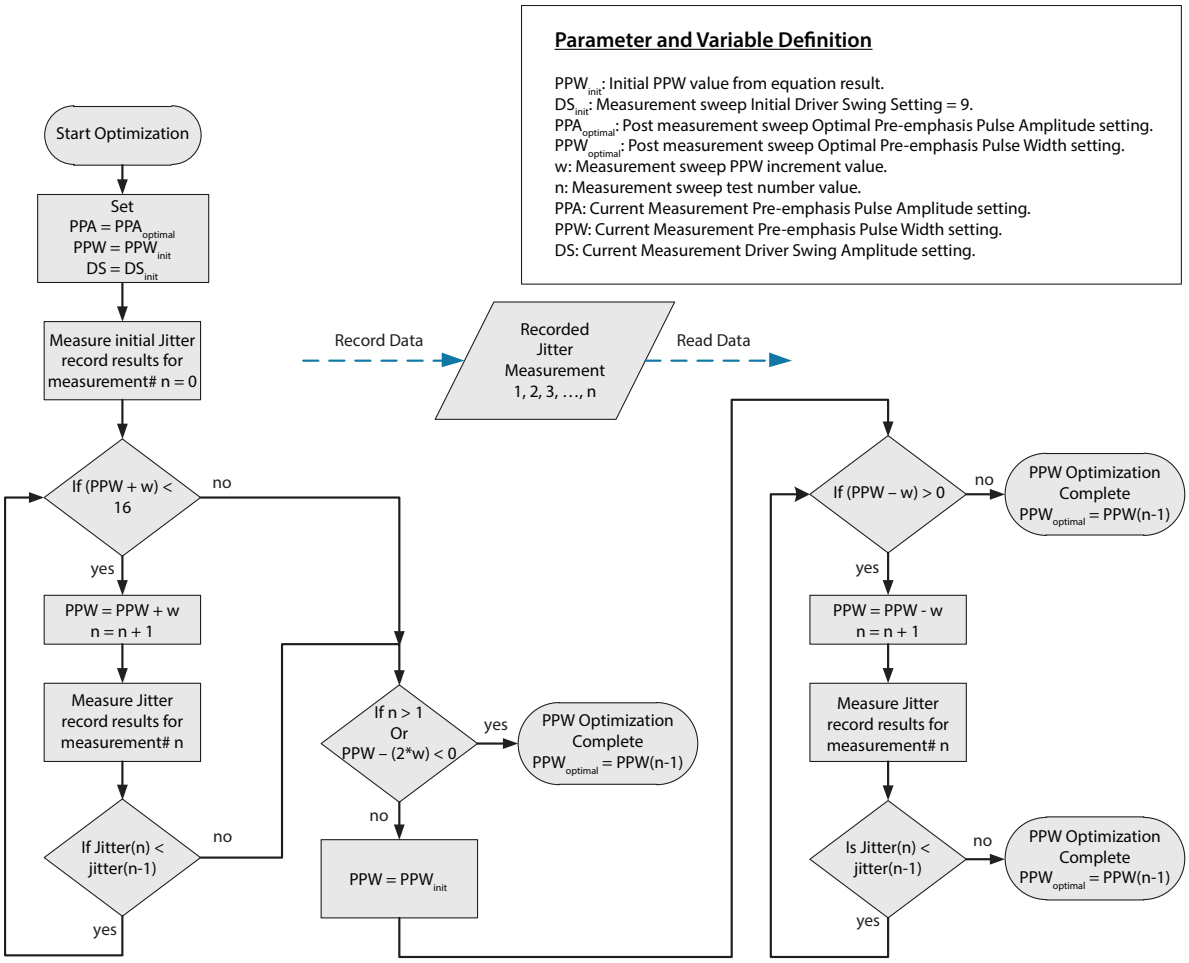


Figure 4-2: PPW Optimization Flow Chart

4.3.4 Output Waveform Specifications

The Duty Cycle Distortion (DCD) of the serial digital differential outputs is less than 12ps. DCD is defined as the difference in the width of an output logic "1" versus that of output logic "0" as measured at the 50% point of the output waveform.

The DCD of the serial digital single ended outputs is less than 30ps.

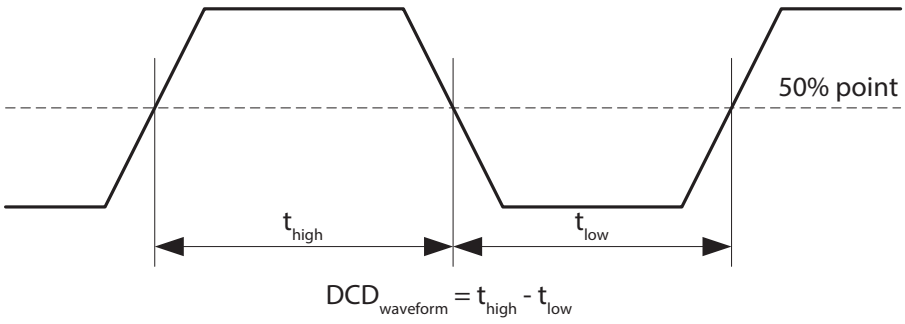


Figure 4-3: Traditional Waveform Definition of DCD

4.3.5 Output State Control Modes

The GS12141 provides several output state control modes to meet specific application requirements. The outputs can be put in low power mode and muted, either manually, or on LOS (Loss of Signal), or on LOS and Loss of Lock. The outputs can also be completely powered down and disabled, either manually, or on LOS. If both mute and disable modes are set, disable will take precedence. Please see Section 4.3.5.1 through Section 4.3.5.3 for more details

4.3.5.1 Output Mute Mode

Each of the outputs on the GS12141 have independent mute controls, which can be configured through the host interface.

The following are the four modes of output mute:

1. Auto Mute on LOS (default)
2. Auto Mute on LOS and during Rate Search
3. Outputs always Operational
4. Outputs always Muted

The default setting on power-up sets the output drivers in the first mode, where the outputs automatically mute on the assertion of LOS. This includes LOS as a result of setting up Squelch Adjust (see Section 4.1.3 for more details). In addition to mute on LOS, with auto mode enabled, setting control parameter **CTRL_OUTPUT<n>_AUTO_MUTE_DURING_RATE_SEARCH** to 1b sets the outputs to mute when the device loses lock and begins to rate search.

The outputs can be set to never mute by setting both the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_MANUAL_MUTE** control parameters in register 0x7349 to 0_b. Alternatively, the outputs can be forced to always be muted by setting the **CTRL_OUTPUT<n>_AUTO_MUTE** and **CTRL_OUTPUT<n>_MANUAL_MUTE** control parameters to 0_b and 1_b respectively.

Note: The <n> in the control parameter names refers to the output number.

4.3.5.2 Output Disable Mode

Each of the outputs on the GS12141 also have independent disable controls, which can be configured through the host interface.

The following are the three modes of output Disable:

1. Outputs defer to Mute settings
2. Auto Disable
3. Outputs always Disabled.

Mode 1 is the default setting on power-up (The **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter in register 0x734A is set to 0_b.), by setting the **CTRL_OUTPUT<n>_AUTO_DISABLE**, the control parameter is set to 1_b and the output will power-down on LOS. This includes LOS as a result of setting up Squelch Adjust (see Section 4.1.2 for more details). This mode takes precedence over any active output mute mode.

By leaving the **CTRL_OUTPUT<n>_AUTO_DISABLE** control parameter set to 0_b and setting the **CTRL_OUTPUT<n>_MANUAL_DISABLE** control parameter also in register 0x734A, to 1_b, it forces the output to be disabled. This mode takes precedence over any active output mute mode. Alternatively, the second output can be powered-down by applying a signal to GPIO3 (SDO1 disable). These are the default function for these GPIO pins at power-up.

Note: The <n> in the control parameter names refers to the output number.

4.3.5.3 Output Control and Status Registers Summary

Table 4-7 and Table 4-8 list the most commonly used control and status parameters of the Output blocks. For a complete list of registers and functions, please see Section 5.

Table 4-7: Re-timer Bypass Control Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x734C	3:3	CTRL_OUTPUT1_RETIMER_MANUAL_BYPASS	Enables manual CDR bypass signal when CTRL_OUTPUT1_RETIMER_AUTO_BYPASS is 0_b.
	2:2	CTRL_OUTPUT1_RETIMER_AUTO_BYPASS	Sets or disables the automatic CDR bypass signal mode.
	1:1	CTRL_OUTPUT0_RETIMER_AUTO_BYPASS	Enables manual CDR bypass signal when CTRL_OUTPUT0_RETIMER_AUTO_BYPASS is 0_b.
	0:0	CTRL_OUTPUT0_RETIMER_MANUAL_BYPASS	Sets or disables the automatic CDR bypass signal mode.
0x7348	0:0	CTRL_OUTPUT1_SIGNAL_SEL	Sets the Clock/Date mode of SDO1. 0_b = Data, 1_b = Clock

Table 4-8: Output Swing and Pre-emphasis Control Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x7328	12:8	CFG_OUTPUT1_CD_SD_TD_PREEMPH_WIDTH	Output 1 pre-emphasis pulse width configuration parameter for all rates.
	6:6	CFG_OUTPUT1_CD_SD_TD_PREEMPH _PWRDWN	SDO1 pre-emphasis power down parameter for all rates.
	5:0	CFG_OUTPUT1_CD_SD_TD_PREEMPH_AMPL	Output 1 pre-emphasis pulse amplitude configuration parameter for all rates.
0x7329	13:8	CFG_OUTPUT1_CD_SD_TD_DRIVER_SWING	Output 1 main output driver amplitude control for all rates.

Table 4-8: Output Swing and Pre-emphasis Control Parameters (Continued)

Address$_h$	Bit Slice	Parameter Name	Description
0x732A	12:8	CFG_OUTPUT0_CD_SD_TD_PREEMPH_WIDTH	Output 0 pre-emphasis pulse width configuration parameter for all rates.
	6:6	CFG_OUTPUT1_CD_SD_TD_PREEMPH _PWRDWN	SDO1 pre-emphasis power down parameter for all rates.
	5:0	CFG_OUTPUT0_CD_SD_TD_PREEMPH_AMPL	Output 0 pre-emphasis pulse amplitude configuration parameter for all rates.
0x732B	13:8	CFG_OUTPUT0_CD_SD_TD_DRIVER_SWING	Output 0 main output driver amplitude control for all rates.

Table 4-9: Mute and Disable Control Parameters

Parameter Name (<n>: Output Number)	GS12141 Output Modes						
	Output Disabled on LOS	Output Disabled on LOS and Muted during Rate Search	Output is always disabled	Output is Muted on LOS, including LOS from Squelch Adjust	Output is Muted on rate Search and on LOS, including LOS from Squelch Adjust	Output is Always On	Output is Always Muted
	Parameter Value						
CTRL_OUTPUT<n>_AUTO_DISABLE	1	1	0	0	0	0	0
CTRL_OUTPUT<n>_MANUAL_DISABLE	X	X	1	0	0	0	0
CTRL_OUTPUT<n>_AUTO_MUTE	X	1	X	1	1	0	0
CTRL_OUTPUT<n>_AUTO_MUTE_DURING_RATE_SEARCH	0	1	X	0	1	X	X
CTRL_OUTPUT<n>_MANUAL_MUTE	X	X	X	X	X	0	1

Table 4-10: Output Status Parameters

Address$_h$	Bit Slice	Parameter Name	Description
0x7386	7:4	STAT_OUTPUT<n>_MODE	Provides the status of the output driver.
0x7387	15:15	STAT_OUTPUT<n>_DISABLE	Indicates if disable mode is enabled for the output in the control priority hierarchy.
	13:13	STAT_OUTPUT<n>_MUTE	Indicates if mute mode is enabled for the output in the control priority hierarchy.
	11:11	STAT_OUTPUT<n>_RETIMER_BYPASS	Indicates the re-timed status of signal available at the output.

As can be seen in Table 4-9, there is a hierarchy in the control modes. If disable and mute are selected, disable takes priority over mute. The **STAT_OUTPUT<n>_MODE** parameter indicates the active mode of each output driver, whereas the **STAT_OUTPUT<n>_DISABLE** and **STAT_OUTPUT<n>_DISABLE** parameters indicate potential active modes if that particular mode is the highest enabled on the list.

Note: The <n> in the control parameter names refers to the output number.

4.4 GPIO Controls

There are four configurable GPIO pins which can independently be configured as inputs or outputs. Each GPIO has a default function which can be re-configured through the host interface.

If there is a conflict between the internal register configuration of a given device function and the logic-level applied to a GPIO pin that is configured to control that same device function, the GPIO logic-level takes precedence over the internal register configuration. The logic HIGH and LOW levels of the GPIO[3:0] pin to which LOS is connected are specified by the EIA/JESD8-5A standard for 1.8V operation.

For a list of available functions and configuration details of GPIO[3:0], please refer to the GPIO Configuration registers in Section 5.

4.5 GSPI Host Interface

The GS12141 is configured via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (SDIN pin), serial data output signal (SDOUT pin), an active-LOW chip select ($\overline{CS}$ pin) and a burst clock (SCLK pin).

The GS12141 is a slave device, so the SCLK, SDIN and $\overline{CS}$ signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

4.5.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-LOW signal provided by the host processor to the GS12141.

The HIGH-to-LOW transition of this pin marks the start of serial communication to the GS12141.

The LOW-to-HIGH transition of this pin marks the end of serial communication to the GS12141.

Each device may use its own separate Chip Select signal from the host processor or up to 32 devices may be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the UNIT ADDRESS in GSPI Command Word 1 will respond to communication from the host processor (unless the B'CAST ALL bit in GSPI Command Word 1 is set to 1).

4.5.2 SDIN Pin

The SDIN pin is the GSPI serial data input pin of the GS12141.

The 32-bit Command and 16-bit Data Words from the host processor or from the SDOUT pin of other devices are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is LOW.

4.5.3 SDOUT Pin

The SDOUT pin is the GSPI serial data output of the GS12141.

All data transfers out of the GS12141 to the host processor or to the SDIN pin of other connected devices occur from this pin.

By default at power up or after system reset, the SDOUT pin provides a non-clocked path directly from the SDIN pin, regardless of the $\overline{CS}$ pin state, except during the GSPI Data Word portion for read operations from the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the SDOUT pin is used to output data read from an internal Configuration and Status Register (CSR) when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK, so that it can be read by the host processor or other downstream connected device on the subsequent SCLK rising edge.

4.5.3.1 GSPI Link Disable Operation

It is possible to disable the direct SDIN to SDOUT (Loop-Through) connection by writing a value of 1 to the GSPI_LINK_DISABLE bit in HOST_CONFIG. When disabled, any data appearing at the SDIN pin will not appear at the SDOUT pin and the SDOUT pin is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter $t_{cmd\_GSPI\_config}$ (4 SCLK cycles).

Table 4-11: GSPI_LINK_DISABLE Bit Operation

Bit State	Description
0	SDIN pin is looped through to the SDOUT pin
1	Data appearing at SDIN does not appear at SDOUT, and SDOUT pin is HIGH.

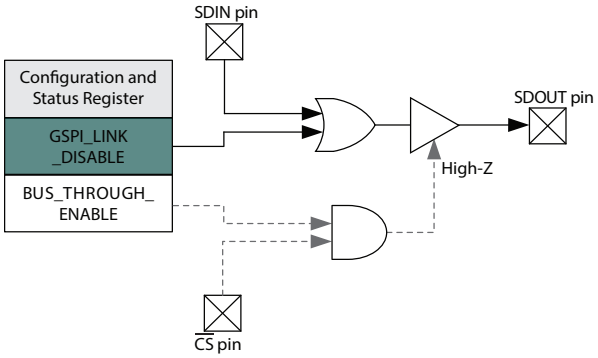


Figure 4-4: GSPI_LINK_DISABLE Operation

4.5.3.2 GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS12141 can share a common PCB trace with other GSPI devices for SDOUT output.

When configured for Bus-Through operation, by setting GSPI_BUS_THROUGH_ENABLE bit to 1, the SDOUT pin will be high-impedance when the $\overline{CS}$ pin is HIGH.

When the $\overline{CS}$ pin is LOW, the SDOUT pin will be driven and will follow regular read and write operation as described in Section 4.5.3.

Multiple chains of GS12141 devices can share a single SDOUT bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select ($\overline{CS}$).

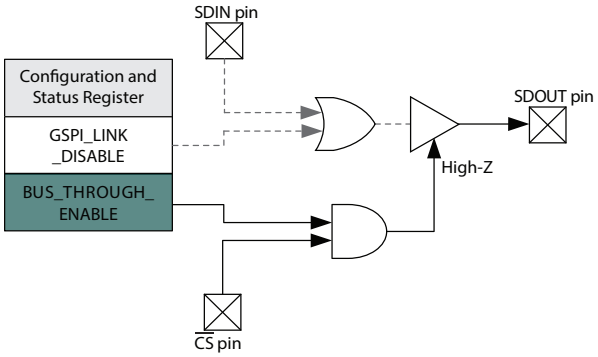


Figure 4-5: GSPI_BUS_THROUGH_ENABLE Operation

4.5.4 SCLK Pin

The SCLK pin is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS12141 SDIN pin on the rising edge of SCLK. Serial data is clocked out of the device from the SDOUT pin on the falling edge of SCLK (read operation). SCLK is ignored when $\overline{CS}$ is HIGH.

The maximum interface clock rate is 27MHz.

4.5.5 Command Word 1 Description

All GSPI accesses are a minimum of 48 bits in length (two 16-bit Command Words followed by a 16-bit Data Word) and the start of each access is indicated by the HIGH-to-LOW transition of the chip select ($\overline{CS}$) pin of the GS12141.

The format of the Command Words and Data Word are shown in Figure 4-6.

Data received immediately following this HIGH-to-LOW transition will be interpreted as a new Command Word.

4.5.5.1 R/$\overline{W}$ bit—B15 Command Word 1

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

4.5.5.2 B'CAST ALL—B14 Command Word 1

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When B'CAST ALL is set to 1, the following Data Word (AUTOINC = 0) or Data Words (AUTOINC = 1) are written to the register specified by the ADDRESS field of the Command Words (and subsequent addresses when AUTOINC = 1), regardless of the setting of the UNIT ADDRESS(es).

When B'CAST ALL is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of Command Word 1 write the Data Word to the register specified by the ADDRESS field of the Command Words.

4.5.5.3 EMEM—B13 Command Word 1

The EMEM bit must be set to 1 in Command Word 1. When EMEM is set to 1, a 23-bit address split between Command Word 1 and Command Word 2 is used to access the registers in this device.

4.5.5.4 AUTOINC—B12 Command Word 1

When AUTOINC is set to 1, Auto-Increment read or write access is enabled.

In Auto-Increment Mode, the device automatically increments the register address for each contiguous read or write access, starting from the address defined in the ADDRESS field of the Command Word.

The internal address is incremented for each 16-bit read or write access until a LOW-to-HIGH transition on the $\overline{CS}$ pin is detected.

When AUTOINC is set to 0, single read or write access is required.

Auto-Increment write must not be used to update values in HOST_CONFIG.

4.5.5.5 UNIT ADDRESS—B11:B7 Command Word 1

The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed DEVICE_UNIT_ADDRESS in HOST_CONFIG.

By default at power-up or after a device reset, the DEVICE_UNIT_ADDRESS is set to 00_h.

4.5.5.6 ADDRESS—B6:B0 Command Word 1 and B15:B0 Command Word 2

The Command and Data Word formats are shown in Figure 4-6 and Figure 4-7 below.

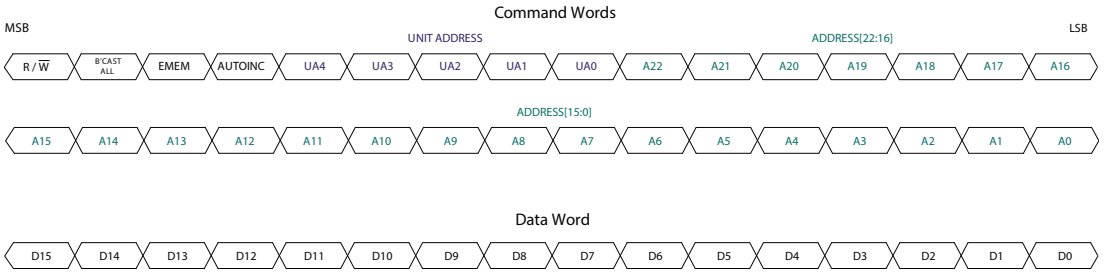


Figure 4-6: Command and Data Word Format

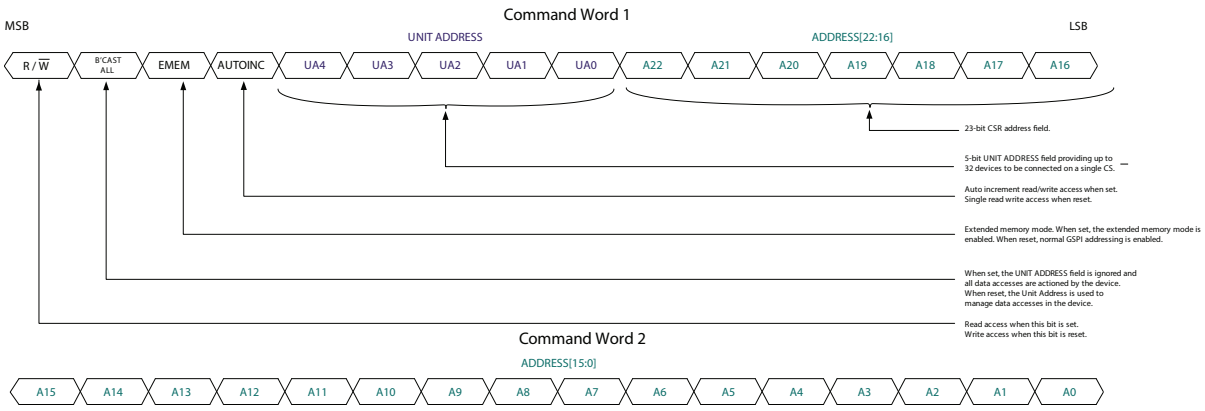


Figure 4-7: Command Word 1 and Command Word 2 Details

4.5.6 GSPI Transaction Timing

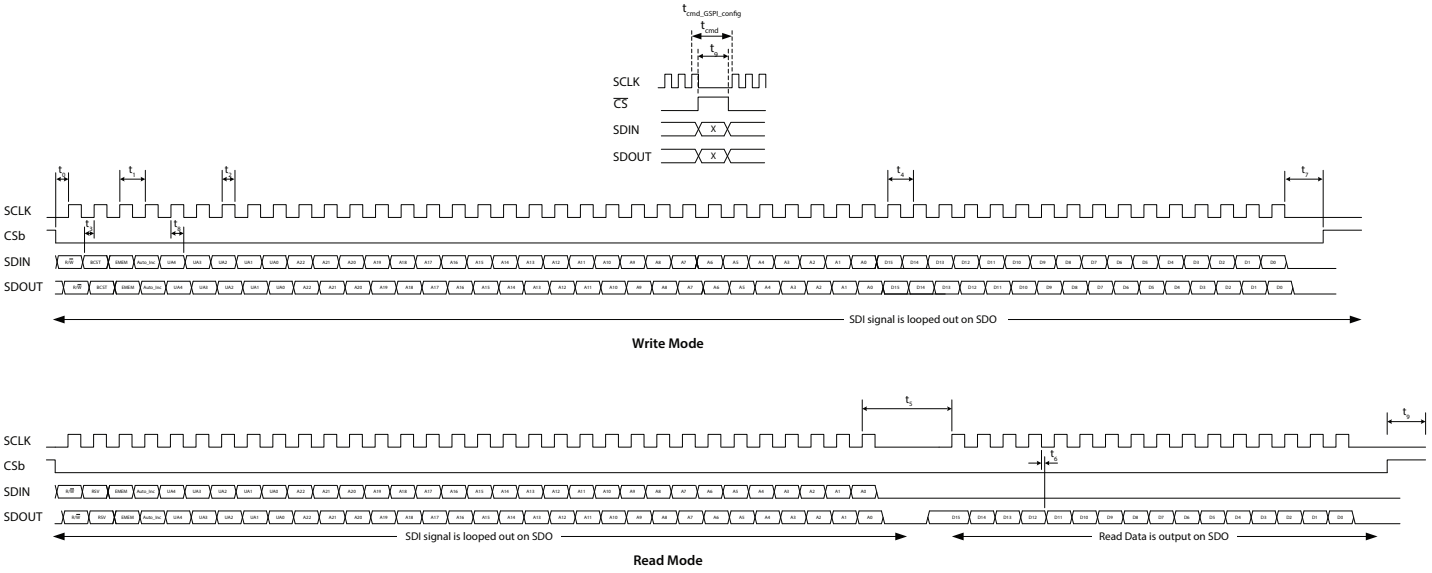


Figure 4-8: GSPI External Interface Timing

Table 4-12: GSPI Timing Parameters

Parameter	Symbol	Equivalent SCLK Cycles	Min	Typ	Max	Units
SCLK Frequency	—	—	—	—	27	MHz
$\overline{CS}$ LOW Before SCLK Rising Edge	t_0	—	1.7	—	—	ns
SCLK Period	t_1	—	37	—	—	ns
SCLK Duty Cycle	t_2	—	40	50	60	%
Input Data Setup Time	t_3	—	2.3	—	—	ns
SCLK Idle Time – Write	t_4	1	38.5[1]	—	—	ns
SCLK Idle Time – Read	t_5	—	138	—	—	ns
Inter–Command Delay Time	t_{cmd}	3	115	—	—	ns
Inter–Command Delay Time (after GSPI configuration write)	$t_{cmd\_GSPI\_conf}$[2]	4	139	—	—	ns
SDOUT After SCLK Falling Edge	t_6	—	1.3	—	6.4	ns
CS HIGH After Final SCLK Falling Edge	t_7	—	0	—	—	ns
Input Data Hold Time	t_8	—	1.2	—	—	ns
$\overline{CS}$ HIGH Time	t_9	—	58	—	—	ns
SDIN to SDOUT Combinatorial Delay	—	—	—	—	3.4	ns
Max chips daisy-chained at max SCLK frequency (26 MHz)	When host clocks in SDOUT data on falling edge of SCLK		—	—	8	# of compatible Semtech devices
Max frequency for 32 daisy-chained devices			—	—	7.5	MHz

Note:

1. Parameter is exactly multiple of SCLK periods and scales proportionally.
2. $t_{cmd\_GSPI\_conf}$ inter-command delay must be used whenever modifying HOST_CONFIG register at address 0x00.

4.5.7 Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-9 to Figure 4-13.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 48-bits long, consisting of two Command Words and a single Data Word. The read or write cycle begins with a HIGH-to-LOW transition of the $\overline{CS}$ pin. The read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 3 SCLK clock cycles. After modifying values in HOST_CONFIG, the inter-command delay time, $t_{cmd\_GSPI\_config}$, is a minimum of 4 SCLK clock cycles.

For read access, the time from the last bit of Command Word 2 to the start of the data output, as defined by t_5, corresponds to no less than 4 SCLK clock cycles at 27MHz.

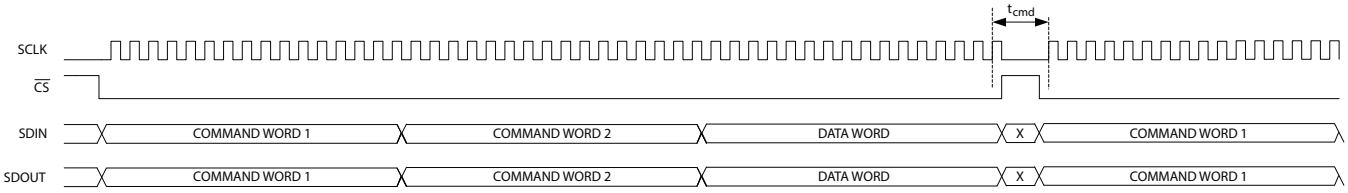


Figure 4-9: GSPI Write Timing—Single Write Access with Loop-Through Operation (default)

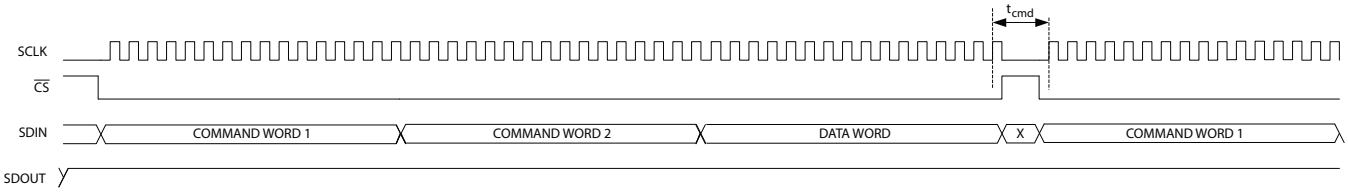


Figure 4-10: GSPI Write Timing—Single Write Access with GSPI Link-Disable Operation

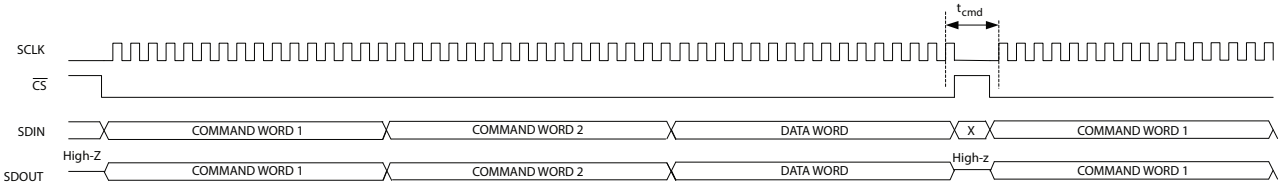


Figure 4-11: GSPI Write Timing—Single Write Access with Bus-Through Operation

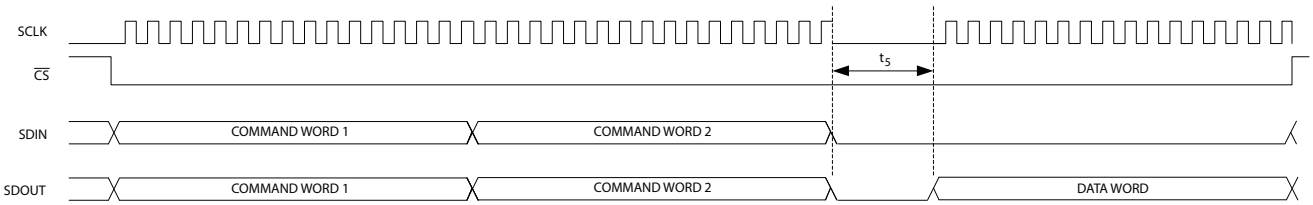


Figure 4-12: GSPI Read Timing—Single Read Access with Loop-Through Operation (default)

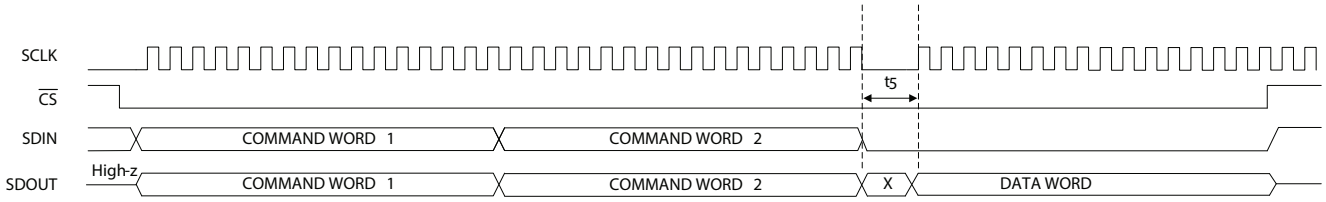


Figure 4-13: GSPI Read Timing—Single Read Access with Bus-Through Operation

4.5.8 Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-14 to Figure 4-18.

Auto-increment mode is enabled by the setting of the AUTOINC bit of Command Word 1.

In this mode, multiple Data Words can be read from/written to the device using only one starting address. Each access is initiated by a HIGH-to-LOW transition of the $\overline{CS}$ pin, and consists of two Command Words and one or more Data Words. The internal address is automatically incremented after the first read or write Data Word, and continues to increment until the read or write access is terminated by a LOW-to-HIGH transition of the $\overline{CS}$ pin.

Note: Writing to HOST_CONFIG using Auto-increment access is not allowed.

The maximum interface clock rate is 27MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of 3 SCLK clock cycles.

For read access, the time from the last bit of the second Command Word to the start of the data output of the first Data Word as defined by t_5 will be no less than 4 SCLK cycles at 27MHz. All subsequent read data accesses will not be subject to this delay during an Auto-Increment read.

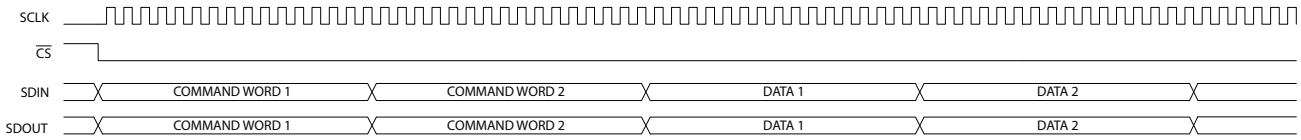


Figure 4-14: GSPI Write Timing—Auto-Increment with Loop-Through Operation (default)

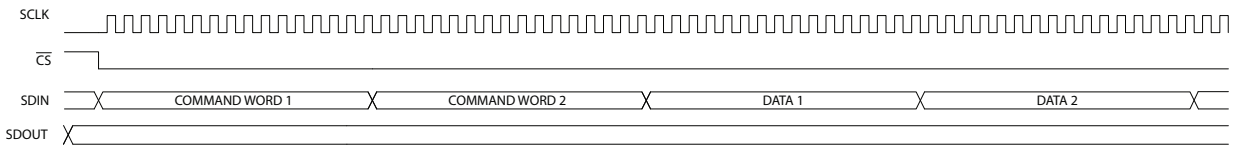


Figure 4-15: GSPI Write Timing—Auto-Increment with GSPI Link Disable Operation

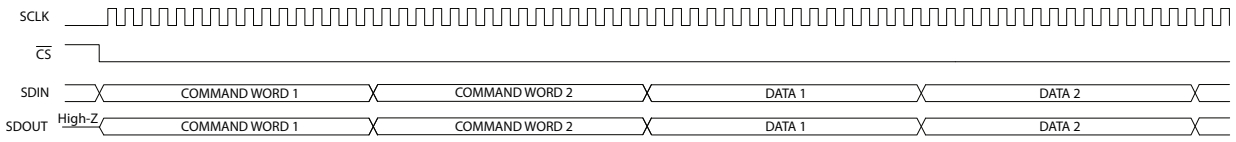


Figure 4-16: GSPI Write Timing—Auto-Increment with Bus-Through Operation

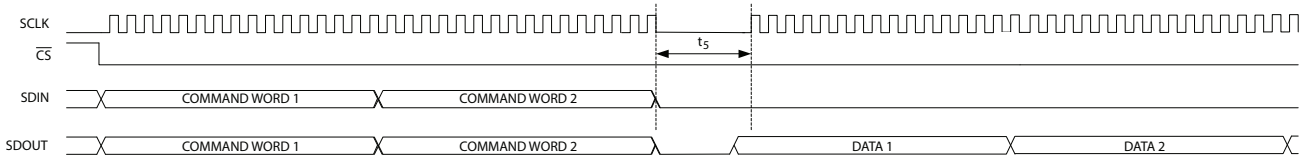


Figure 4-17: GSPI Read Timing—Auto-Increment Read with Loop-Through Operation (default)

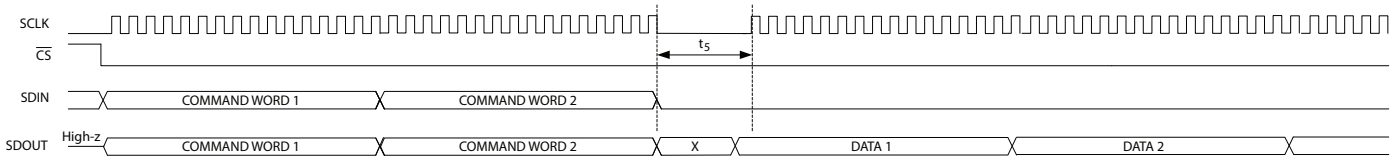


Figure 4-18: GSPI Read Timing—Auto-Increment Read with Bus-through Operation

4.5.9 Setting a Device Unit Address

Multiple (up to 32) GS12141 devices can be connected to a common Chip Select ($\overline{CS}$) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common $\overline{CS}$ can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

Note: By default at power up or after a device reset, the **DEVICE_UNIT_ADDRESS** of each device is set to 0_h and the SDIN→SDOUT non-clocked loop-through for each device is enabled.

These are the steps required to set the **DEVICE_UNIT_ADDRESS** of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting **HOST_CONFIG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 1 and the **DEVICE_UNIT_ADDRESS** field set to 0. This disables the direct SDIN→SDOUT non-clocked path for all devices on chip select.
2. Write to Unit Address 0 selecting **HOST_CONFIG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 0 and the **DEVICE_UNIT_ADDRESS** field set to a unique Unit Address. This configures **DEVICE_UNIT_ADDRESS** for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use **DEVICE_UNIT_ADDRESS** value 0.

3. Repeat step 2 using new, unique values for the **DEVICE_UNIT_ADDRESS** field in **HOST_CONFIG** until all devices in the chain have been configured with their own unique Unit Address value.

Note: $t_{cmd\_GSPI\_conf}$ delay must be observed after every write that modifies **HOST_CONFIG**.

All connected devices receive this command (by default the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the **DEVICE_UNIT_ADDRESS** in **HOST_CONFIG**.

Note: Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's SDOUT connected to the application host processor. Multiple chains configured in Bus-Through mode can have their final SDOUT outputs connected to a single application host processor input.

4.5.10 Default GSPI Operation

By default at power up or after a device reset, the GS12141 is set for Loop-Through Operation and the internal **DEVICE_UNIT_ADDRESS** field of the device is set to 0.

Figure 4-19 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS12141.

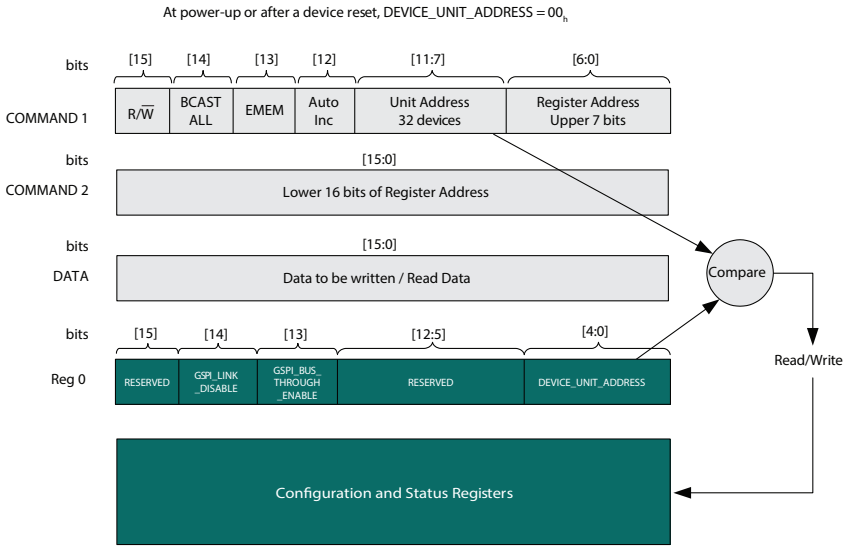


Figure 4-19: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word 1 for write access (R/$\overline{W}$ = 0); set Auto Increment; set the Unit Address field in the Command Word 1 to match the configured **DEVICE_UNIT_ADDRESS** which will be zero after power-up. Set the Register Address bits in Command Word 1 to match the upper 7 bits of the register address to be accessed. Set the bits in Command Word 2 to match the lower 16 bits of the register address to be accessed. Write Command Word 1 and Command Word 2.
2. Write the Data Word to be written to the first register.
3. Write the Data Word to be written to the next register in Auto Increment mode, etc.

Read access is the same as the above with the exception of step 1, where the Command Word 1 is set for read access (R/$\overline{W}$ = 1).

Note: The UNIT ADDRESS field of Command Word 1 must always match **DEVICE_UNIT_ADDRESS** for an access to be accepted by the device. Changing **DEVICE_UNIT_ADDRESS** to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration).

5. Register Map

The host interface on the GS12141 provides users complete control of key features such as GPIO configuration, PLL loop bandwidth settings, re-time parameters, carrier detection, cable equalization, bypass modes, output swing controls, mute functions, pre-emphasis control and many others.

5.1 Control Registers

Table 5-1: Control Registers

GSPI Address$_h$	Register Name	R/W
00	CONTROL_ REG	RW
01 to 7E	RSVD	RW
7F	RESET_REG_0	RW
Device Configuration		
7304	MISC_CTRL	RW
7305	RSVD	RW
7306	RATE_ DETECT_ MODE	RW
7307	RSVD	RW
CDR Configuration		
7308	RSVD	RW
7309	CFG_PLL	RW
730A	PLL_LOOP_ BANDWIDTH_ UHD	RW
730B	PLL_LOOP_ BANDWIDTH_ HD	RW
730C	PLL_LOOP_ BANDWIDTH_ SD_MADI	RW
730D to 730F	RSVD	RW
GPIO Configuration		
7310	GPIO0_CFG	RW
7311	GPIO1_CFG	RW
7312	GPIO2_CFG	RW
7313	GPIO3_CFG	RW
Equalizer Configuration		
7314	RSVD	RW

Table 5-1: Control Registers (Continued)

GSPI Address$_h$	Register Name	R/W
7315	CARR_ DET_CFG	RW
7316	SQUELCH_ PARAMETERS	RW
7317	CABLE_EQ_ BYPASS_ MODE	RW
7318	INPUT_ LAUNCH_ SWING_CFG	RW
7319 to 731F	RSVD	RW
7320	CD_FILTER_ DELAYS_0	RW
7321	CD_FILTER_ DELAYS_1	RW
7322	CD_FILTER_ DELAYS_2	RW
7323 to 7325	RSVD	RW
Output Configuration		
7326	OUTPUT_CFG	RW
7327	RSVD	RW
7328	OUTPUT_ PARAM_CD_ SD_TD_0	RW
7329	OUTPUT_ PARAM_CD_ SD_TD_1	RW
732A	OUTPUT_ PARAM_CD_ SD_TD_2	RW
732B	OUTPUT_ PARAM_CD_ SD_TD_3	RW
732C to 7347	RSVD	RW
7348	OUTPUT_SIG_ SELECT	RW
7349	CONTROL_ OUTPUT_ MUTE	RW
734A	CONTROL_ OUTPUT_ DISABLE	RW
734B	RSVD	RW
734C	CONTROL_ RETIMER_ BYPASS	RW
734D to 737F	RSVD	RW

5.2 Status Registers

Table 5-2: Status Registers

GSPI Address$_h$	Register Name	R/W
7380 to 7382	RSVD	RW
7383	DEVICE_ID	RW
7384	STICKY_ COUNTS_0	RW
7385	STICKY_ COUNTS_1	RW
7386	CURRENT_ STATUS_0	RW
7387	CURRENT_ STATUS_1	RW
7388	EQ_GAIN_IND	RW
7389 to 7390	RSVD	RW

5.3 Register Descriptions

Table 5-3: Register Descriptions

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
00	CONTROL_ REG	RSVD	15:15	RW	0	Reserved — do not modify.
		GSPI_LINK_DISABLE	14:14	RW	0	GSPI loop-through disable.
		GSPI_BUS_THROUGH_ ENABLE	13:13	RW	0	GSPI bus-through enable.
		DEV_UNIT_ADDRESS	4:0	RW	0	Device address programmed by application.
01 to 7E	RSVD	RSVD	15:0	RW	—	Do not access these registers. It is not permitted to perform a read/write function on these registers. If data is written, any of the registers device performance is not guaranteed, and a device Reset must be applied.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7F	RESET_REG_0	RESET_CONTROL	15:0	RW	DD00	Device Reset, Reverts all internal logic and register values to defaults. Write Values: AA00 = Asserts device reset DD00 = De-assert device reset AD00 = Assert/de-assert device reset in a single write Read Values: $AA00_h$ = User-initiated reset is asserted $DD00_h$ = User-initiated reset is de-asserted
7304	MISC_CTRL	RSVD	15:1	RW	0	Reserved — do not modify.
		CTRL_CLEAR_COUNTS	0:0	RW	0	0 = No action 1 = Clear sticky counts Part of a four way handshake with STAT_CLEAR_COUNTS_STATUS (register 0x7386). Ensure STAT_CLEAR_COUNTS _STATUS = 0 (idle), before setting CTRL_CLEAR_COUNTS = 1 (clear sticky counts). Once the device reports STAT_CLEAR_COUNTS _STATUS = 2 (cleared), reset CTRL_CLEAR_COUNTS to 0. The device will now reset STAT_CLEAR_COUNTS_STATUS to 0 (idle) and the clearing process can be repeated at any time.
7305	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7306	RATE_ DETECT_ MODE	RSVD	15:14	RW	0	Reserved — do not modify.
		RSVD	13:9	RW	1	Reserved — do not modify.
		RSVD	8:5	RW	0	Reserved — do not modify.
		CFG_MANUAL_RATE	4:1	RW	0	0 = < MADI (bypass for LOW data rates, also drives the EQ bypass selection in GS12141) 1 = MADI 2 = SD 3 = HD 4 = 3G 5 = 6G 6 = 12G 7 = Reserved Manual rate selection. The CDR will only lock to the selected rate.
		CFG_AUTO_RATE_ DETECT_ENA	0:0	RW	1	0 = Disable auto rate detection 1 = Enable auto rate detection When automatic rate detection is disabled, the rate is set by CFG_MANUAL_RATE.
7307	RSVD	RSVD	15:0	RW	0	Do not modify these registers.
CDR Configuration						
7308	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7309	CFG_PLL	RSVD	15:2	RW	28	Reserved — do not modify.
		CFG_MAX_LBW	1:1	RW	1	To maximize LBW of PLL, set this parameter to 0.
		RSVD	1:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
730A	PLL_LOOP_BANDWIDTH_UHD	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_12G	12:8	RW	8	11.88Gb/s (12G) loop bandwidth setting: 00 = Reserved 01 = 0.0625x 02 = 0.125x 03 = Reserved 04 = 0.25x 05 to 07 = Reserved 08 = 0.5x 09 to 1B = Reserved 1C = 1.0x 1D to 1F = Reserved
		RSVD	7:5	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_6G	4:0	RW	8	5.94Gb/s (6G) loop bandwidth setting. See CFG_PLL_LBW_12G.
730B	PLL_LOOP_BANDWIDTH_HD	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_3G	12:8	RW	8	2.97Gb/s (3G) loop bandwidth setting. See CFG_PLL_LBW_12G.
		RSVD	7:5	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_HD	4:0	RW	8	1.485Gb/s (HD) loop bandwidth setting. See CFG_PLL_LBW_12G.
730C	PLL_LOOP_BANDWIDTH_SD_MADI	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_SD	12:8	RW	1C	270Mb/s (SD) loop bandwidth setting. See CFG_PLL_LBW_12G.
		RSVD	7:5	RW	0	Reserved — do not modify.
		CFG_PLL_LBW_MADI	4:0	RW	8	125Mb/s (MADI) loop bandwidth setting. See CFG_PLL_LBW_12G.
730D to 730F	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
GPIO Configuration						
7310	GPIO0_CFG	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_GPIO0_OUTPUT_ENA	8:8	RW	1	0 = Output disabled (tri-stated/ high impedance); GPIO pin is configured as an input. 1 = Output enabled.
		CFG_GPIO0_FUNCTION	7:0	RW	80	Function select for GPIO 0 pin. GPIO0 Output Functions: 00 = Output driven LOW 01 = Output driven HIGH 02 = PLL lock status 03 to 7F = Reserved 80 = LOS (Loss of Signal, inverse of Carrier Detect) 81 = CD (Carrier Detect) 82 = Reserved 83 = SD/$\overline{HD}$ status 84 = Rate detected [0] 85 = Rate detected [1] 86 = Rate detected [2] 87 to FF = Reserved GPIO0 Input Functions: 00 to 81 = Reserved 82 = Output 1 disable control 83 to FF = Reserved
7311	GPIO1_CFG	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_GPIO1_OUTPUT_ENA	8:8	RW	1	See GPIO0_CFG.
		CFG_GPIO1_FUNCTION	7:0	RW	2	
7312	GPIO2_CFG	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_GPIO2_OUTPUT_ENA	8:8	RW	0	See GPIO0_CFG.
		CFG_GPIO2_FUNCTION	7:0	RW	86	
7313	GPIO3_CFG	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_GPIO3_OUTPUT_ENA	8:8	RW	0	See GPIO0_CFG.
		CFG_GPIO3_FUNCTION	7:0	RW	82	

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Equalizer Configuration						
7314	RSVD	RSVD	15:0	RW	102	Reserved — do not modify.
7315	CARR_ DET_CFG	RSVD	15:1	RW	0	Reserved — do not modify.
		CFG_SEC_CD_INCL_ CLI_SQUELCH	0:0	RW	0	Additional conditions for deriving secondary carrier detection status: 0 = Ignore CLI squelch 1 = Take into account CLI squelch
7316	SQUELCH_ PARAMETERS	RSVD	15:15	RW	0	Reserved — do not modify.
		CFG_CLI_SQUELCH_ THRESHOLD	14:8	RW	40	Squelch Threshold.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_CLI_SQUELCH_ HYSTERESIS	6:0	RW	2	Squelch Hysteresis.
7317	CABLE_EQ_ BYPASS_ MODE	RSVD	15:2	RW	0	Reserved — do not modify.
		CTRL_CEQ_MANUAL_ BYPASS	1:1	RW	0	0 = Cable Equalizer not bypassed 1 = Cable Equalizer bypassed Controls EQ bypass when CTRL_CEQ_AUTO_ BYPASS is disabled.
		CTRL_CEQ_AUTO_ BYPASS	0:0	RW	1	Auto mode control: 0 = Disable auto mode 1 = Enable auto mode When CFG_CEQ_AUTO_BYPASS = 0, EQ bypass is controlled by CFG_CEQ_MANUAL_BYPASS.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
		RSVD	15:7	RW	0	Reserved — do not modify.
7318	INPUT_ LAUNCH_ SWING_CFG	CFG_EQ_INPUT_ LAUNCH_SWING_ COMP	6:0	RW	50	Input LSC (Launch Swing Compensation) setting in units of $50mV_{ppd}$ Any setting from 0 to 127 (decimal) can be set. The device will use the closest multiple of 50mV in the range 250mV to 1000mV as follows: 0 to 25 dec = Selects 250mV 25 to 100 dec = Valid range of settings (250mV to 1000mV) closest multiple of 50mV used 100 to 127 dec = Selects 1000mV Default setting of 80_d (50_h) corresponds to 800mV. Register Setting (Decimal) — LSC Voltage 25 — 250mV 30 — 300mV 35 — 350mV ... — ... 100 — 1000mV
7319	RSVD	RSVD	15:0	RW	1	Reserved — do not modify.
731A	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
731B	RSVD	RSVD	15:0	RW	1	Reserved — do not modify.
731C to 731E	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
731F	RSVD	RSVD	15:8	RW	0	Reserved — do not modify.
	RSVD	RSVD	7:4	RW	4	Reserved — do not modify.
	RSVD	RSVD	3:0	RW	3	Reserved — do not modify.
7320	CD_FILTER_ DELAYS_0	RSVD	15:8	RW	0	Reserved — do not modify.
		CFG_CD_FILTER_ SAMPLE_WIN	7:0	RW	3	Carrier detect sample window period in clock cycles. Sample window size is this value plus 1 clock cycle.
7321	CD_FILTER_ DELAYS_1	RSVD	15:10	RW	0	Reserved — do not modify.
		CFG_CD_FILTER_ DEASSERT_CNT	9:0	RW	F	Number of samples for detecting carrier detection de-assertion.
7322	CD_FILTER_ DELAYS_2	RSVD	15:10	RW	0	Reserved — do not modify.
		CFG_CD_FILTER_ ASSERT_CNT	9:0	RW	3FF	Number of samples for detecting carrier detection assertion.
7323 to 7325	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
Output Configuration						
7326	OUTPUT_CFG	RSVD	15:4	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_SUPPLY_VOLTAGE	3:3	RW	0	0 = 1.8V and 2.5V supply 1 = 1.2V supply Host must configure this setting based on the power supply connected to the trace driver for output 1.
		RSVD	2:2	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_SUPPLY_VOLTAGE	1:1	RW	0	0 = 1.8V and 2.5V supply 1 = 1.2V supply Host must configure this setting based on the power supply connected to the trace driver for output 0.
		RSVD	0:0	RW	0	Reserved — do not modify.
7327	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7328	OUTPUT_PARAM_CD_SD_TD_0	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_SD_TD_PREEMPH_WIDTH	12:8	RW	2	Configure pre-emphasis pulse width for all data rates on DDO1. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse width to better match the channel loss response.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_SD_TD_PREEMPH_PWRDWN	6:6	RW	0	Pre-emphasis power-down control for all data rates on DDO1: 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled)
		CFG_OUTPUT1_CD_SD_TD_PREEMPH_AMPL	5:0	RW	1	Configure pre-emphasis pulse amplitude for all data rates on DDO1. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse amplitude to better match the channel loss response.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7329	OUTPUT_PARAM_CD_SD_TD_1	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_OUTPUT1_CD_SD_TD_DRIVER_SWING	13:8	RW	9	Configure output swing for all data rates on DDO1. Range: 0 to 50 decimal. Default value results in 800mVpp.
		RSVD	7:4	RW	8	Reserved — do not modify.
		RSVD	3:0	RW	0	Reserved — do not modify.
732A	OUTPUT_PARAM_CD_SD_TD_2	RSVD	15:13	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_SD_TD_PREEMPH_WIDTH	12:8	RW	2	Configure pre-emphasis pulse width for all data rates on DDO0. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse width to better match the channel loss response.
		RSVD	7:7	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_SD_TD_PREEMPH_PWRDWN	6:6	RW	0	Pre-emphasis power-down control for all data rates on DDO0: 0 = Pre-emphasis driver powered-up (pre-emphasis enabled) 1 = Pre-emphasis driver powered-down (pre-emphasis disabled)
		CFG_OUTPUT0_CD_SD_TD_PREEMPH_AMPL	5:0	RW	1	Configure pre-emphasis pulse amplitude for all data rates on DDO0. Range: 0 to 15 decimal. Adjust the pre-emphasis pulse amplitude to better match the channel loss response.
732B	OUTPUT_PARAM_CD_SD_TD_3	RSVD	15:14	RW	0	Reserved — do not modify.
		CFG_OUTPUT0_CD_SD_TD_DRIVER_SWING	13:8	RW	9	Configure output swing for all data rates on DDO0. Range: 0 to 50 decimal. Default value results in 800mV$_{pp}$.
		RSVD	7:4	RW	8	Reserved — do not modify.
		RSVD	3:0	RW	0	Reserved — do not modify.
732C	RSVD	RSVD	15:13	RW	0	Reserved — do not modify.
		RSVD	12:8	RW	2	Reserved — do not modify.
		RSVD	7:6	RW	0	Reserved — do not modify.
		RSVD	5:0	RW	1	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
732D	RSVD	RSVD	15:14	RW	0	Reserved — do not modify.
		RSVD	13:8	RW	9	Reserved — do not modify.
		RSVD	7:4	RW	8	Reserved — do not modify.
		RSVD	3:0	RW	0	Reserved — do not modify.
732E	RSVD	RSVD	15:13	RW	0	Reserved — do not modify.
		RSVD	12:8	RW	2	Reserved — do not modify.
		RSVD	7:6	RW	0	Reserved — do not modify.
		RSVD	5:0	RW	1	Reserved — do not modify.
732F	RSVD	RSVD	15:14	RW	0	Reserved — do not modify.
		RSVD	13:8	RW	9	Reserved — do not modify.
		RSVD	7:4	RW	8	Reserved — do not modify.
		RSVD	3:0	RW	0	Reserved — do not modify.
7330	RSVD	RSVD	15:13	RW	0	Reserved — do not modify.
		RSVD	12:8	RW	2	Reserved — do not modify.
		RSVD	7:6	RW	0	Reserved — do not modify.
		RSVD	5:0	RW	1	Reserved — do not modify.
7331	RSVD	RSVD	15:14	RW	0	Reserved — do not modify.
		RSVD	13:8	RW	9	Reserved — do not modify.
		RSVD	7:4	RW	8	Reserved — do not modify.
		RSVD	3:0	RW	0	Reserved — do not modify.
7332	RSVD	RSVD	15:13	RW	0	Reserved — do not modify.
		RSVD	12:8	RW	2	Reserved — do not modify.
		RSVD	7:6	RW	0	Reserved — do not modify.
		RSVD	5:0	RW	1	Reserved — do not modify.
7333	RSVD	RSVD	15:14	RW	0	Reserved — do not modify.
		RSVD	13:8	RW	9	Reserved — do not modify.
		RSVD	7:4	RW	8	Reserved — do not modify.
		RSVD	3:0	RW	0	Reserved — do not modify.
7334	RSVD	RSVD	15:0	RW	24	Reserved — do not modify.
7335	RSVD	RSVD	15:0	RW	112	Reserved — do not modify.
7336	RSVD	RSVD	15:0	RW	24	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7337	RSVD	RSVD	15:0	RW	112	Reserved — do not modify.
7338	RSVD	RSVD	15:0	RW	24	Reserved — do not modify.
7339	RSVD	RSVD	15:0	RW	112	Reserved — do not modify.
733A	RSVD	RSVD	15:0	RW	24	Reserved — do not modify.
733B	RSVD	RSVD	15:0	RW	112	Reserved — do not modify.
733C	RSVD	RSVD	15:0	RW	3AE	Reserved — do not modify.
733D	RSVD	RSVD	15:0	RW	FC	Reserved — do not modify.
733E	RSVD	RSVD	15:0	RW	3AE	Reserved — do not modify.
733F	RSVD	RSVD	15:0	RW	FC	Reserved — do not modify.
7340	RSVD	RSVD	15:0	RW	2E	Reserved — do not modify.
7341	RSVD	RSVD	15:0	RW	D0	Reserved — do not modify.
7342	RSVD	RSVD	15:0	RW	2E	Reserved — do not modify.
7343	RSVD	RSVD	15:0	RW	D0	Reserved — do not modify.
7344	RSVD	RSVD	15:0	RW	3AE	Reserved — do not modify.
7345	RSVD	RSVD	15:0	RW	FA	Reserved — do not modify.
7346	RSVD	RSVD	15:0	RW	3AE	Reserved — do not modify.
7347	RSVD	RSVD	15:0	RW	FA	Reserved — do not modify.
7348	OUTPUT_SIG_SELECT	RSVD	15:11	RW	0	Reserved — do not modify.
		RSVD	10:8	RW	1	Reserved — do not modify.
		RSVD	7:4	RW	0	Reserved — do not modify.
		CTRL_OUTPUT0_DATA_INVERT	3:3	RW	0	Controls optional signal polarity inversion on output 0.
		CTRL_OUTPUT1_DATA_INVERT	2:2	RW	0	Controls optional signal polarity inversion on output 1 when data is selected (CTRL_OUTPUT1_SIGNAL_SEL = 0).
		RSVD	1:1	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_SIGNAL_SEL	0:0	RW	0	Output 1 data/clock select: 0 = Data 1 = Clock (CDR recovered clock) Clock output is half rate of the recovered clock.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7349	CONTROL_ OUTPUT_ MUTE	RSVD	15:6	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_AUTO _MUTE_DURING_RATE _SEARCH	5:5	RW	0	Auto mode control: 0 = Disable auto mode 1 = Enable auto mode during rate search When enabled, the output is muted during rate search or loss of signal.
		CTRL_OUTPUT0_AUTO _MUTE_DURING_RATE _SEARCH	4:4	RW	0	Auto mode control: 0 = Disable auto mode 1 = Enable auto mode during rate search When enabled, the output is muted during rate search or loss of signal.
		CTRL_OUTPUT1_ MANUAL_MUTE	3:3	RW	0	0 = Unmute 1 = Mute Controls mute for output 1 when CTRL_OUTPUT1_AUTO _MUTE is disabled.
		CTRL_OUTPUT1_AUTO _MUTE	2:2	RW	1	0 = Disable auto mode 1 = Enable auto mode Selects between auto or manual mute control for output 1.
		CTRL_OUTPUT0_ MANUAL_MUTE	1:1	RW	0	0 = Unmute 1 = Mute Controls mute for output 1 when CTRL_OUTPUT0_AUTO _MUTE is disabled
		CTRL_OUTPUT0_AUTO _MUTE	0:0	RW	1	0 = Disable auto mode 1 = Enable auto mode Selects between auto or manual mute control for output 1.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
734A	CONTROL_ OUTPUT_ DISABLE	RSVD	15:4	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_ MANUAL_DISABLE	3:3	RW	0	0 = Enable output driver. 1 = Disable (power-down) output driver. Controls output disable for output 1 when CTRL_OUTPUT1_AUTO _DISABLE is disabled.
		CTRL_OUTPUT1_AUTO _DISABLE	2:2	RW	0	0 = Disable auto output disable mode. 1 = Enable auto output disable mode. Selects between auto or manual output disable for output 1. Disable mode overrides mute mode.
		CTRL_OUTPUT0_ MANUAL_DISABLE	1:1	RW	0	0 = Enable output driver. 1 = Disable (power-down) output driver. Controls output disable for output 1 when CTRL_OUTPUT1_AUTO _DISABLE is disabled.
		CTRL_OUTPUT0_AUTO _DISABLE	0:0	RW	0	0 = Disable auto output disable mode. 1 = Enable auto output disable mode. Selects between auto or manual output disable for output 0. Disable mode overrides mute mode.
734B	RSVD	RSVD	15:11	RW	0	Reserved — do not modify.
		RSVD	10:9	RW	2	Reserved — do not modify.
		RSVD	8:8	RW	1	Reserved — do not modify.
		RSVD	7:3	RW	0	Reserved — do not modify.
		RSVD	2:1	RW	2	Reserved — do not modify.
		RSVD	0:0	RW	1	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
734C	CONTROL_ RETIMER_ BYPASS	RSVD	15:4	RW	0	Reserved — do not modify.
		CTRL_OUTPUT1_ RETIMER_MANUAL_ BYPASS	3:3	RW	0	0 = Disable re-timer bypass 1 = Enable re-timer bypass Controls re-timer bypass for output 1 when CTRL_OUTPUT1_ RETIMER_AUTO_BYPASS is disabled.
		CTRL_OUTPUT1_ RETIMER_AUTO_BYPASS	2:2	RW	1	0 = Disable auto mode 1 = Enable auto mode Selects between auto and manual control of re-timer bypass for output 1.
		CTRL_OUTPUT0_ RETIMER_MANUAL_ BYPASS	1:1	RW	0	0 = Disable re-timer bypass 1 = Enable re-timer bypass Controls re-timer bypass for output 0 when CTRL_OUTPUT1_ RETIMER_AUTO_BYPASS is disabled.
		CTRL_OUTPUT0_ RETIMER_AUTO_BYPASS	0:0	RW	1	0 = Disable auto mode 1 = Enable auto mode Selects between auto and manual control of re-timer bypass for output 0.
734D to 734F	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7350	RSVD	RSVD	15:0	RW	C	Reserved — do not modify.
7351	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7352	RSVD	RSVD	15:0	RW	180	Reserved — do not modify.
7353 to 7356	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
7357	RSVD	RSVD	15:0	RW	40	Reserved — do not modify.
7358 to 7359	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.
735A	RSVD	RSVD	15:0	RW	3F8	Reserved — do not modify.
735B	RSVD	RSVD	15:0	RW	A	Reserved — do not modify.
735C	RSVD	RSVD	15:0	RW	2FE	Reserved — do not modify.
735D to 737C	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-3: Register Descriptions (Continued)

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
737D	CFG_ACM	RSVD	15:9	RW	0	Reserved — do not modify.
		CFG_SD_JIT	8:8	RW	0	To reduce SD output jitter, set this bit to 1. It is recommended to set this bit to 0 for all other rates, although certain applications may benefit with this set to 1 for all rates. After changing this bit, there must be a change in carrier detect. To force a change in carrier detect, remove input signal or set CFG_CLI_SQUELCH_THRESHOLD = 0, and CFG_SEC_CD_INCL_CLI_SQUELCH=1.
		RSVD	7:0	RW	31	Reserved — do not modify.
737E to 737F	RSVD	RSVD	15:0	RW	0	Reserved — do not modify.

Table 5-4: Status Descriptions

The registers in Table 5-4 are status registers and should not be written to, otherwise the status data will be invalid.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Description
7380 to 7382	RSVD	RSVD	15:0	RW	Reserved — do not modify.
7383	DEVICE_ID	DEVICE_ID_REG	15:12	RW	Device Identification: 0 = GS12181 1 = GS12141
		RSVD	11:0	RW	Reserved — do not modify.
7384	STICKY_ COUNTS_0	STAT_CNT_PRI_CD _CHANGES	15:8	RW	Count of primary carrier detection status changes (i.e. ignoring CLI squelch).
		STAT_CNT_SEC_CD _CHANGES	7:0	RW	Count of secondary carrier detection status changes (i.e. taking into account CLI squelch).
7385	STICKY_ COUNTS_1	STAT_CNT_RATE _CHANGES	15:8	RW	Count of rate changes.
		STAT_CNT_PLL_LOCK_CH ANGES	7:0	RW	Count of PLL lock status changes since last cleared.

Table 5-4: Status Descriptions (Continued)

The registers in Table 5-4 are status registers and should not be written to, otherwise the status data will be invalid.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Description
7386	CURRENT_STATUS_0	RSVD	15	RW	Reserved — do not modify.
		STAT_CLEAR_COUNTS_STATUS	14:13	RW	0 = Idle 1 = Reserved 2 = Indicates device has cleared the sticky counts 3 = Reserved Part of a four way handshake with CTRL_CLEAR_COUNTS (register 4). When STAT_CLEAR_COUNTS _STATUS = 0 (idle), host may clear sticky counts by setting CTRL_CLEAR_COUNTS = 1. Once the device reports STAT_CLEAR _COUNTS_STATUS = 2 (cleared), the host must reset CTRL_CLEAR _COUNTS to 0 for the device to reset STAT_CLEAR_COUNTS _STATUS to 0 (idle).
		STAT_LOCK	12:12	RW	0 = PLL is unlocked 1 = PLL is locked
		RSVD	11:9	RW	Reserved — do not modify.
		STAT_CLI_SQUELCH	8:8	RW	0 = CLI squelch is de-asserted 1 = CLI squelch is asserted CLI squelch status.
		STAT_OUTPUT1_MODE	7:4	RW	00 = All Trace Driver rates 01 = Reserved 02 = Reserved 03 = Reserved 04 = Reserved 05 = Reserved 06 = Muted 07 = Disabled
		STAT_OUTPUT0_MODE	3:0	RW	See STAT_OUTPUT1_MODE.

Table 5-4: Status Descriptions (Continued)

The registers in Table 5-4 are status registers and should not be written to, otherwise the status data will be invalid.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Description
7387	CURRENT_STATUS_1	STAT_OUTPUT1_DISABLE	15:15	RW	0 = Output 1 is not disabled 1 = Output 1 is disabled
		STAT_OUTPUT0_DISABLE	14:14	RW	0 = Output 1 is not disabled 1 = Output 1 is disabled
		STAT_OUTPUT1_MUTE	13:13	RW	0 = Output 1 is not muted 1 = Output 1 is muted
		STAT_OUTPUT0_MUTE	12:12	RW	0 = Output 1 is not muted 1 = Output 1 is muted
		STAT_OUTPUT1_RETIMER_BYPASS	11:11	RW	0 = Re-timer path to output 1 is not bypassed 1 = Re-timer path to output 1 is bypassed
		STAT_OUTPUT0_RETIMER_BYPASS	10:10	RW	0 = Re-timer path to output 1 is not bypassed 1 = Re-timer path to output 1 is bypassed
		STAT_SEC_CD	9:9	RW	0 = Secondary carrier is not detected 1 = Secondary carrier is detected Secondary carrier detection status (optionally taking into account CLI squelch).
		STAT_PRI_CD	8:8	RW	0 = Primary carrier is not detected 1 = Primary carrier is detected Primary carrier detection status (ignoring CLI squelch).
		STAT_CEQ_BYPASS	7:7	RW	0 = CEQ is not bypassed 1 = CEQ is bypassed
		STAT_OUTPUT1_RATE_MODE	6:5	RW	2 = UHD rate mode
		STAT_OUTPUT0_RATE_MODE	4:3	RW	2 = UHD rate mode
		STAT_DETECTED_RATE	2:0	RW	0 = Unlocked 1 = MADI (125Mb/s) 2 = SD (270Mb/s) 3 = HD (1.485Gb/s) 4 = 3G (2.97Gb/s) 5 = 6G (5.94Gb/s) 6 = 12G (11.88Gb/s) 7 = Reserved
7388	EQ_GAIN_IND	RSVD	15:8	RW	Reserved — do not modify.
		STABLE_CABLE_LEN_INDICATION	7:0	RW	00 to 40 = Cable length indication FF = Unknown cable length
7389 to 7390	RSVD	RSVD	15:0	RW	Reserved — do not modify.

6. Application Information

6.1 Typical Application Circuit

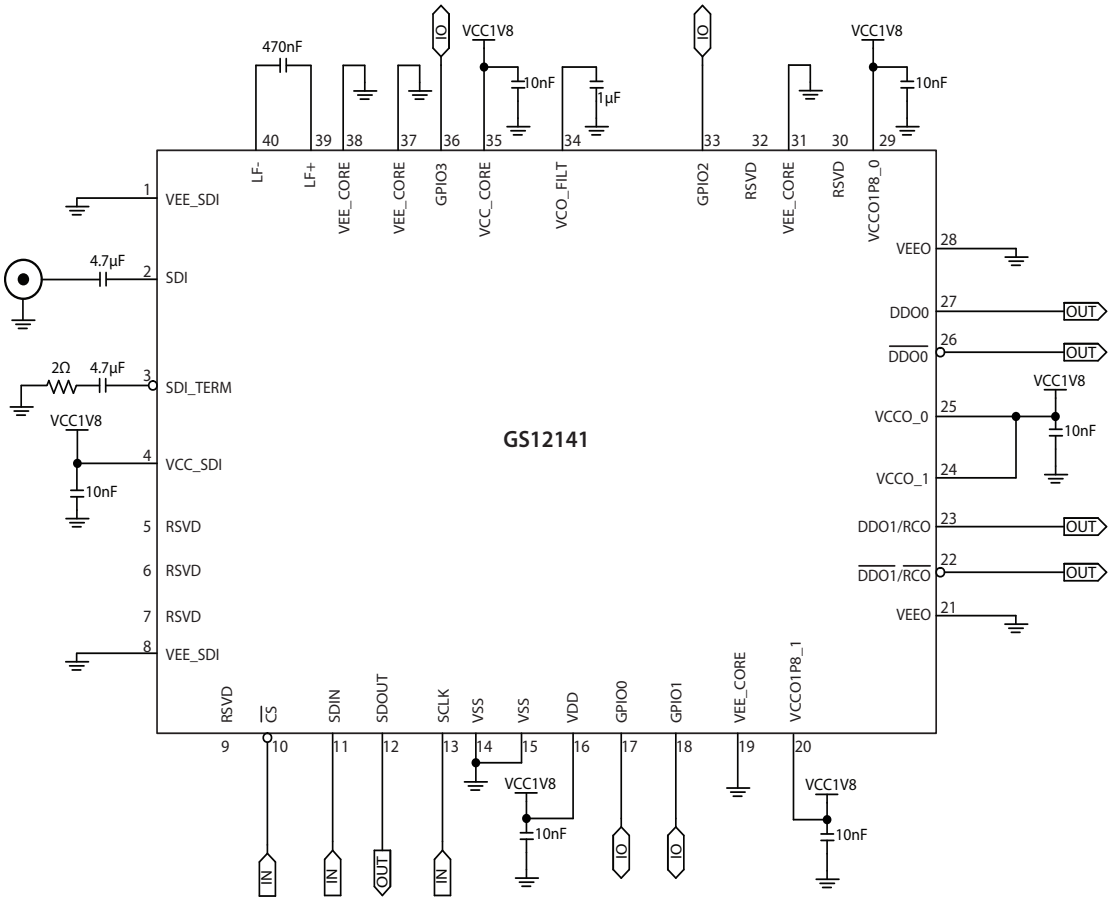


Figure 6-1: Typical Application Circuit

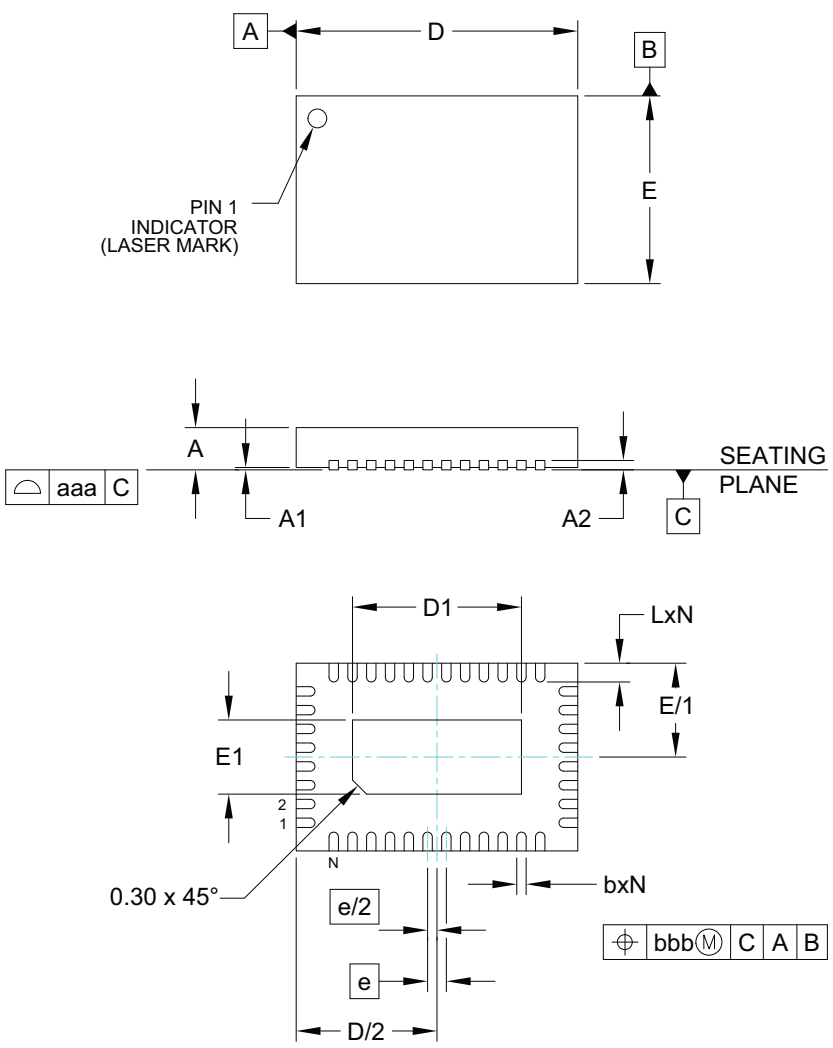
Note 1: 4.7µF AC-coupling capacitors are required on DDO0/$\overline{\text{DDO0}}$ and DDO1/RCO/$\overline{\text{DDO1}}$/$\overline{\text{RCO}}$ when the downstream IC has an input common mode range that is incompatible with the output common mode range of the GS12141.

Note 2: VCCO_0 and VCCO_1 can be tied to two independent supplies running different voltages.

Note 3: Although 1µF AC-coupling capacitors may be adequate at the input of SDI for most applications, it is recommended to use 4.7µF capacitors for increased margin to pathological signals.

7. Package & Ordering Information

7.1 Package Dimensions



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		(0.02)	
b	0.15	0.20	0.25
D	5.95	6.00	6.05
D1	3.45	3.60	3.70
E	3.95	4.00	4.05
E1	1.43	1.58	1.68
e	0.40 BSC		
L	0.30	0.40	0.50
N	40		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DIMENSION OF LEAD WIDTH APPLIES TO TERMINAL AND IS MEASURED BETWEEN 0.15 to 0.30mm FROM THE TERMINAL TIP.

Figure 7-1: Package Dimensions

7.2 Recommended PCB Footprint

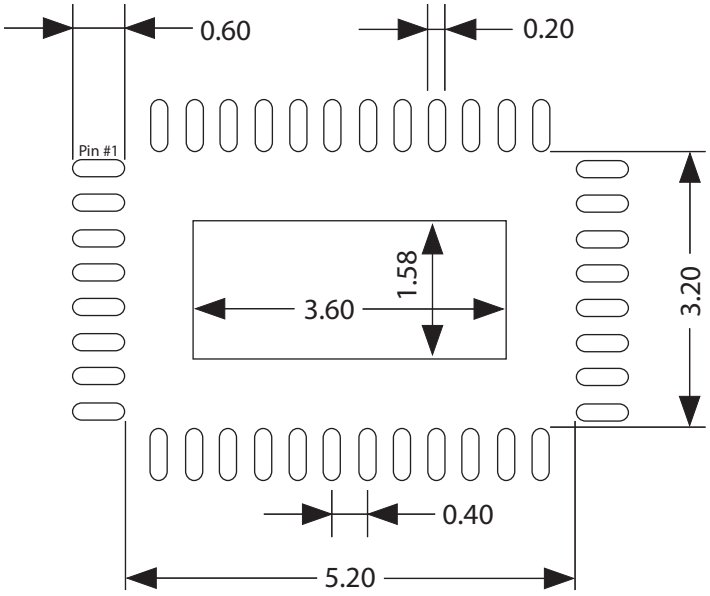


Figure 7-2: Recommended PCB Footprint

7.3 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	6mm x 4mm 40-pin QFN
Moisture Sensitivity Level	3
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	40.0°C/W
Junction to Board Thermal Resistance, θ_{j-b}	32.0°C/W
Junction to Case Thermal Resistance, θ_{j-c}	36.0°C/W
Psi, Ψ – Junction-to-Top Characterization Parameter	<1.0°C/W
Pb-free and RoHS compliant	Yes

7.4 Marking Diagram

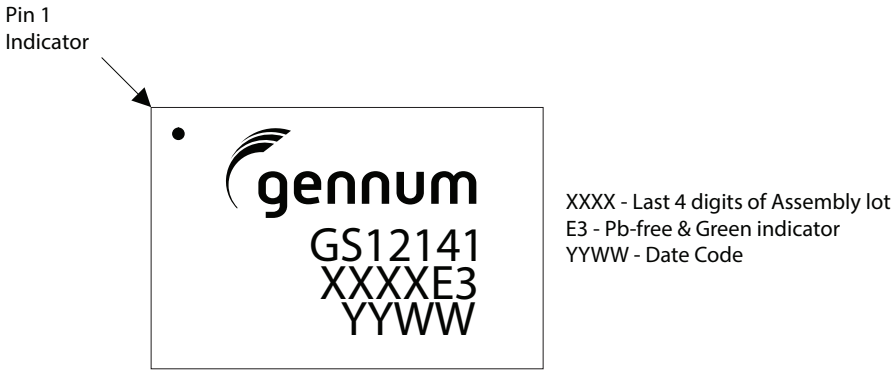


Figure 7-3: Marking Diagram

7.5 Solder Reflow Profiles

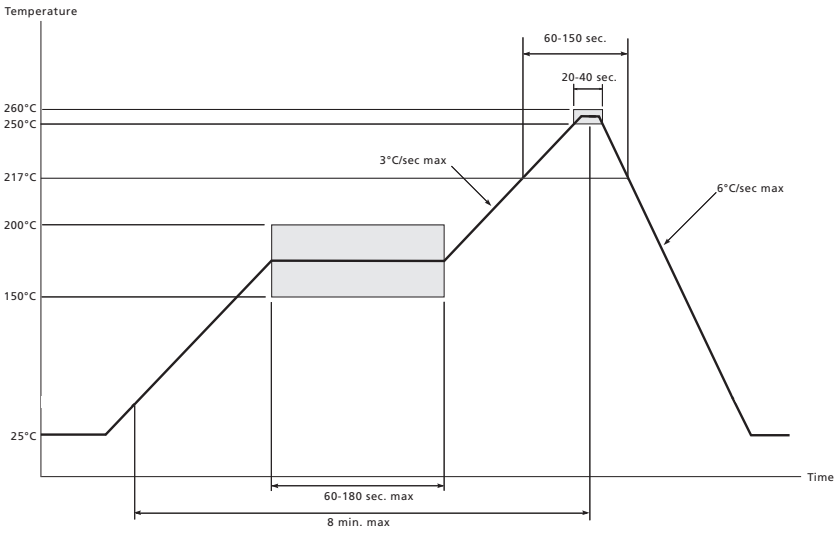


Figure 7-4: Maximum Pb-free Solder Reflow Profile

7.6 Ordering Information

Table 7-2: Ordering Information

Part Number	Minimum Order Quantity	Format
GS12141-INE3	490	Tray
GS12141-INTE3	250	Tape and Reel
GS12141-INTE3Z	2500	Tape and Reel

Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
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