

PROTECTION PRODUCTS

Description

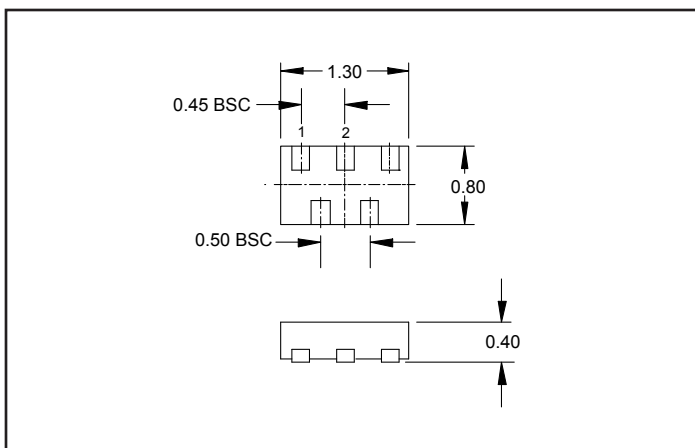
RailClamp® TVS arrays are ultra low capacitance ESD protection devices designed to protect high speed data interfaces. This series has been specifically engineered to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

The RClamp®7524T will protect four lines or two differential pairs. Each line has a maximum capacitance of only 0.60pF between any I/O pin and ground.

This allows it to be used on circuits operating in excess of 5GHz without signal attenuation. They feature high maximum ESD withstand voltage of +/- 25kV contact, +/-30kV air discharge per IEC 61000-4-2.

The RClamp7524T is in a 5-pin SLP1308N5T package. It measures 1.3 x 0.8mm with a nominal height of 0.40mm. The innovative flow through package design simplifies PCB layout and allows matched trace lengths for consistent impedance between high speed differential lines. The combination of small size, low capacitance, and high level of ESD protection makes this device a flexible solution for applications such as HDMI, MHL, MDDI, and eDP interfaces.

Package Dimension



Features

- ESD protection for high-speed data lines to IEC 61000-4-2 (ESD) $\pm 30\text{kV}$ (air), $\pm 25\text{kV}$ (contact)
- IEC 61000-4-5 (Lightning) 5A (8/20 μs)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- Package design optimized for high speed lines
- Flow-Through design
- Protects four high-speed lines
- Low capacitance: 0.60pF Maximum (I/O to Ground)
- Low ESD clamping voltage
- Low dynamic resistance: 0.50 Ohms (Typ)
- Solid-state silicon-avalanche technology

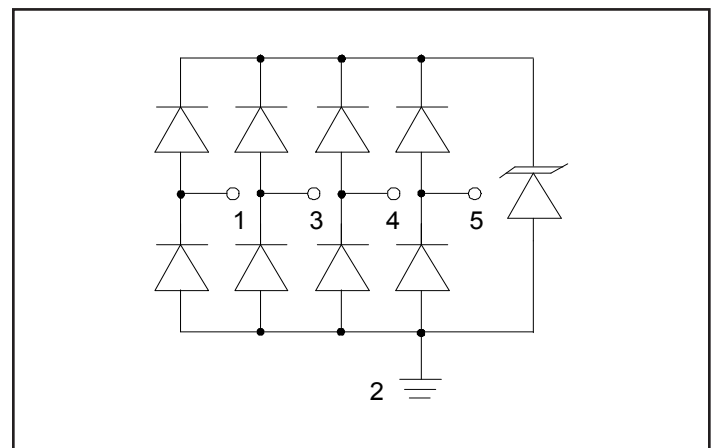
Mechanical Characteristics

- SLP1308N5T 5-pin package (1.3 x 0.8 x 0.40mm)
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Lead Pitch: 0.45mm
- Lead finish: NiPdAu
- Marking: Marking Code
- Packaging: Tape and Reel

Applications

- HDMI 1.3 and HDMI 1.4
- V-By-One
- USB 3.0
- MHL
- eDP
- LVDS Interfaces
- eSATA Interfaces

Schematic & Pin Configuration



Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P _{PK}	75	W
Peak Pulse Current (tp = 8/20μs)	I _{PP}	5	A
ESD per IEC 61000-4-2 (Air) ⁽¹⁾ ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V _{ESD}	±30 ±25	kV
Operating Temperature	T _J	-55 to +125	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

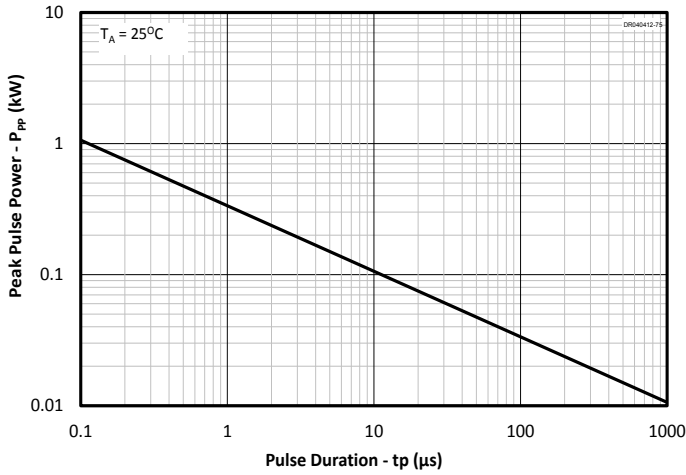
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}	Any I/O to GND			5	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} = 1mA, Any I/O to GND	6.5	9	11	V
Reverse Leakage Current	I _R	V _{RWM} = 5V, Any I/O to GND		5	100	nA
Clamping Voltage	V _C	tp = 8/20μs Any I/O to GND	I _{PP} = 1A		12	V
			I _{PP} = 5A		15	
ESD Clamping Voltage ²	V _C	tp = 0.2/100ns Any I/O to GND	I _{TLP} = 4A	11		V
			I _{TLP} = 16A	17		
Dynamic Resistance ^{2,3}	R _{DYN}	tp = 0.2/100ns		0.5		Ω
Junction Capacitance	C _J	V _R = 0V, f = 1MHz	Any I/O to GND	0.5	0.6	pF
			Between I/O pins	0.25	0.4	

Notes

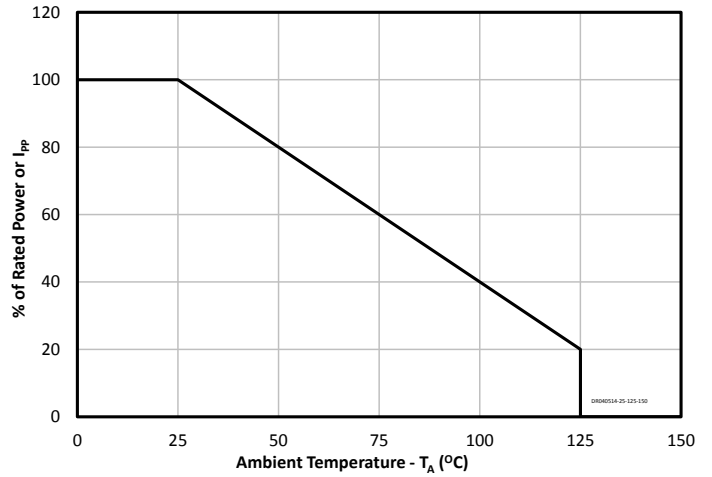
- 1) Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.
- 2) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t1 = 70ns to t2 = 90ns.
- 3) Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

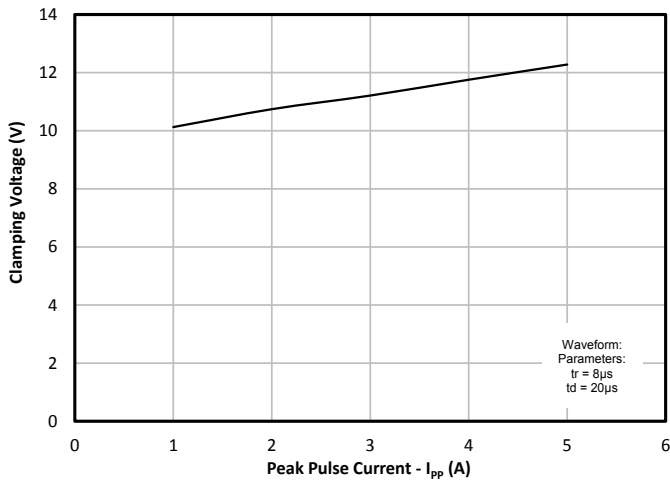
Non-Repetitive Peak Pulse Power



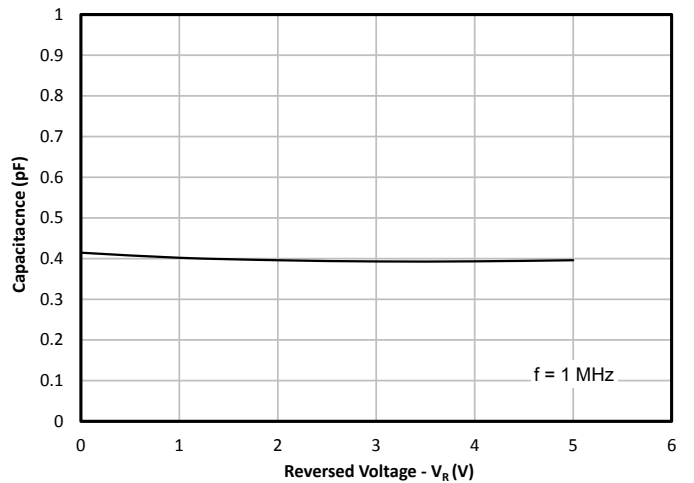
Power Derating Curve



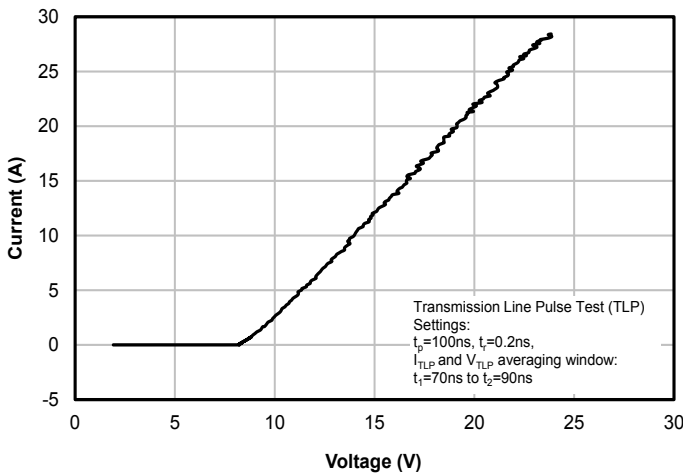
Clamping Voltage vs. Peak Pulse Current (Between any I/O and Ground)



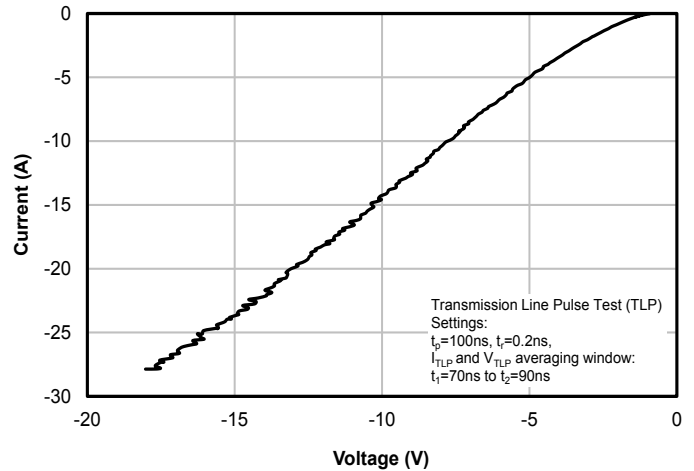
Junction Capacitance vs. Reverse Voltage (Between any I/O and Ground)



TLP Characteristic (Positive)

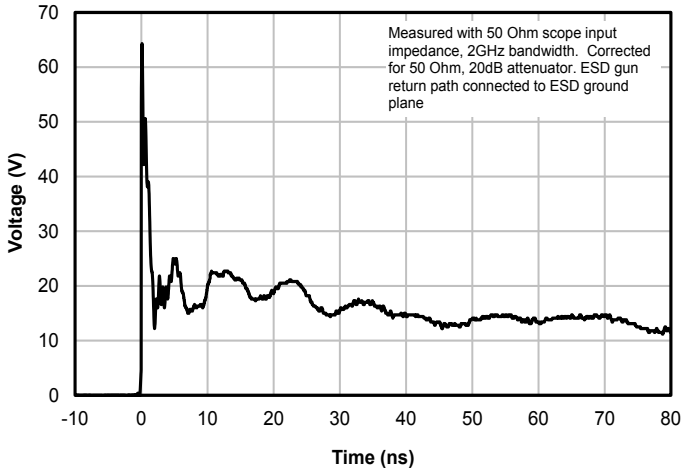


TLP Characteristic (Negative)

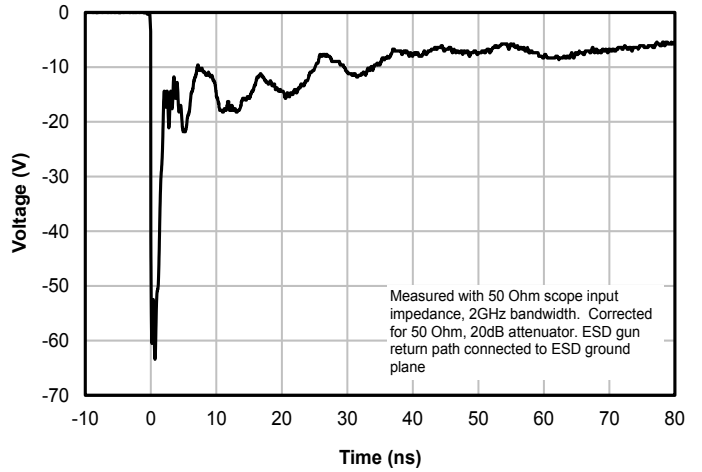


Typical Characteristics (Continued)

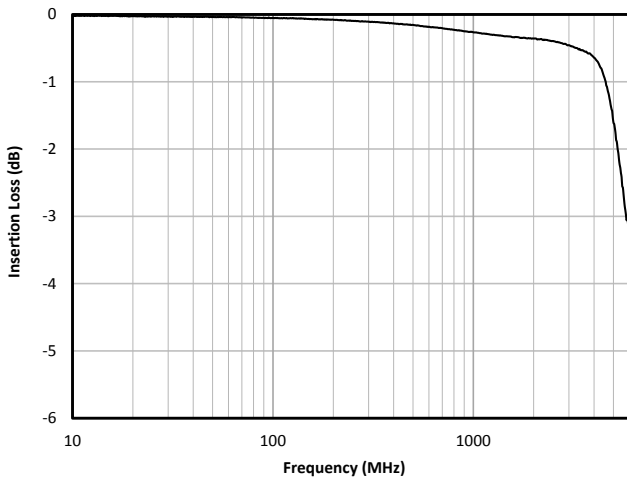
**ESD Clamping (+8kV Contact per IEC 614000-4-2)
(Between any I/O to Ground)**



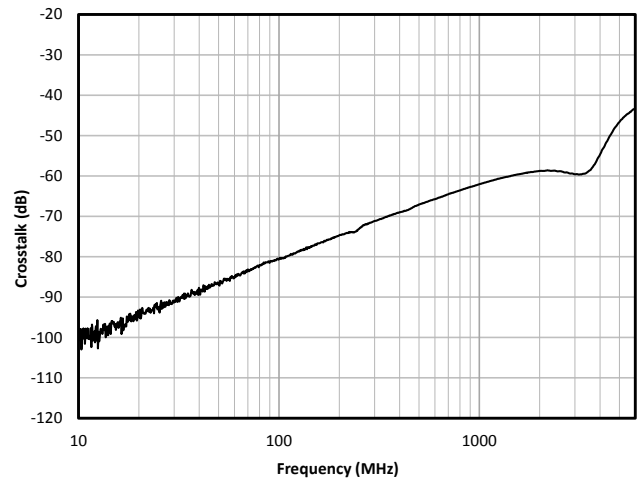
**ESD Clamping (-8kV Contact per IEC 614000-4-2)
(Between any I/O to Ground)**



Typical Insetion Loss S21



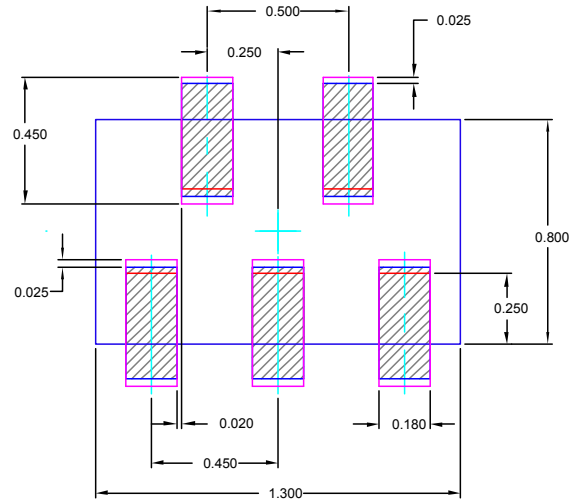
Analog Crosstalk




Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. The table below provides Semtech's recommended assembly guidelines for mounting this device. The figure at the right details Semtech's recommended aperture based on the below recommendations. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. The exact manufacturing parameters will require some experimentation to get the desired solder application.



All Dimensions are in mm.

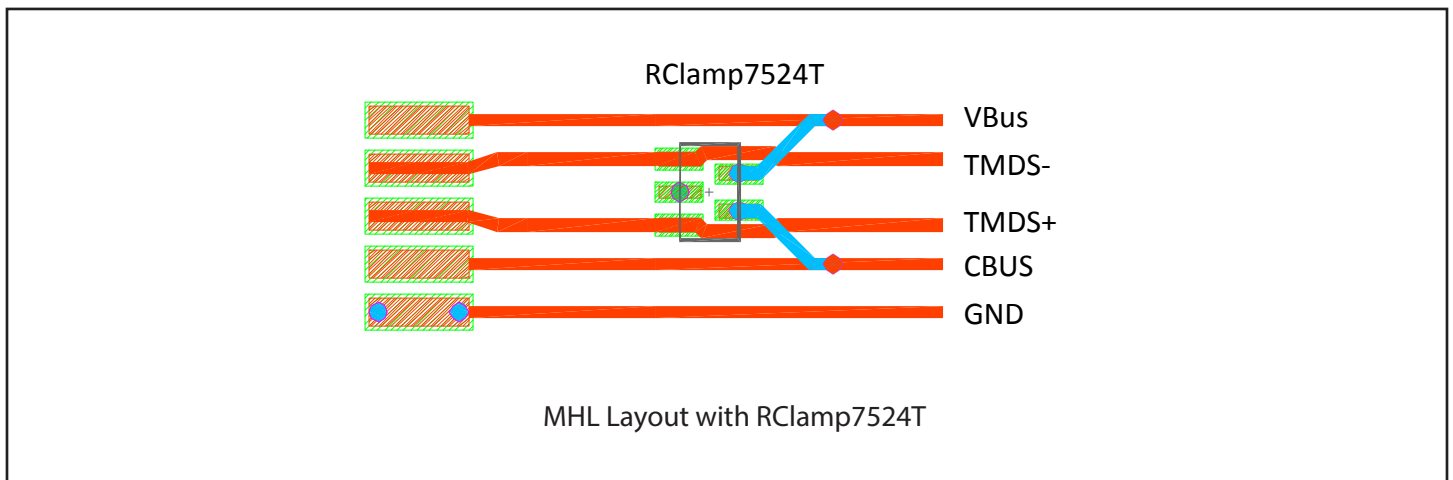
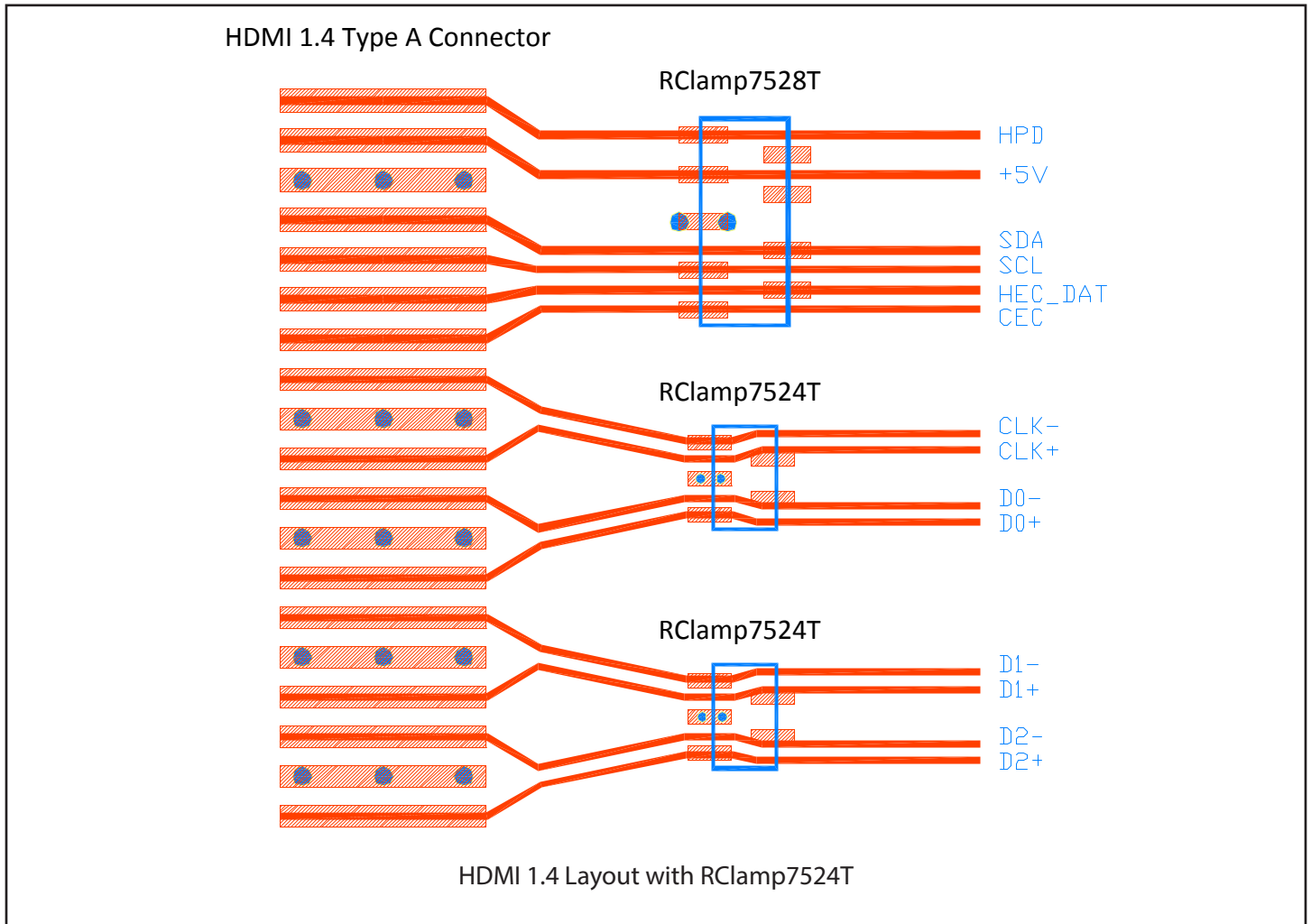
 Land Pad.  Stencil opening  Component

Recommended Mounting Pattern

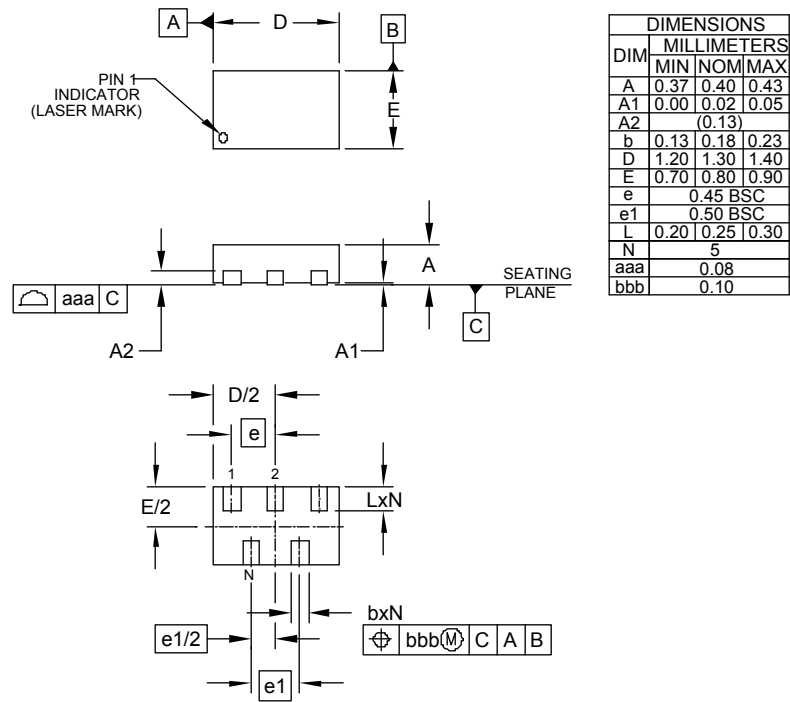
Assembly Parameter	Recommendation
Solder Stencil Design	Laser cut, Electro-polished
Aperture shape	Rectangular
Solder Stencil Thickness	0.100 mm (0.004")
Solder Paster Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Non-Solder mask defined
PCB Pad Finish	OSP Or NiAu

Application Information

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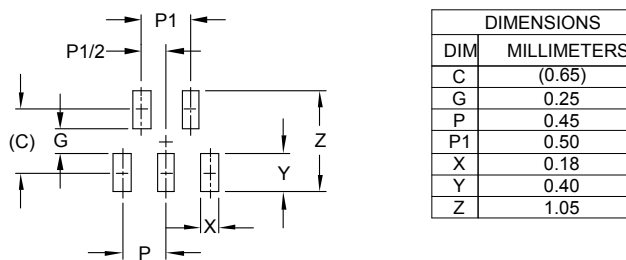


Outline Drawing - SLP1308N5T



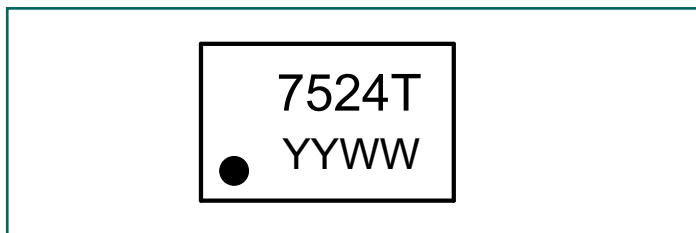
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

Land Pattern - SLP1308N5T



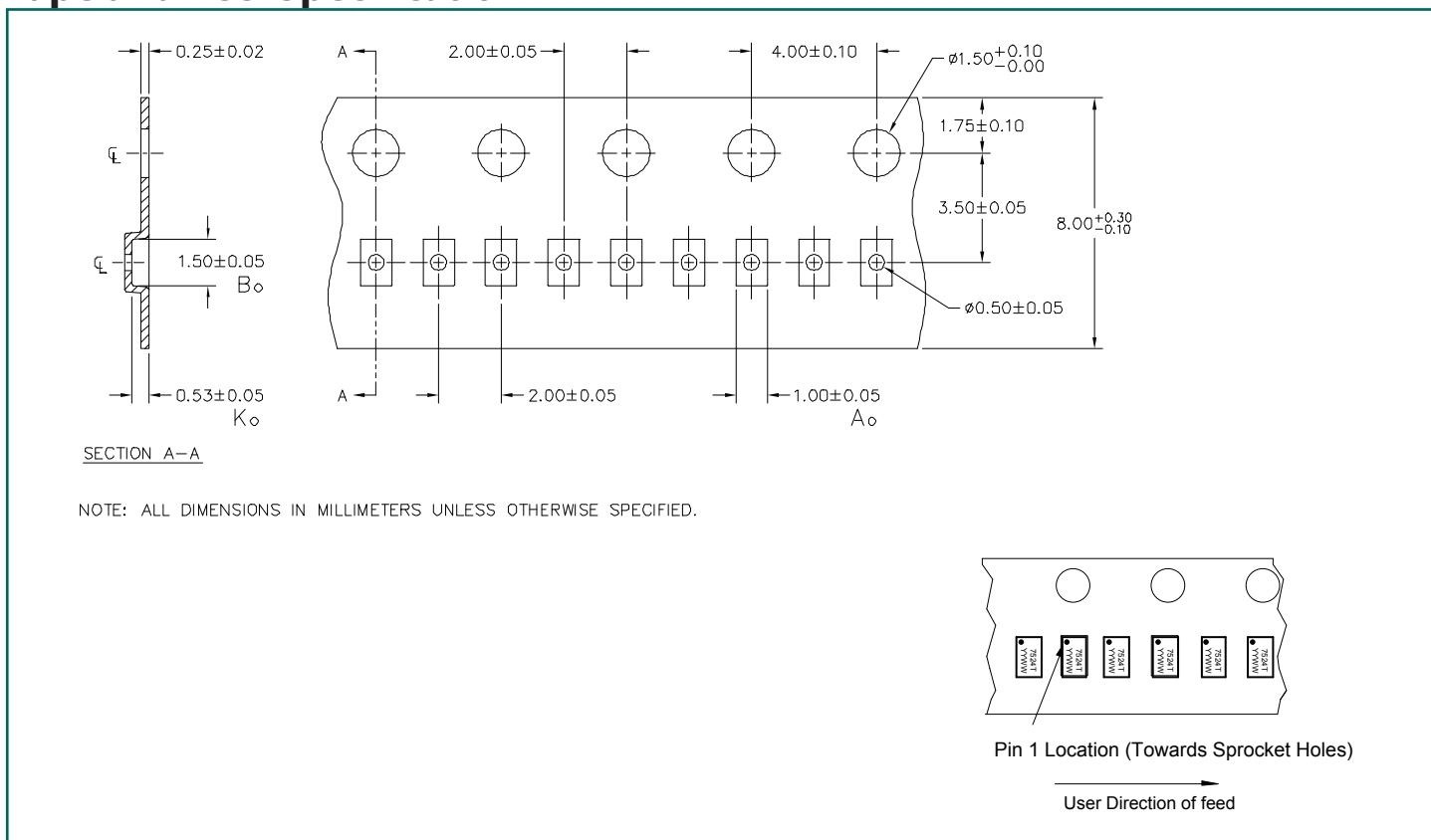
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Note: YYWW = Date Code

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp7524T.TNT	10,000	7"



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