SC1101
Asynchronous Voltage Mode PWM Controller

POWER MANAGEMENT

Description

The SC1101 is a versatile, low-cost, voltage-mode PWM controller designed for low output voltage DC/DC power supply applications. A simple, fixed-voltage buck regulator can be implemented using the SC1101 with a minimum of external components. Internal level shift and drive circuitry eliminates the need for an expensive p-channel, high-side switch. The small device footprint allows for compact circuit design.

SC1101 features include a temperature compensated voltage reference, triangle wave oscillator, current limit comparator, frequency shift over-current protection, and an internally compensated error amplifier. Pulse by pulse current limiting is implemented by sensing the differential voltage across an external resistor, or an appropriately sized PC board trace.

The SC1101 operates at a fixed frequency of 200kHz, providing an optimum compromise between efficiency, external component size, and cost.

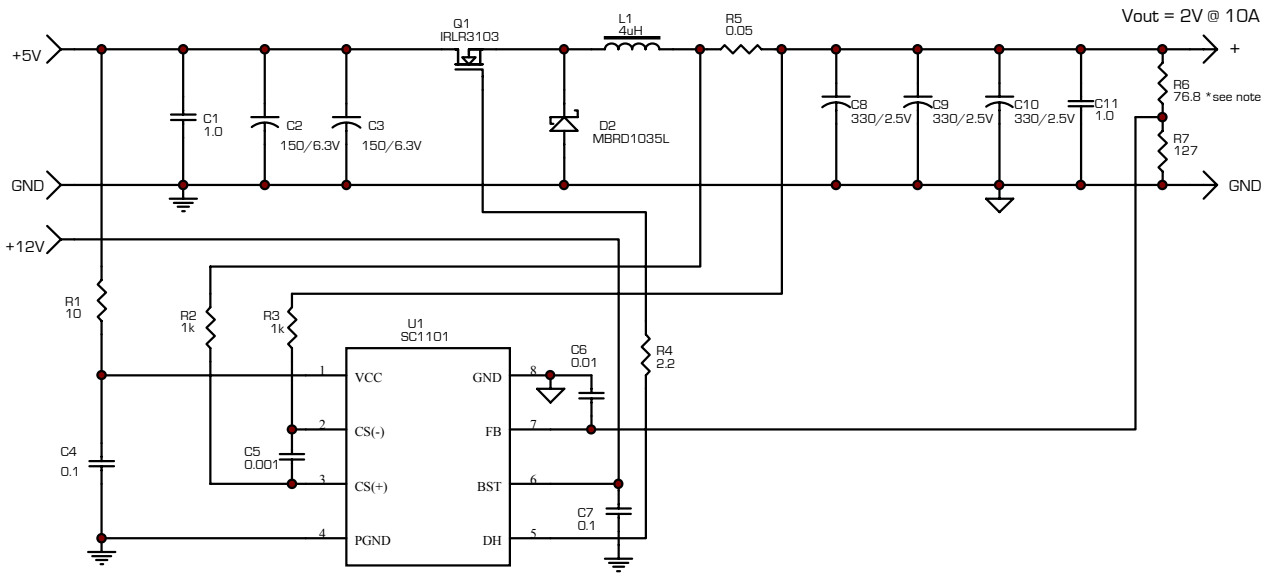
Features

- Low cost / small size
- Switch mode efficiency up to 95%
- 1% reference voltage accuracy
- Over current protection
- 500mA output drive
- SO-8 package

Applications

- Pentium® P55 Core Supply
- Low Cost Microprocessor Supplies
- Peripheral Card Supplies
- Industrial Power Supplies
- High Density DC/DC Conversion

Typical Application Circuit



*** NOTE:**
R6 = R7 x (Vout/1.25 - 1) rounded to nearest 1%value

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Input Voltage	V_{CC} to GND	-0.3 to +7	V
Ground Differential	P_{GND} to GND	± 1	V
Boost Input Voltage	BST to GND	-0.3 to +15	V
Operating Ambient Temperature Range	T_{AMB}	0 to +70	°C
Storage Temperature Range	T_{STG}	-45 to 125	°C
Maximum Junction Temperature	T_J	125	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
Thermal Resistance Junction to Ambient	θ_{JA}	165	°C/W
Thermal Resistance Junction to Case	θ_{JC}	40	°C/W

Electrical Characteristics

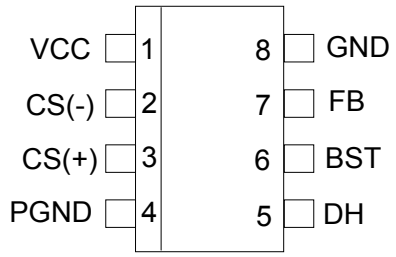
Unless specified: V_{CC} = 4.75 to 5.25, GND = P_{GND} = 0V, V_O = 2.5V, T_A = 25°C, BST = 12V.
Per test circuit, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reference	V_{REF}		1.238	1.250	1.263	V
		Over 0 to 125°C Temp. range	1.225	1.250	1.275	
Feedback Bias Current	I_{FB}			2.0	8.0	uA
Quiescent Current	I_Q	Current into V_{CC} pin		5.0	8.0	mA
Load Regulation		I_O = 1A to 10A		0.5	1.0	%
Line Regulation		I_O = 10A			0.5	%
Current Limit Threshold		CS(+) to CS(-)	60	70	80	mV
Oscillator Frequency			170	200	230	kHz
Oscillator Frequency Shift		$V_{FB} < V_{REF}/2$		50		kHz
Max Duty Cycle			90	95		%
DH Sink/Source Current	I_O	$V_{BST} - V_{DH}$ = 4.5V / $V_{DH} - V_{PGND}$ = 2V	500			mA
UVLO Threshold	V_{UVLO}			3.8		V

Note:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Pin Configuration

Top View



(8 Lead Plastic SOIC)

Ordering Information

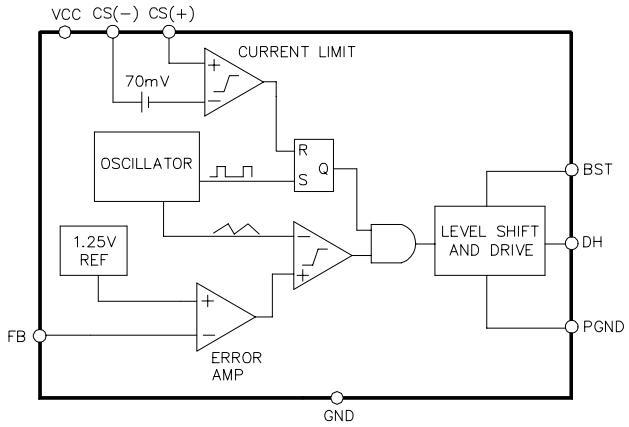
Device (1)	Package	Temp Range (T_J)
SC1101CS.TR	SO-8	0° to 125°C
SC1101CSTRT(2)		

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin Number	Pin Name	Pin Function
1	VCC	Device input voltage.
2	CS(-)	Current sense input (Negative) .
3	CS(+)	Current sense input (Positive) .
4	PGND	Device power ground .
5	DH	High side driver output .
6	BST	High side driver V_{CC} (Boost) .
7	FB	Error amplifier input (-) .
8	GND	Signal ground .

Block Diagram



Applications Information

Layout Guidelines

Careful attention to layout requirements are necessary for successful implementation of the SC1101 PWM controller. High currents switching at 200kHz are present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used, the number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, for example the input capacitor and bottom Schottky ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q1) and the Schottky (D1) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will reduce EMI, lower ground injection currents, resulting in electrically “cleaner” grounds for the rest of the system and minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of Q1, D1 and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. The connection between the output inductor and the sense resistor should be a wide trace or copper area, there are no fast voltage or current transitions in this connection and length is not so important, however adding unnecessary impedance will reduce efficiency.

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible, fast transient load currents are supplied by Cout only, and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC1101 is best placed over an isolated ground plane area. GND and PGND should be returned to this isolated ground. This isolated ground area should be connected to the main ground by a trace that runs from the GND pin to the ground side of (one of) the output capacitor(s). If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, D1 loop. Under no circumstances should GND be returned to a ground inside the Cin, Q1, D1 loop.

6) Vcc for the SC1101 should be supplied from the 5V supply through a 10Ω resistor, the Vcc pin should be decoupled directly to GND by a 0.1µF ceramic capacitor, trace lengths should be as short as possible.

7) The Current Sense resistor and the divider across it should form as small a loop as possible, the traces running back to CS(+) and CS(-) on the SC1101 should run parallel and close to each other.

8) To minimize noise pickup at the sensitive FB pin, the feedback resistors should both be close to the SC1101 with the bottom resistor (Rb) returned to ground at the GND pin.

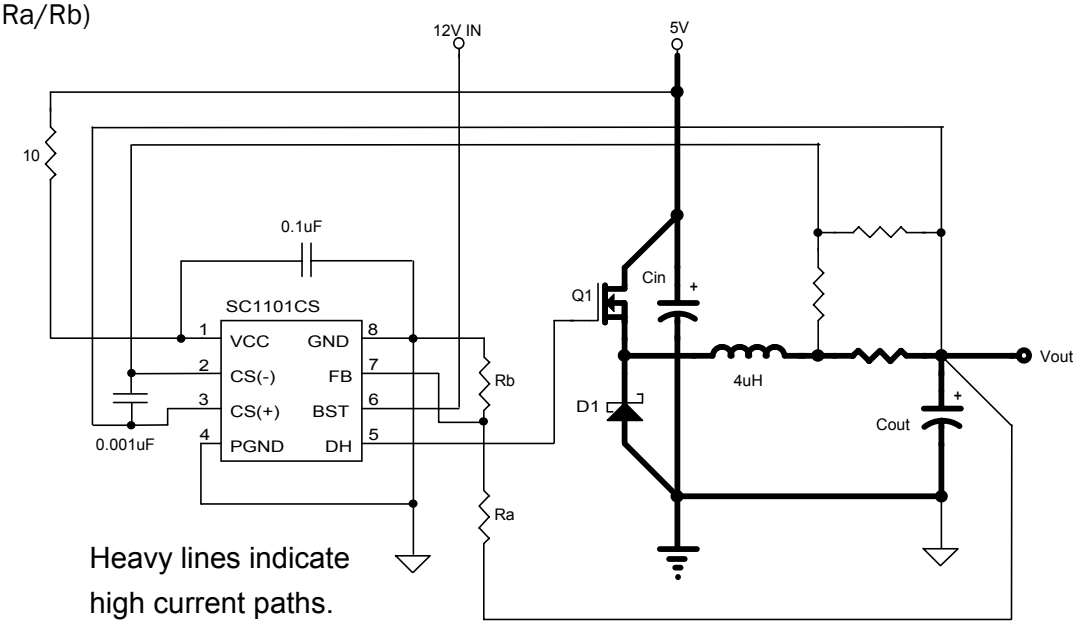
Under Voltage Lockout

The under voltage lockout circuit of the SC1101 assures that the high-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below set parameters. Lockout occurs if V_{CC} falls below 3.8V. Normal operation resumes once V_{CC} rises above 3.8V.

Applications Information (Cont.)

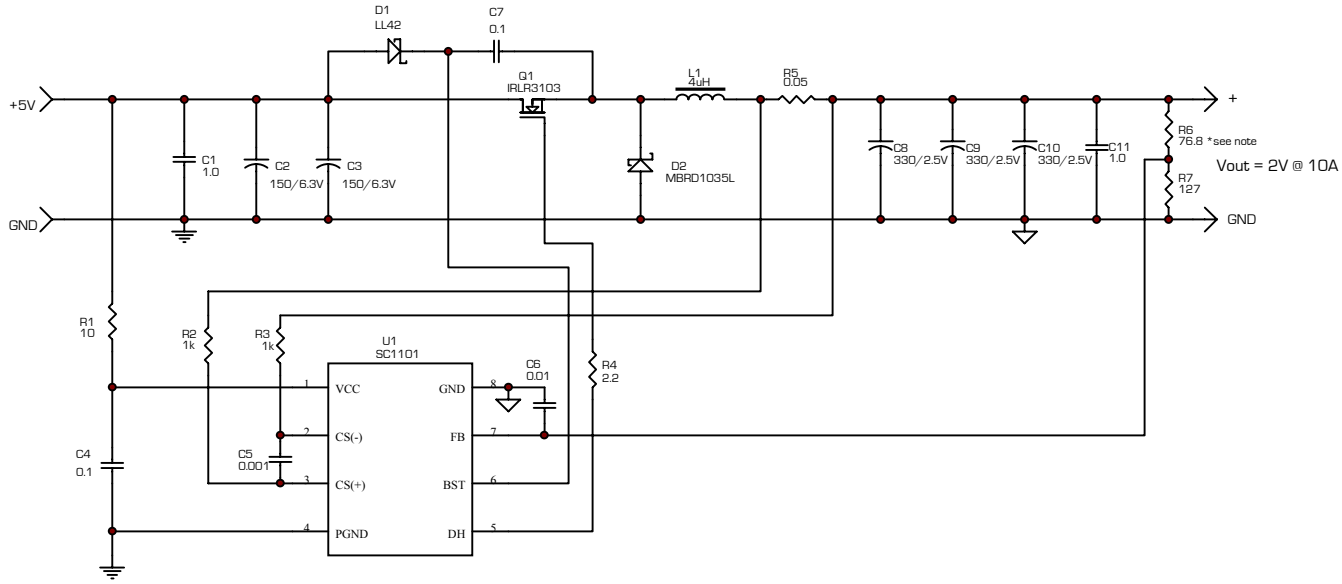
Layout diagram for the SC1101

$V_O = V_{REF} (1 + Ra/Rb)$



Application Circuit

5V to 2.0V @ 10A (Bootstrapped)

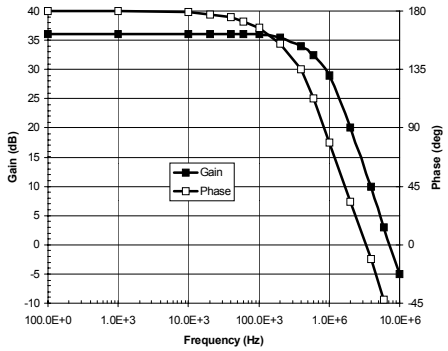


*** NOTE:**

R6 = R7 x (Vout/1.25 - 1) rounded to nearest 1%value

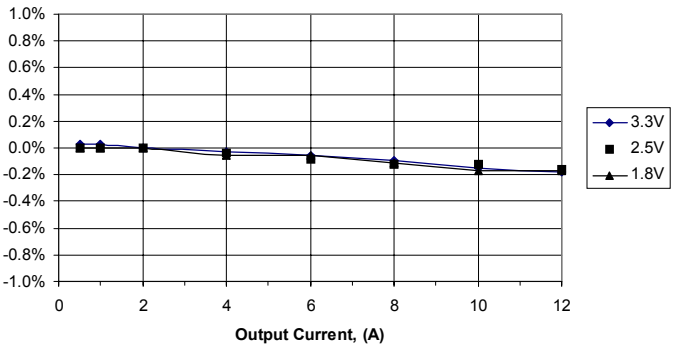
Typical Characteristics

Error Amplifier, Gain and Phase



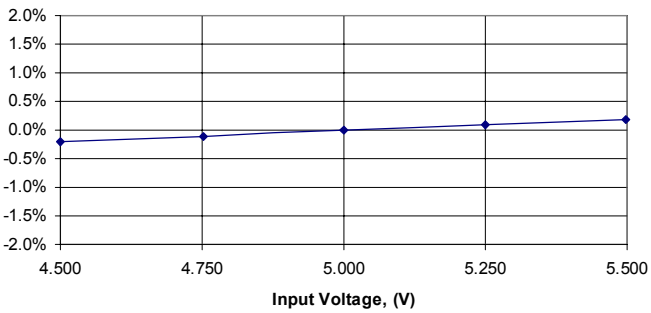
Load Regulation

V_{IN} = 5V



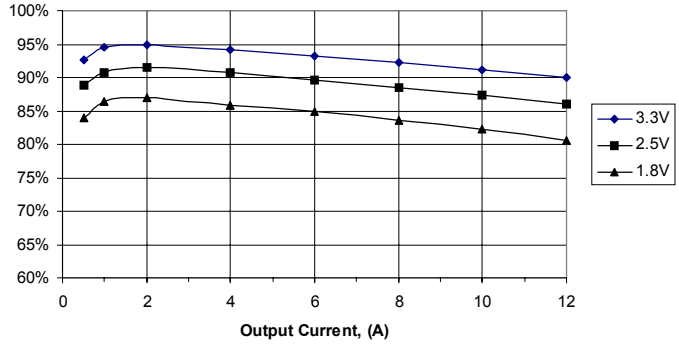
Line Regulation

V_O = 2.5V; I_O = 10A



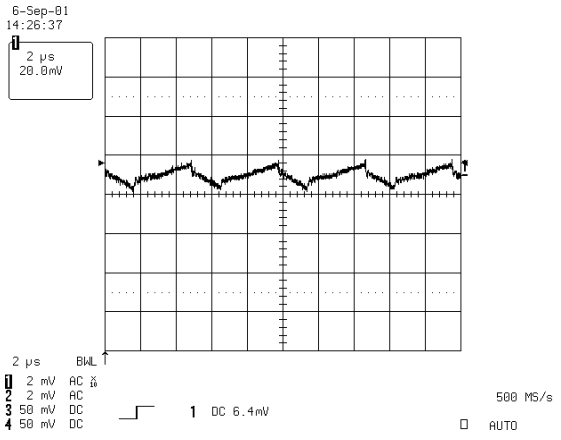
Efficiency

V_{IN} = 5V

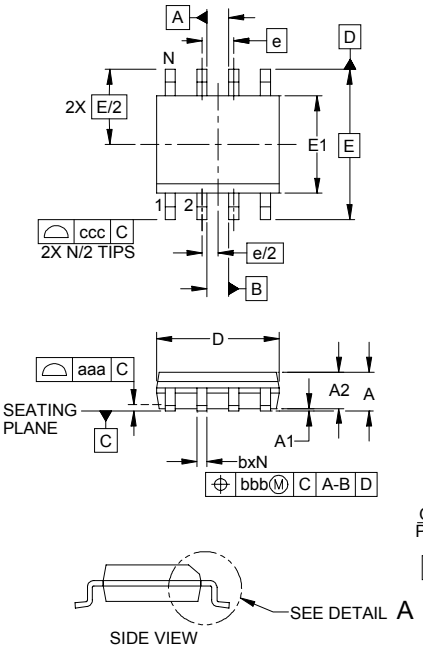


Output Ripple Voltage

V_{IN} = 5V; V_O = 3.3V; I_O = 10A



Outline Drawing - SO-8

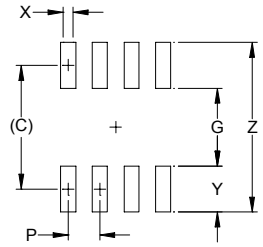


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Minimum Land Pattern - SO-8



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

Contact Information

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