SEMTECH

POWER MANAGEMENT

Dual 30V Step-Down Switching Regulator with 2A Switches

Features

- Wide Input Voltage Range: 2.8V to 30V
- Two Integrated 2A Switches
- Up to 2.5MHz per Channel Programmable Constant Switching Frequency
- Out of Phase Switching Reduces Input Ripple
- Both Switching Regulators share a single Input Filtering Capacitor, Reducing Cost
- External Synchronization
- Cycle-by-Cycle Current-limiting
- Independent Soft-Start/Enable Pins
- Independent Hiccup Overload Protection
- Power Good Indicators Ease Output Sequencing
- Low Shutdown Current
- Thermally Enhanced 16-pin TSSOP Lead Free Package
- Fully WEEE and RoHS Compliant

Applications

- XDSL and Cable Modems
- Point of Load Applications
- Security Cameras

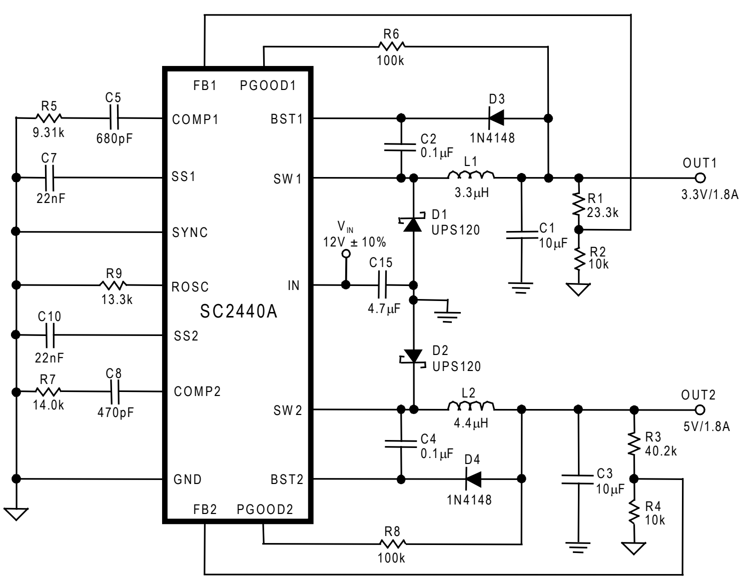
Description

The SC2440A is a constant frequency dual current-mode step-down regulator with integrated 30V switches. It produces two independent outputs from a common input power supply. Channel switching frequency can be programmed up to 2.5MHz. The two regulators switch in opposite phase, reducing input ripple current. As a result, a smaller input filtering capacitor can be used.

Current-mode PWM control simplifies loop compensation. Cycle-by-cycle current limiting and hiccup overload protection reduce power dissipation during overload. The SC2440A is output short-circuit robust.

Separate soft-start/enable pins allow independent control of each channel. Output power good indicators ease output sequencing. The SC2440A can be synchronized to an external clock. This eases noise filtering by eliminating beat frequencies and confining switching noise to a narrow band.

Typical Application Circuit



L1: Sumida CR43
L2: Falco D04012

C1, C3: Murata GRM21BR60J106K
C15: Murata GRM21BR61E475K

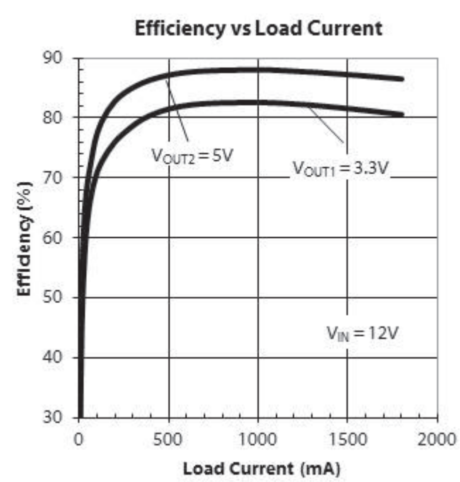
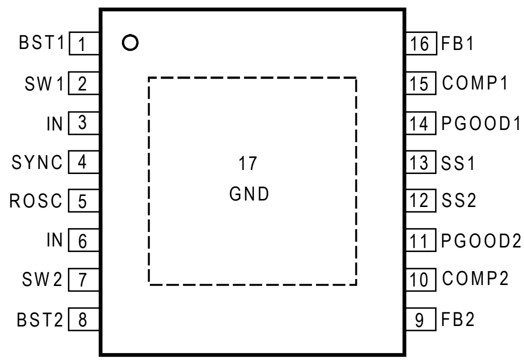


Figure 1. 1.3MHz 12V to 5V and 3.3V Step-down Converter

Pin Configuration

Top View



θ_{JA} = 40°C/W
16 Pin TSSOP-EDP

Ordering Information

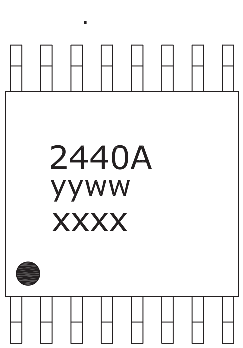
Device	Package
SC2440ATETRT(1) (2)	TSSOP-16 EDP
SC2440AEVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 2,500 devices.

(2) Available in lead-free package only. Device is WEEE and RoHS compliant.

Marking Information



yyww - Date Code
xxxxx
xxxxx - Semtech Lot Number

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Absolute Maximum Ratings

IN .... -0.3V to 32V

SW1/2 .... -0.6V to V_{IN}

BST1/2 .... -0.3V to 42V

BST1/2 Voltage Above SW1/2 .... -4V to 36V

SS1/2, COMP1/2, ROSC .... -0.3V to 3V

SYNC .... -0.3V to 6V

SYNC Pin Current .... -1mA to 5mA

FB1/2 .... -0.3V to 7V

PGOOD1/2 .... -0.3V to V_{IN}

ESD Protection Level[1] 2.5kV

Recommended Operating Conditions

Junction Temperature Range .... -40°C to +105°C

V_{IN} .... 2.8V to 30V

Thermal Information

Thermal Resistance, Junction to Ambient[2] .... 45°C/W

Maximum Junction Temperature .... +150 °C

Storage Temperature Range .... -65°C to +150°C

Peak IR Reflow Temperature (10s to 30s) .... +260°C

Exceeding the above specifications may result in permanent damage to the device or the device may malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless otherwise noted: V_{IN} = 5V, $V_{BST1/2}$ = 8V, V_{SYNC} = 0, ROSC = 12.1kΩ, T_J = -40°C to 105°C. Typical values are at T_J = 25°C.

Parameter	Conditions	Min	Typ	Max	Units
Input Supply					
Maximum Operating V_{IN}				30	V
V_{IN} Start Voltage	V_{IN} Rising	2.6	2.7	2.8	V
V_{IN} Start Hysteresis			90		mV
Shutdown Supply Current	V_{SS1} = V_{SS2} = 0, PGOOD1,2 Open		27	40	µA
Quiescent Supply Current	Not Switching, PGOOD1,2 Open		4.1	5.5	mA
Control Loops					
Feedback Voltage		0.980	1.000	1.020	V
Feedback Voltage Line Regulation	V_{IN} = 3V to 30V		0.006		%/V
FB Pin Input Bias Current			-100	-200	nA
Error Amplifier Transconductance			280		$\mu\Omega^{-1}$
Error Amplifier Open-loop Gain			53		dB
COMP Sourcing Current	V_{FB} = 0.8V, V_{COMP} = 1.2V		16		µA
COMP Sinking Current	V_{FB} = 1.2V, V_{COMP} = 1.2V		18		µA
COMP Maximum Voltage	V_{FB} = 0.9V		1.7		V
COMP to Switch Current Gain			7.5		A/V
COMP Switching Threshold		0.7	1.0	1.3	V

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Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Oscillator and Synchronization					
Channel Free-running Frequency		1.2	1.4	1.6	MHz
Minimum Switch Off-time			90	140	ns
SYNC Input High Voltage		2			V
SYNC Input Low Voltage				0.8	V
SYNC Pin Input Current	$V_{SYNC} = 2V$		60	75	µA
Power Switch					
Switch Current Limit[1]		2.0	2.6	3.8	A
Switch Saturation Voltage	$I_{SW1} = -2A$		300	460	mV
Switch Leakage Current				10	µA
Switch Minimum Bootstrap Voltage	$I_{SW1} = -2A$		1.8	2.4	V
BST Pin Current	$I_{SW1} = -0.5A$		20	30	mA
	$I_{SW1} = -2A$		50	80	mA
Soft-start and Hiccup Overload Protection					
Shutdown SS Threshold	$V_{SS1} = V_{SS2}$	0.15	0.25	0.35	V
Soft-start Charging Current	$V_{SS} = 0$		1.8		µA
	V_{SS} Rising and $V_{SS} = 1.5V$	1.0	1.8	2.6	µA
Soft-start Discharging Current	In Overload Shutdown, V_{SS} Falling and $V_{SS} = 1.5V$		0.8		µA
SS Switching Threshold	$V_{FB} = 0$, $V_{COMP} = 1.3V$, V_{SS} Rising		1.21		V
Hiccup Arming SS Voltage	V_{SS} Rising		2.1		V
Hiccup Retry SS Voltage	V_{SS} Falling	0.7	1.0	1.3	V
FB Overload Threshold	$V_{SS} = 2.3V$, V_{FB} Falling		0.72		V
Output Power Good Indicators					
PGOOD Threshold Below FB	V_{FB} Rising	80	100	120	mV
PGOOD Output Low Voltage	$V_{FB} = 0.8V$, $I_{PGOOD} = 250µA$		0.2	0.4	V
PGOOD Pin Leakage Current	$V_{PGOOD} = 5V$		0.1	1	µA
Thermal Protection					
Thermal Shutdown Temperature	T_J Rising		160		°C
Thermal Shutdown Hysteresis			18		°C

Notes:
(1) Switch current limits do not vary with duty cycle.

Pin Descriptions

Pin #	Pin Name	Pin Function
1, 8	BST1, BST2	Supply pins to the power transistor drivers. Tie to external diode-capacitor bootstrap circuits to generate drive voltages higher than V_{IN} in order to fully enhance the internal power switches.
2, 7	SW1, SW2	Emitters of the internal power NPN transistors. Each SW pin is connected to the corresponding inductor, freewheeling diode and bootstrap capacitor.
3, 6	IN	Power transistor collectors and the power supply to the internal control circuitry. Pins 3 and 6 are internally connected. These pins are to be tied to the same power supply and must be closely bypassed.
4	SYNC	Driving the SYNC pin with a TTL-compatible clock synchronizes the SC2440A. If the SC2440A is to be synchronized to a channel frequency f_{SYNC}, then program the channel free-running frequency to approximately f_{SYNC} using the ROSC resistor. The applied clock frequency can be f_{SYNC} or $2f_{SYNC}$. See Applications Information for details. Tie this pin to ground if not used.
5	ROSC	An external resistor from this pin to ground sets the channel free-running frequency.
9, 16	FB2, FB1	Inverting inputs of the error amplifiers. Each FB pin is tied to a resistor divider between the corresponding output and ground. The resistor divider sets the channel output voltage.
10, 15	COMP2, COMP1	Outputs of the error amplifiers. The voltages at these pins control the peak switch currents. RC networks at these pins compensate the control loops. Pulling either pin below 0.8V stops the corresponding regulator.
11, 14	PGOOD2, PGOOD1	Open-collector outputs of power good comparators. Tie to external pull-up resistors from the input or the output of the converter. The PGOOD outputs become valid as soon as V_{IN} rises above 0.9V during power-up. The PGOOD pin is actively pulled low until the corresponding FB pin rises to within 10% of the final regulation voltage.
12, 13	SS2, SS1	A capacitor from either SS pin to ground sets the soft-start interval and provides an overload hiccup function for that channel. Pulling either SS pin below 0.8V with an open-collector or an open-drain transistor shuts off the corresponding regulator. To completely shut off the SC2440A to low current state, pull both SS pins below 0.15V.
17 (Exposed Pad)	GND	The exposed pad at the bottom of the package is the analog ground of the SC2440A. It also serves as a thermal contact to the circuit board. It is to be connected to the ground plane of the PC board using multiple vias.

Block Diagram

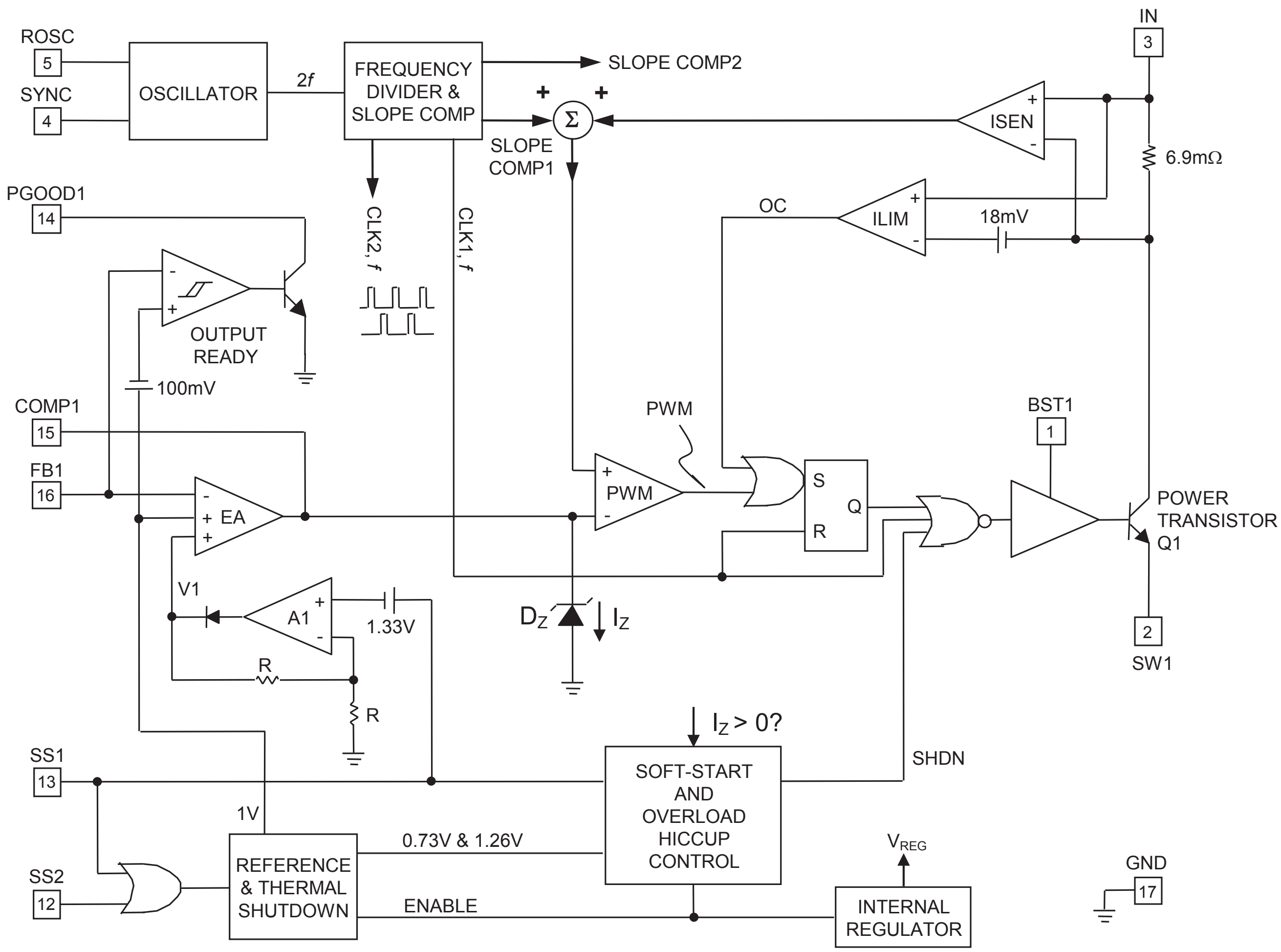

Figure 2. SC2440A Block Diagram (Channel 1 Shown)

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Block Diagram

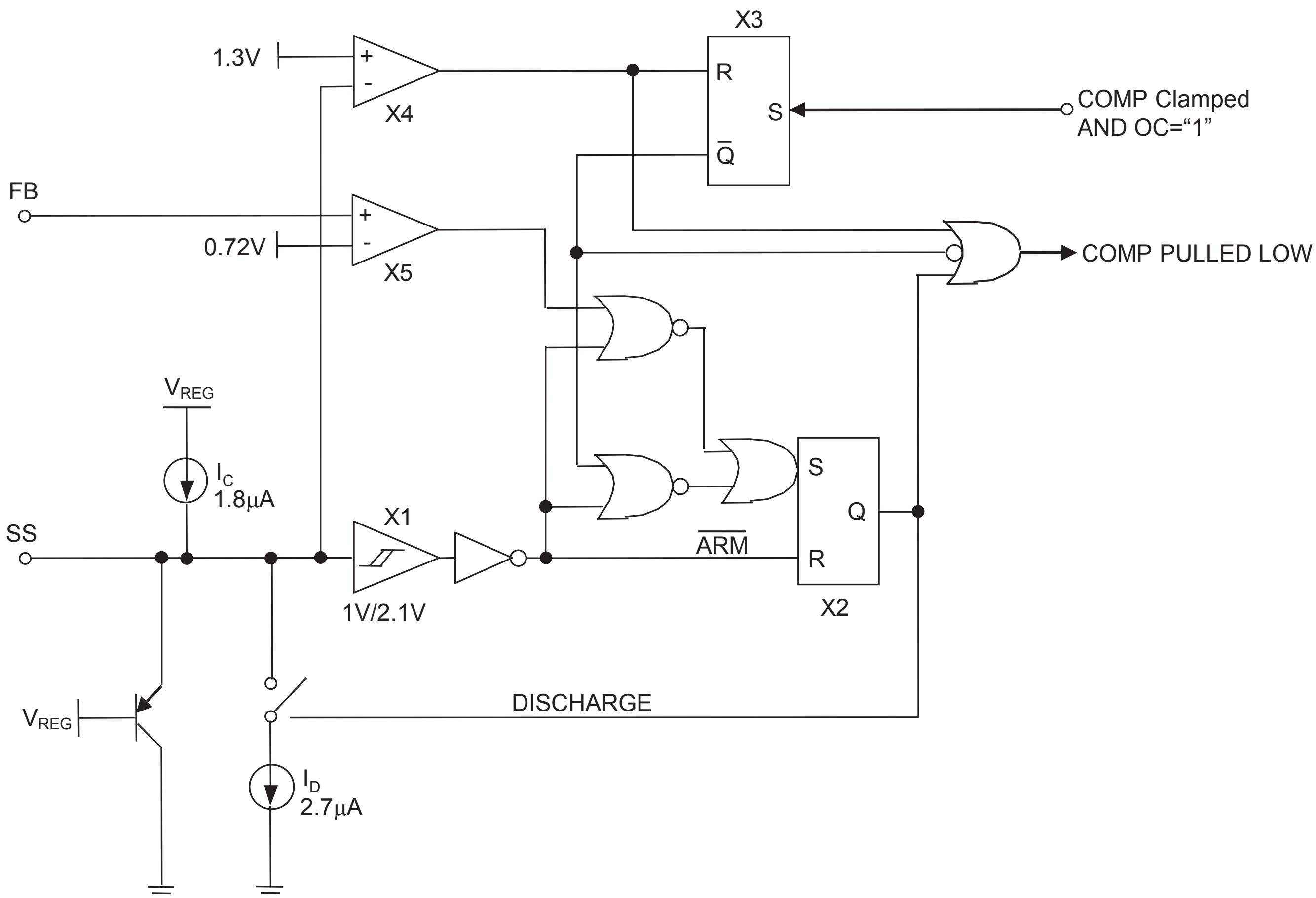

Figure 3. Details of the Soft-start and Overload Hiccup Control Circuit

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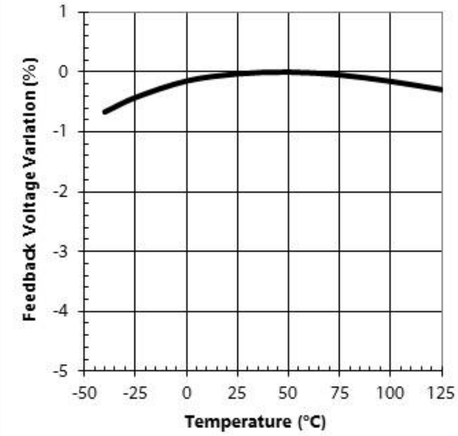
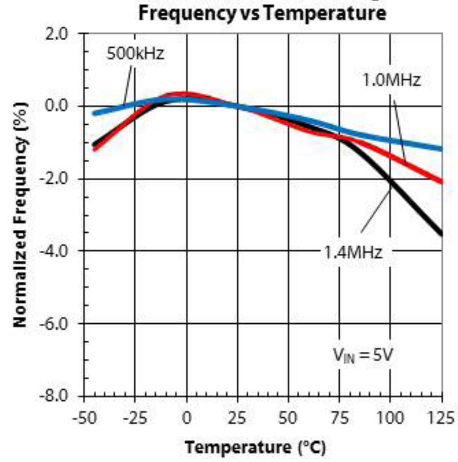
Typical Characteristics

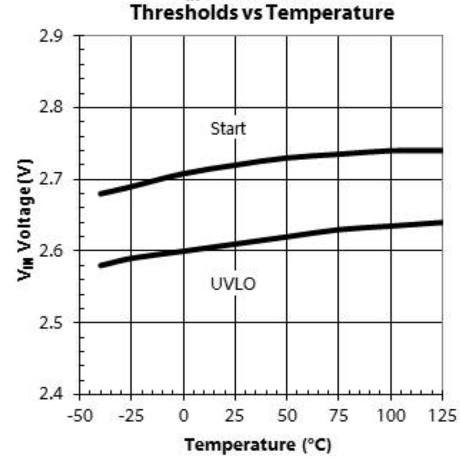
Normalized Feedback Voltage vs Temperature



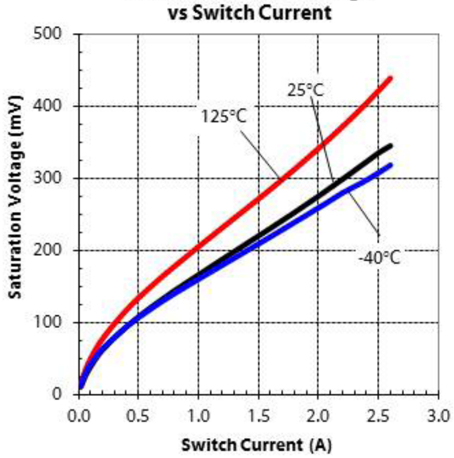
Normalized Free-Running Frequency vs Temperature



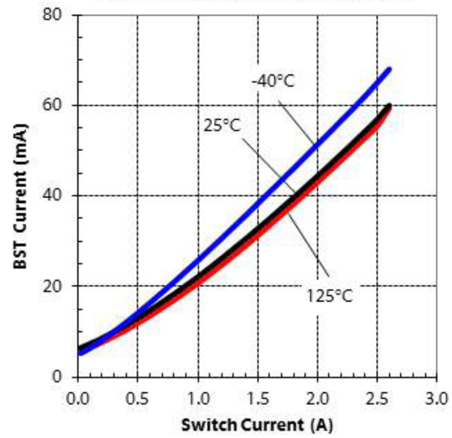
V_{IN} Start and UVLO Thresholds vs Temperature



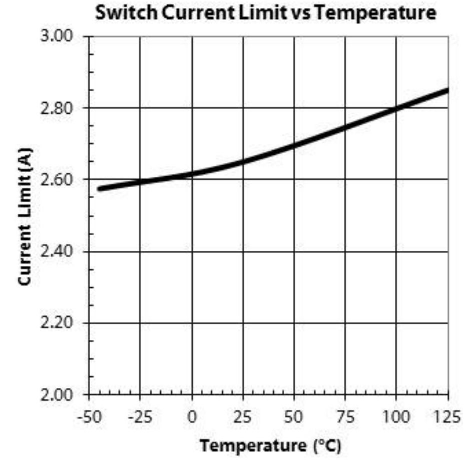
Switch Saturation Voltage vs Switch Current



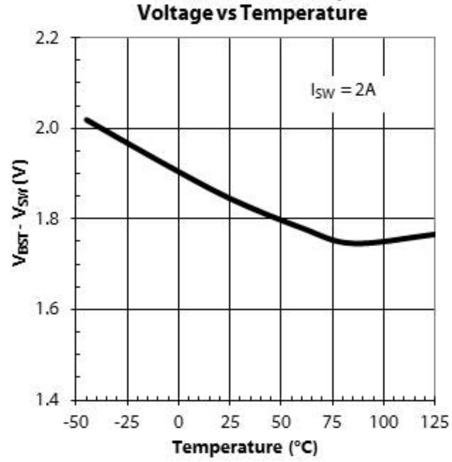
BST Pin Current vs Switch Current



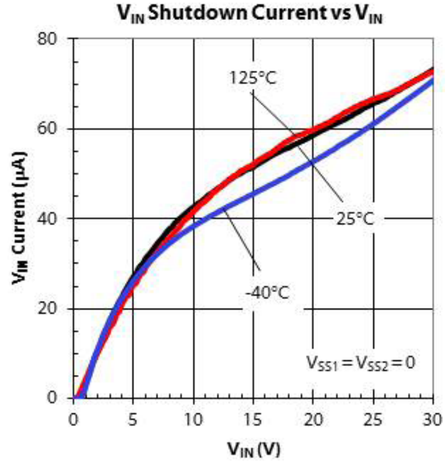
Switch Current Limit vs Temperature



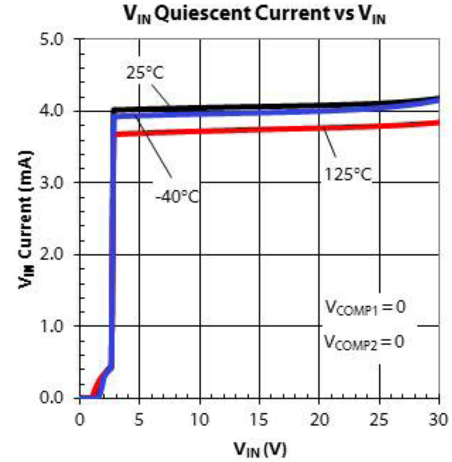
Minimum Bootstrap Voltage vs Temperature



V_{IN} Shutdown Current vs V_{IN}

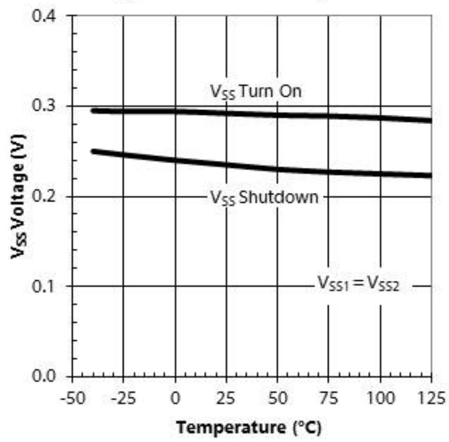


V_{IN} Quiescent Current vs V_{IN}

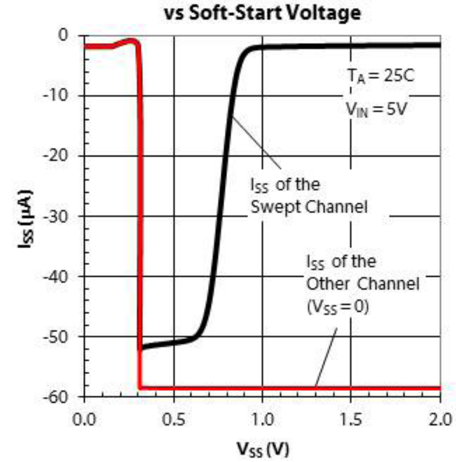


Typical Characteristics (Continued)

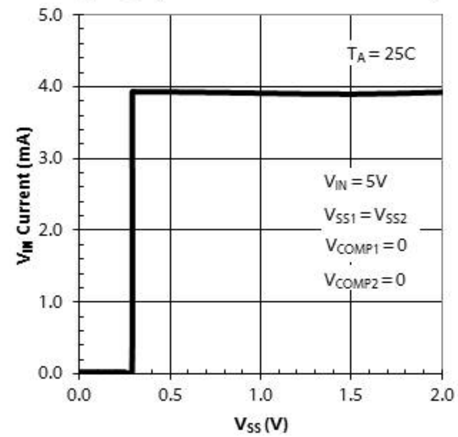
V_{SS} Thresholds vs Temperature



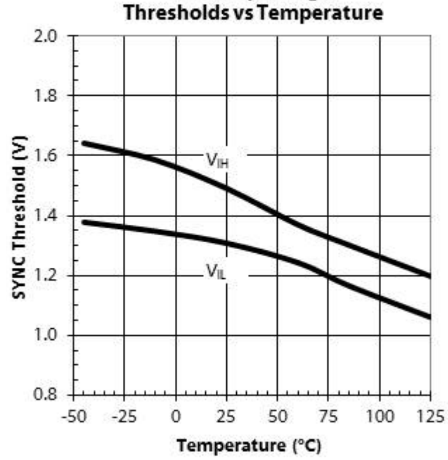
Soft-Start Pin Current vs Soft-Start Voltage



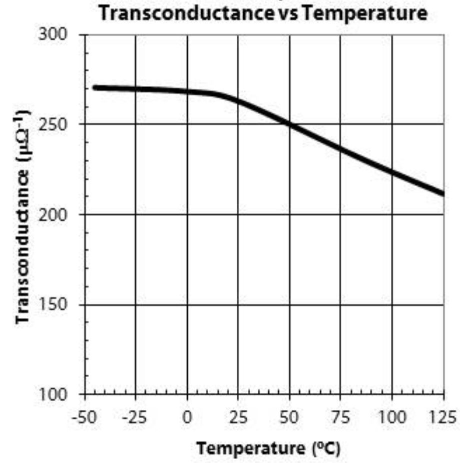
V_{IN} Supply Current vs Soft-Start Voltage



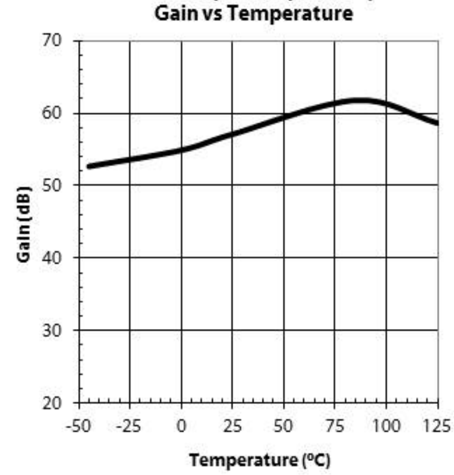
SYNC Input Logic Thresholds vs Temperature



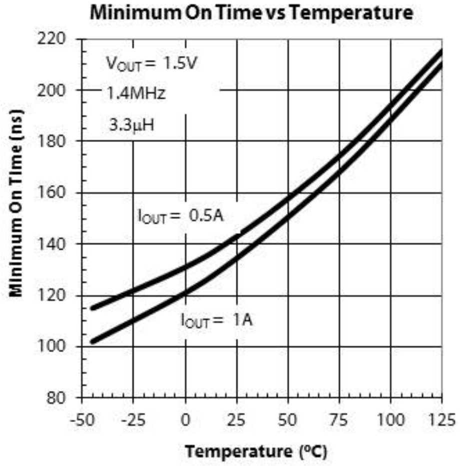
Error Amplifier Transconductance vs Temperature



Error Amplifier Open-Loop Gain vs Temperature



Minimum On Time vs Temperature



General Description

The SC2440A is a dual constant frequency peak current-mode step-down switching regulator with integrated 2A high-side transistors. Both regulators share the same voltage reference, oscillator and synchronizing circuit. Turn-on of the power transistors is phase-shifted by 180° for input ripple reduction. The two regulators are otherwise identical, independent and are capable of producing two independent outputs from a common power supply.

The free-running frequency of the master oscillator is programmed with an external resistor from the ROSC pin to ground, giving the user the flexibility of setting the switching frequency according to the input to output voltage conversion ratio. The master clock is fed into a frequency divider for phase clocks generation. As a result, each regulator runs at half the master clock rate (Figure 2). The SC2440A can also be synchronized to an external clock.

The SC2440A uses peak current-mode control. The inner current loop of current-mode control reduces the double reactive poles of the output LC filter to a single real pole, easing loop compensation. A simple Type-2 compensation network ensures stability with fast transient response.

The switch collector current of each channel is sensed with an integrated sense resistor. The sensed current is summed with a slope-compensating ramp before it is compared with the error amplifier output. The PWM comparator trip point determines the switch turn-on pulse width (Figure 2). ILIM is a cycle-by-cycle current-limit comparator that turns off the power switch whenever the sensed-signal exceeds 18mV.

Driving the base of the power transistor above the input power supply rail minimizes the power transistor turn-on voltage and maximizes efficiency. An external bootstrap circuit (formed by the capacitor C_2 and the diode D_3 in Figure 1) generates a voltage higher than V_{IN} at the BST1 pin. The bootstrapped voltage generated becomes the supply voltage for the power transistor driver.

The SS pin is a multiple-function pin. An external capacitor connected from the SS pin to ground together with the internal charging and discharging circuits set the soft-start and overload shutoff times for the regulator (Figure 3). The SS pin can also be used to shut off the corresponding regulator. When either SS pin is pulled below 0.8V, the corresponding regulator is turned off. If both SS pins are pulled below 0.15V, then the SC2440A will undergo overall shutdown, drawing less than 40µA from a 5V input. When either SS pin is released, the corresponding soft-start capacitor is charged with a 1.8µA current source (not shown in Figure 3). When either SS voltage exceeds 0.35V, the internal regulator in the SC2440A turns on. V_{IN} quiescent current increases to 4.1mA. An internal fast charge circuit (not shown) quickly charges the soft-start capacitor to 1V. At this juncture, the fast charge circuit turns off and the 1.8µA current source slowly charges the soft-start capacitor.

The error amplifier EA in Figure 2 has two non-inverting inputs. The non-inverting input with the lower voltage predominates. One of the non-inverting inputs is biased to a precision 1V reference and the other non-inverting input is tied to the output of the amplifier A_1. Amplifier A_1 produces an output $V_1 = 2(V_{SS} – 1.33)$ if $V_{SS} > 1.33V$. For $V_{SS} < 1.33V$, $V_1 = 0$. During start up, COMP is pulled low initially. When V_{SS} exceeds 1.21V, COMP is released. However the effective non-inverting input of EA remains zero. As a result, the regulator output stays at zero as the soft-start capacitor is charged from 1.21V to 1.33V. The regulator output starts to ramp when V_{SS} exceeds 1.33V and V_{COMP} rises above 1.1V. If the soft-start interval is made sufficiently long, then the FB voltage (hence the output voltage) will track V_1 during start up. V_{SS} must be at least 1.88V to ensure regulation. Zener diode D_Z clamps COMP to a voltage higher than that corresponding to the cycle-by-cycle switch current limit. Current flow in D_Z indicates clamping of COMP.

As the load draws more current from the regulator, the current-limit comparator ILIM (Figure 2) limits the switch current on a cycle-by-cycle basis. If the over-current condition persists, then the COMP voltage will continuously increase to its clamp level, eventually setting the overload shutdown latch X_3. The COMP pin is immediately pulled low, turning off the corresponding regulator (Figure 3). Overload shutdown can occur during soft-start. However the SS capacitor is always charged to the upper trip voltage of the Schmitt trigger X_1 before it can be discharged. The reset input of the discharge latch X_2 stays high before the soft-start capacitor is charged to 2.1V. Once the soft-start capacitor is charged above 2.1V, X_1 output goes high and the reset input of the SS discharge latch X_2 goes low,

General Description (Continued)

enabling SS discharge. The net soft-start capacitor discharging current is $I_D - I_C \approx 1.2\mu A$. The switching regulator remains off until the soft-start capacitor is discharged below 1V. At this moment, the SS discharge latch is reset. The soft-start capacitor is recharged and the converter again undergoes soft-start, delaying converter restart until the hiccup cycle completes, reducing power dissipation in overload. The regulator will go through soft-start, overload shutdown and restart until it is no longer overloaded. Comparator X_4 resets latch X_3 during initial start-up or before recovering from overload shutdown. Comparator X_5 monitors the output voltage after hiccup is armed. If excessive overload causes the converter output voltage to fall below 72% of its set point, then the converter will be shut off immediately, without waiting for V_{COMP} to rise to its clamp level. The converter restarts after timing out.

The output power good comparator indicates that the channel output voltage has risen to within 10% of its set value. Each regulator of the SC2440A has its own output good comparator. The open collector output of the voltage ready comparator will be actively pulled low if the corresponding feedback voltage is below 0.9V.

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Applications Information

Setting the Output Voltage

The regulator output voltage is set with an external resistor divider (Figure 4) with its center tap tied to the FB pin.

$$R_1 = R_2 \cdot (V_{OUT} - 1) \qquad (1)$$

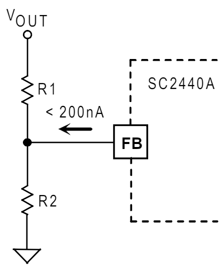

Figure 4. R_1 and R_2 Set the Output Voltage

The percentage error due the input bias current of the error amplifier is

$$\frac{\Delta V_{OUT}}{V_{OUT}} < \frac{-200nA \cdot 100 \cdot (R_1 || R_2)}{1V}$$

Using a smaller R_2 (preferably < 20kΩ) makes the effect of the amplifier input bias current insignificant compared to the V_{OUT} tolerance resulting from the use of 1% resistors.

Setting the Operating Frequency

The master oscillator in the SC2440A feeds a toggle flip-flop which in turn generates the individual channel clocks CLK1 and CLK2 (Figure 2). The phase clocks run at half the master oscillator frequency and are shifted in phase by 180°. The external resistor from the ROSC pin to ground programs the channel free-running frequency $f_{FREE-RUN}$. Table 1 lists the suggested programming resistors for various channel frequencies.

Before choosing the operating frequency, tradeoffs among efficiency, operating duty cycle, component size and EMI must be considered. High frequency operation reduces the size of passive components but switching losses are higher. Lowering the switching frequency improves efficiency, however the required inductor and capacitor are larger. It is also worth noting that a dual DC-DC converter with each channel switching at 1MHz will produce a switching noise spectrum at integer multiples of the 1MHz fundamental.

Switching frequency is also limited by the minimum controllable on time when stepping down from high V_{IN} to low V_{OUT}. This will be described in next section.

Table 1. Programming the Channel Frequency

Channel $f_{FREE-RUN}$ (kHz)	ROSC Resistor (kΩ)
200	118
300	78.7
400	57.6
500	45.3
600	35.7
700	30.9
800	24.9
900	22.1
1000	19.6
1100	17.4
1200	15.4
1300	13.3
1400	12.1
1500	11.0
1600	10.0
1700	9.09
1800	8.25
1900	7.50
2000	6.65
2100	6.19
2200	5.62
2300	4.99
2400	4.53
2500	4.02

Minimum On Time Considerations

The switching duty cycle of a DC-DC converter is the ratio of the switch on time to the switching period. For a non-synchronous step-down regulator, the duty cycle D in continuous-conduction mode (CCM) is given by:

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Applications Information (Continued)

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{CESAT}} \quad (2)$$

where V_{CESAT} is the switch saturation voltage and V_D is voltage drop across the freewheeling diode.

For a given output voltage, the switch on time becomes shorter as V_{IN} increases. In peak current-mode control, the PWM modulating ramp is the sensed current ramp of the power switch. This current ramp is absent unless the switch is turned on. The switch is turned off when this ramp intersects the error amplifier output. The propagation delay time required to immediately turn off the switch after it is turned on is the minimum controllable switch on time [$t_{ON(MIN)}$]. The typical minimum on time is plotted against temperature in "Typical Characteristics". $t_{ON(MIN)}$ increases with temperature and is also load-dependent. The power switch in the SC2440A is either not turned on at all or for at least $t_{ON(MIN)}$. If the required on time (= $\frac{D}{f}$) is shorter than the minimum on time, the regulator will either jitter or skip cycles.

Example: Determine the maximum switching frequency of a dual 12V to 1.2V and 3.3V regulator. The regulator needs to work up to 85°C.

We only need to consider the 1.2V output because this channel is switching at the lower duty cycle. Assuming that V_D = 0.45V, V_{CESAT} = 0.3V and V_{IN} = 13.2V (10% high line), the duty ratio D_1 of the 1.2V can be calculated using equation (2).

$$D_1 = \frac{1.2 + 0.45}{13.2 + 0.45 - 0.3} = 0.124$$

To allow for transient headroom and frequency tolerances, the minimum operating switch on time should be at least 237ns (1.3 times the 0.5A minimum on time at 85°C). The maximum operating frequency of the 12V to 1.2V and 3.3V converter is therefore $\frac{D_1}{237ns} \approx 520kHz$.

Minimum Off Time Limitation

The PWM latch in Figure 2 is reset every period by the clock. The clock also turns off the power transistor to refresh the bootstrap capacitor. This minimum off time limits the attainable duty cycle of the regulator at a given switching frequency. Measurement shows that the power transistor is turned off for at least 140ns every switching period to reset the latch and to refresh the bootstrap capacitor. For a step-down converter, duty cycle increases with increasing $\frac{V_{OUT}}{V_{IN}}$ ratio. If the required duty cycle is higher than the attainable maximum, then the output voltage will not be able to reach its set value regardless of the load.

Example: Determine the maximum operating frequency of a dual 3.3V to 1.8V and 2.5V switching regulator using the SC2440A.

The 2.5V channel is switching at the higher duty cycle. Assuming that V_D = 0.45V, V_{CESAT} = 0.3V and V_{IN} = 2.97V (10% low line), the duty ratio D_2 of the 2.5V converter can be calculated using equation (2).

$$D_2 = \frac{2.5 + 0.45}{2.97 + 0.45 - 0.3} = 0.946$$

The maximum operating frequency of the 1.8V and the 2.5V converter is therefore $\frac{1 - D_2}{140ns} = 380kHz$.

Transient headroom requires that channel frequency be set below 380kHz.

External Synchronization

The SC2440A can be synchronized by feeding an external clock to the SYNC pin. The SYNC input buffer is positive-edge triggered and TTL-compatible (V_{IL} < 0.8V and V_{IH} > 2V). The synchronizing frequency can be either 1X or 2X the desired channel switching frequency.

1X Frequency Synchronization

If the channels are to be synchronized to run at an external clock frequency f_{SYNC}, then set the free-running channel frequency between $0.95f_{SYNC}$ and f_{SYNC} to allow for free-running frequency tolerance. The leading edge of the external clock will lock onto one of the channels and turn on its power transistor. With 1X frequency synchronization, the phase difference between the two channels is not exactly 180°. However, setting the nominal free-running channel frequency near f_{SYNC} will minimize the phase deviation from 180°.

Applications Information (Continued)

2X Frequency Synchronization

An external clock with frequency f_{SYNC} ranging from 1.8X to 2.7X $f_{FREE\text{-}RUN}$ will synchronize the individual channels to $\frac{f_{SYNC}}{2}$ with 180° out of phase switching. The nominal free-running channel frequency should be programmed to between $0.475f_{SYNC}$ and $0.5f_{SYNC}$ when synchronizing using a 2X frequency clock.

Example: Detemine the value of the frequency setting resistor if the SC2440A is to be synchronized to run at 1.03MHz per channel.

The required external clock is a TTL-compatible pulse train running at either 1.03MHz (for 1X frequency synchronization) or 2.06MHz (for 2X frequency synchronization).

Using the guideline given above, set the nominal free-running channel frequency to 1MHz (0.97 × 1.03MHz for 1X frequency synchronization or 0.485 × 2.06MHz for 2X frequency synchronization).

From Table 1, a 19.6kΩ resistor sets the channel free-running frequency to 1MHz.

Inductor Selection and Output Current

The inductor ripple current ΔI_L for a non-synchronous step-down converter in continuous-conduction mode is

$$\Delta I_L = \frac{(V_{OUT} + V_D)(1-D)}{fL} \quad (3)$$

where f is the switching frequency and L is the inductance.

In current-mode control, the slope of the modulating (sensed switch current) ramp should be steep enough to lessen jitter tendency but not so steep that the large flux swing decreases efficiency. An inductor ripple current ΔI_L between 20-30% of the peak inductor current limit is a good compromise. Inductors so chosen are not only small but also have low core losses. Setting $\Delta I_L = 0.25(2.6) = 0.65A$, $V_D = 0.45V$ and $V_{CESAT} = 0.3V$ in (3), the inductance can be calculated as:

$$L = \frac{(V_{OUT} + 0.45)(V_{IN} - V_{OUT} - 0.3)}{(V_{IN} + 0.15)\cdot \Delta I_L \cdot f} \quad (4)$$

where L is in µH and f is in MHz.

Equation (3) shows that for a given V_{OUT}, ΔI_L increases as D decreases. If V_{IN} varies over a wide range, then choose L based on the nominal input voltage. Always verify converter operation at the input voltage extremes.

The channel current limit is at least 2A. The maximum load current of a step-down converter is the switch current limit I_{LIM} minus $\frac{\Delta I_L}{2}$. The maximum channel output current is slightly less than 2A.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} = 2A - \frac{\Delta I_L}{2} \quad (5)$$

The available output current can be made to approach I_{LIM} by using a larger inductor.

The saturation current of the inductor should be 20-30% higher than the peak current limit. Low-cost powder iron cores are not suitable for high-frequency switching power supplies due to their high core losses. Inductors with ferrite cores are recommended.

Interleaved Switching and Input Capacitor

A step-down converter draws a pulsed current with peak-to-peak amplitude equal to its output current I_{OUT} from the input power supply. An input capacitor placed between the supply and the buck converter filters the AC current and keeps the current drawn from the supply constant. The input capacitance C_{IN} should be high enough to filter the pulsed input current. Its equivalent series resistance (ESR) should be low so that power dissipated in the capacitor does not result in significant temperature rise and degrade reliability.

For a single channel step-down converter, the RMS ripple current in the input capacitor is

$$I_{RMS_{(CIN)}} = I_{OUT}\sqrt{D(1-D)} \quad (6)$$

Power dissipated in the input capacitor is $I^2_{RMS_{(CIN)}}(ESR)$.

Applications Information (Continued)

Equation (6) has a maximum of $\frac{I_{OUT}}{2}$ when $D = \frac{1}{2}$, corresponding to the worst-case power dissipation of $\frac{I_{OUT}^2 \cdot ESR}{4}$ in C_{IN}. For example, if one power transistor in the SC2440A is switching from zero to 2A and operating at 50% duty cycle while the other channel is disabled, then the input capacitor will carry 1A of RMS ripple current. If both power transistors in the SC2440A were to switch on in phase, the current drawn by the SC2440A would consist of current pulses with amplitude equal to the sum of the channel switch currents. If both channels were delivering full load to their outputs and operating at 50% duty cycle, then the input current would switch from zero to 4A. The RMS ripple current in the input capacitor would then be 2A. Power dissipated in C_{IN} would be $(2A)^2(ESR)$, four times the maximum due to one channel alone. The SC2440A produces the highest RMS ripple current in C_{IN} when only one channel is switching at current limit (< 3.4A). The input capacitor therefore should have a RMS ripple current rating of at least 1.7A.

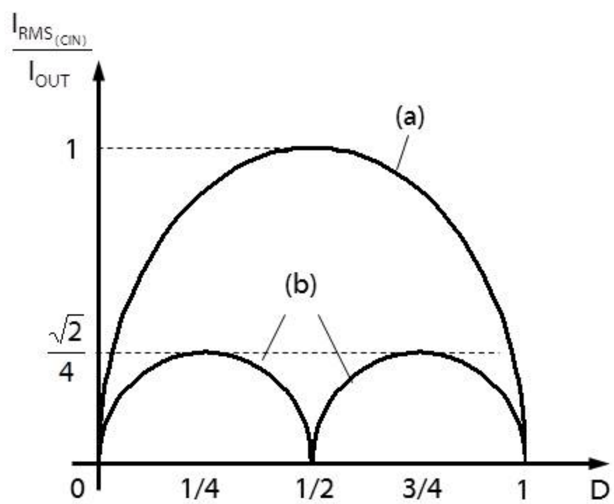


Figure 5. Normalized C_{IN} RMS Ripple Current as a Function of the Duty Cycle D for the Following Regulators:

(a) Two step-down converters switching in phase and at the same duty cycle. Each regulator delivers I_{OUT} to its corresponding output for a total output current of $2I_{OUT}$.

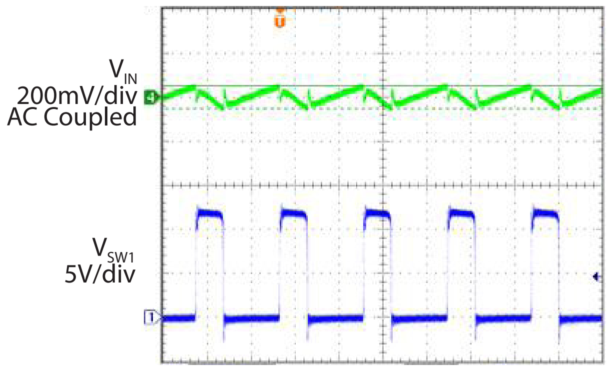
(b) A 180° out of phase switching dual step-down regulator. The output currents and the duty cycles of the individual regulators are identical. Each regulator delivers I_{OUT} to its corresponding output for a total output current of $2I_{OUT}$.

Figure 5 compares the RMS ripple currents produced in the input capacitor by (a) two identical step-down converters switching in phase and (b) a dual step-down converter with 180° out of phase switching (as implemented in the SC2440A) as a function of the switching duty cycle D. For simplicity, each individual converter in both cases is assumed to operate at the same duty cycle and deliver the same output current I_{OUT} for a total output current of $2I_{OUT}$. Case (a) produces a maximum C_{IN} RMS ripple current of I_{OUT} when D = 0.5. Whereas the corresponding ripple current is reduced to $\frac{\sqrt{2}}{4} I_{OUT}$ in Case (b). At 50% duty cycle, 180° out of phase switching nulls C_{IN} ripple current. Figure 5(b) also shows that slight deviation from 180° phase shift has no major impact on input ripple reduction. **Interleaved switching therefore generates lower input voltage noise and requires a smaller input ceramic capacitor for filtering.** This saves cost for V_{IN} > 25V as high voltage ceramic capacitors are not cheap. Predicting the input capacitor RMS ripple current of a dual step-down converter operating at different duty cycles and delivering different output currents is not easy. However, the aforementioned advantages of interleaved switching are still valid.

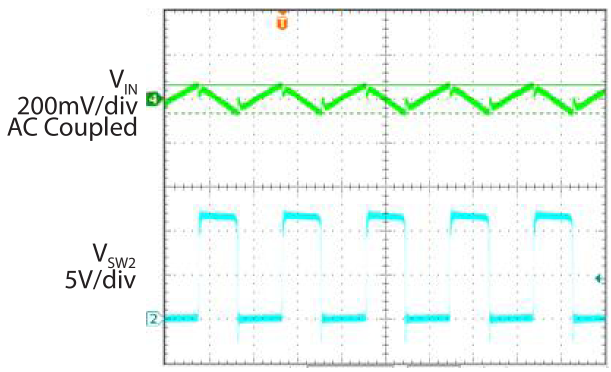
Figure 6 compares the input voltage ripple generated by the DC-DC converter in Figure 1 with either channel or both channels switching. The low-noise advantage of interleaved switching is clearly evident.

Multi-layer ceramic capacitors, which have very low ESR (a few mΩ) and can easily handle high RMS ripple current are the ideal choice for input filtering. A single 4.7μF or 10μF X5R ceramic capacitor is adequate. For high voltage applications, a small ceramic (1μF or 2.2μF) can be placed in parallel with a low ESR electrolytic capacitor to satisfy both the ESR and bulk capacitance requirements.

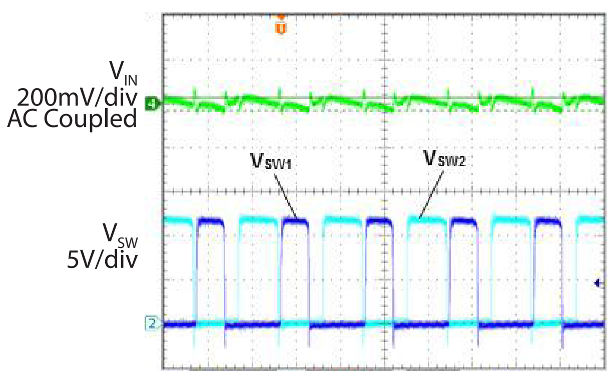
Applications Information (Continued)



400ns/div
(a)



400ns/div
(b)



400ns/div
(c)

Figure 6. Input Voltage Ripple Generated by the DC-DC Converter in Figure 1.

(a) Channel 1 is delivering 1.8A with Channel 2 shut off. The input ripple voltage ≈105mV.

(b) Channel 2 is delivering 1.8A with Channel 1 shut off. The input ripple voltage ≈ 130mV.

(c) Both Channels are supplying 1.8A to the loads. Interleaved switching reduces the input ripple voltage to about 60mV.

Output Capacitor

The output ripple voltage ΔV_{OUT} of a buck converter can be expressed as

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right) \quad (7)$$

where C_{OUT} is the output capacitance.

Inductor ripple current ΔI_L increases as D decreases [Equation (3)]. The output ripple voltage is therefore the highest when V_{IN} is at its maximum. The first term in (7) results from the ESR of the output capacitor while the second term is due to the charging and discharging of C_{OUT} by the inductor ripple current. Substituting ΔI_L = 0.65A, f = 550kHz and C_{OUT} = 22µF ceramic with ESR = 3mΩ in (7),

$$\Delta V_{OUT} = 0.65A \cdot (3m\Omega + 10.3m\Omega)$$
$$= 1.95mV + 6.70mV = 8.65mV$$

Depending upon operating frequency and the type of capacitor, ripple voltage resulting from the charging and discharging of C_{OUT} may be higher than that due to the ESR of the output capacitor. A 10µF to 47µF X5R ceramic capacitor is found adequate for output filtering in most applications. Ripple current in the output capacitor is not a concern because the inductor current of a buck converter directly feeds C_{OUT}, resulting in very low ripple current. Avoid using Z5U and Y5V ceramic capacitors for output filtering because these types of capacitors have high temperature and voltage coefficients.

Freewheeling Diode

Use of Schottky barrier diodes as freewheeling rectifiers reduces diode reverse recovery current spikes, easing high-side current sensing in the SC2440A. These diodes should have an average current rating between 1A and 2A. The reverse blocking voltage of the Schottky diode should be derated by 10%-20% for reliability. The Schottky diode used in a 12V input step-down converter should have a reverse voltage rating of at least 16V (20% derating). For switching regulators operating at low duty cycles (i.e. low output voltage to input voltage conversion ratios), it is beneficial to use freewheeling diodes with somewhat higher average current ratings (thus lower forward voltages). This is because the diode conduction in-

Applications Information (Continued)

terval is much longer than that of the transistor. Converter efficiency will be improved if the voltage drop across the diode is lower.

The freewheeling diodes should be placed close to the SW pins of the SC2440A to minimize ringing due to trace inductance.

Bootstrapping the Power Transistors

To maximize efficiency, the turn-on voltage across the internal power NPN transistors should be minimized. If these transistors are to be driven into saturation, then their bases will have to be driven from a power supply higher in voltage than V_{IN}. The required driver supply voltage (at least 2.4V higher than the SW voltage) is generated with a bootstrap circuit (the diode D_{BST} and the capacitor C_{BST} in Figure 7). The bootstrapped output (the common node between D_{BST} and C_{BST}) is connected to the BST pin of the SC2440A.

The minimum BST to SW voltage required to fully saturate the power transistor is shown in the "Typical Characteristics" (pages 8-9). The minimum required V_{CBST} increases as temperature decreases. The bootstrap circuit reaches equilibrium when the base charge drawn from C_{BST} during transistor on time is equal to the charge replenished during the off interval.

Figure 7 summarizes various ways of bootstrapping the SC2440A. A fast switching PN diode (such as 1N4148 or 1N914) and a small (0.1μF – 0.47μF) ceramic capacitor can be used.

In Figure 7(a) the power switch is bootstrapped from the output. This is the most efficient configuration and it also results in the least voltage stress at the BST pin. The maximum BST pin voltage is about $V_{IN} + V_{OUT}$. The minimum V_{OUT} required for this bootstrap configuration is 2.5V. If the output voltage is 2.5V, then D_{BST} will preferably be a small Schottky diode (such as BAT54) to maximize the bootstrap voltage. A 0.33-0.47μF bootstrap capacitor may also be needed to reduce droop. Bench measurement shows

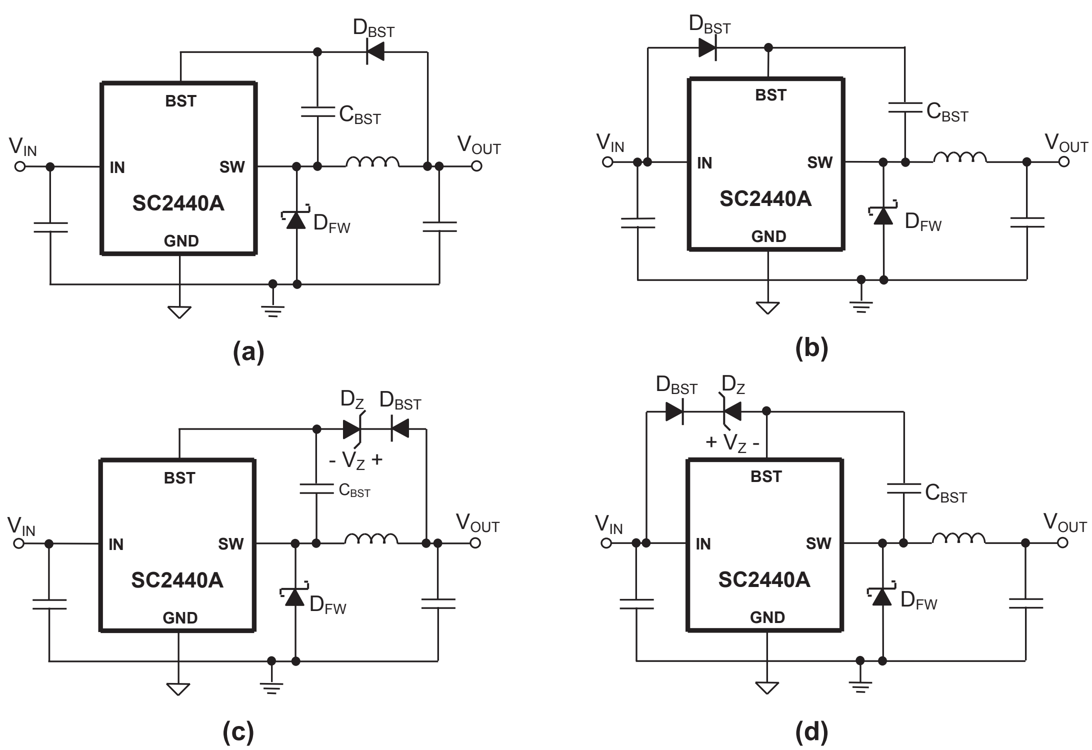


Figure 7(a)-(d). Bootstrap Configurations for the SC2440A

Applications Information (Continued)

that using a Schottky bootstrapping diode when V_{OUT} > 2.5V produces no noticeable efficiency benefit.

If $V_{IN(MAX)} + V_{OUT} > 42V$, then a Zener diode D_Z can be used in series with D_{BST} to lower the BST voltage [Figure 7(c)]. The following inequality gives a suitable range for the Zener diode voltage V_Z:

$$V_{OUT} - 3 > V_Z > V_{IN(MAX)} + V_{OUT} - 42 \qquad (8)$$

The SC2440A can also be bootstrapped from the input [Figure 7(b)]. This configuration is not as efficient as Figure 7(a). However this may be the only option if the output voltage is less than 2.5V and there is no other available supply with voltage higher than 2.5V. Voltage stress at the BST pin can be somewhat higher than $2V_{IN}$. The BST pin voltage should not exceed its absolute maximum rating of 42V. To reduce BST voltage stress when stepping down from high V_{IN} (>20V) to low V_{OUT} (<2.5V), a Zener diode can be added in series with D_{BST}. This is shown in Figure 7(d). The Zener voltage can be selected using (9):

$$V_{IN(MIN)} - 3 > V_Z > 2V_{IN(MAX)} - 42 \qquad (9)$$

Figures 7(e) and (f) show how to bootstrap the SC2440A from a second independent power supply V_S. In Figure 7(g), the channel 1 output is used as the bootstrap power supply for channel 2. DC-DC regulators using this bootstrap method are shown in Figure 16(a). If channel 1 is out of regulation, then channel 2 will be shut off by PGOOD1. Correct operation of channel 2 thus depends on the readiness of V_{OUT1}. This may be a drawback.

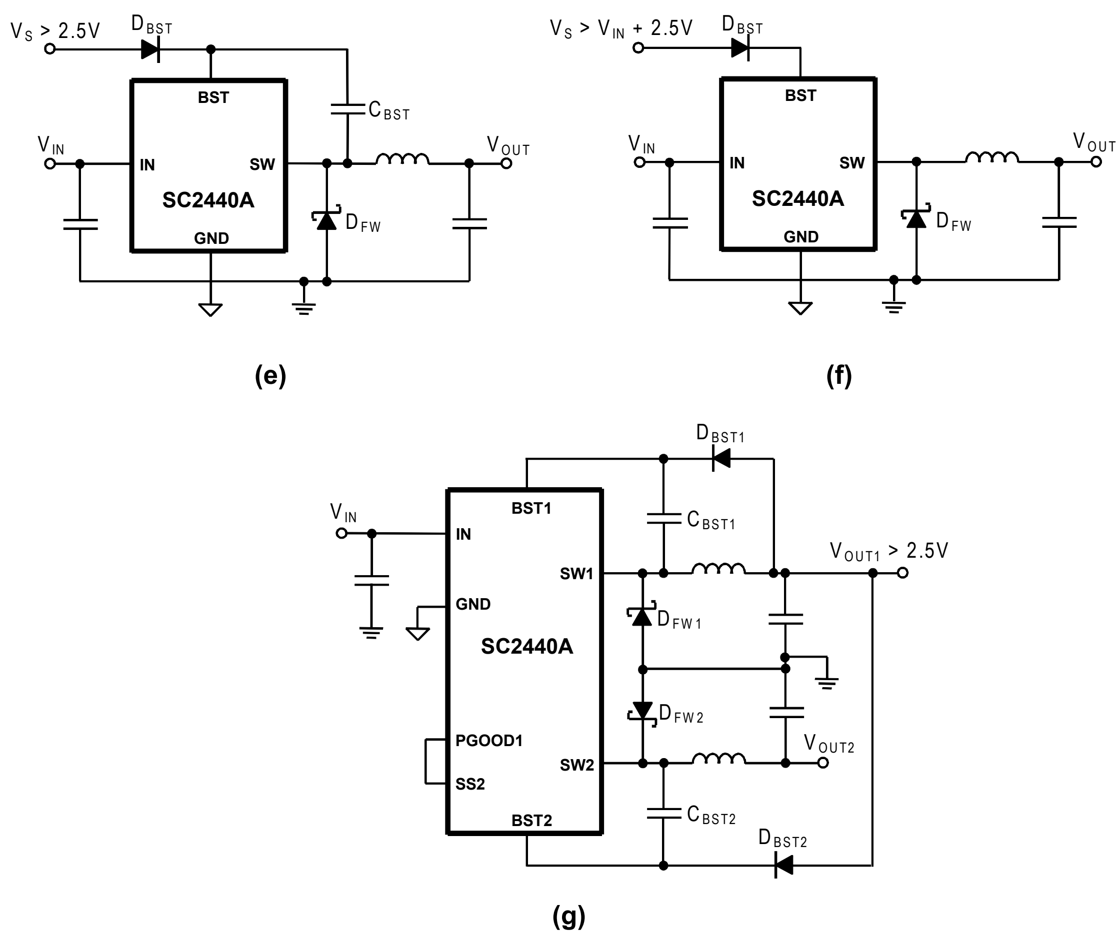


Figure 7(e)-(g). Bootstrap Configurations for the SC2440A (Continued)

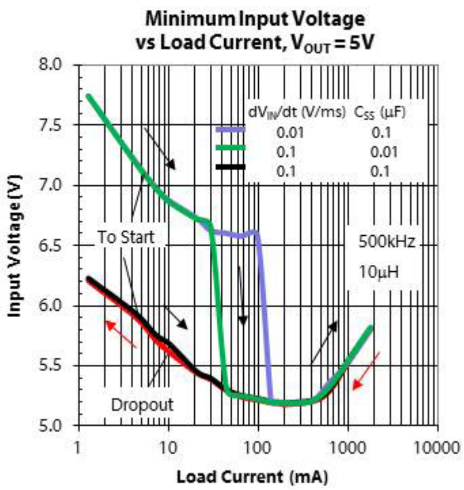
Applications Information (Continued)

The minimum C_{BST} value can be estimated as follows:

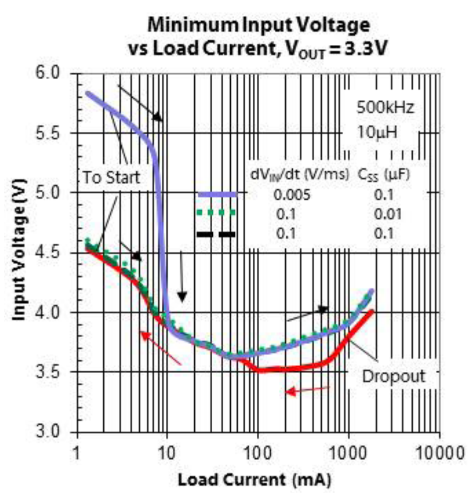
$$C_{BST} > \frac{I_{OUT(MAX)} \cdot D}{10 \cdot f \cdot (V_S - 2.4)} \qquad (10)$$

where V_S is the voltage applied to the anode of D_{BST}.

The inductor current charges the bootstrap capacitor when it pulls the SW node low during the switch off time.



(a)



(b)

Figure 8. The Minimum Input Voltage to Start and to Run Before Dropout. The regulator is bootstrapped from its output [Figure 7(a)] with 1N4148. The minimum starting V_{IN} decreases when C_{SS} or dV_{IN}/dt increases.
(a) V_{OUT} = 5V
(b) V_{OUT} = 3.3V

If D_{BST} is connected to the converter input, then C_{BST} will be charged as soon as V_{IN} is applied.

If the bootstrap diode is tied to the converter output [Figures 7(a), 7(c) and 7(g)], then C_{BST} can only be charged from the regulator output through the inductor. Before the converter starts, there is neither output voltage nor inductor current. Hence it is necessary for the regulator to deliver some inductor current to the output before C_{BST} can be charged. If V_{IN} is not much higher than the programmed V_{OUT} and it ramps up very slowly, then the inductor current will not be high enough for the bootstrap circuit to run, especially at light loads. In order to have some inductor current to charge C_{BST}, the converter output needs to be loaded or V_{IN} needs to be increased. Using a larger soft-start capacitor C_{SS} will also help the bootstrap circuit to run because there will be current in the inductor over a longer period of time. Figures 8(a) and 8(b) show the minimum input voltage required to start and run before dropping out as a function of the load current. The minimum start-up V_{IN} decreases with higher dV_{IN}/dt or larger soft-start capacitor C_{SS}. The lines labeled “dropout” in these graphs show that once started, the bootstrap circuit is able to sustain itself down to zero load.

Soft-Start

Each regulating channel of the SC2440A has its own soft-start circuit. Pulling its soft-start pin below 0.8V with an open-collector NPN or an open-drain NMOS transistor turns off the corresponding regulator. The other regulator continues to run. During startup the soft-start capacitors are charged as soon as V_{IN} exceeds its start threshold (2.71V). The converter remains off until I_C (see Figure 3) charges the soft-start capacitor above 1.3V. One of the non-inverting inputs of the error amplifier EA is connected to the output of amplifier A_1 (Figure 2). The voltage V_1 at this non-inverting input rises at twice the soft-start capacitor charging rate.

If the converter is to start into a constant current load I_{OUT} by releasing its SS pin with the input power supply already applied, then the sum of I_{OUT} and the C_{OUT} charging current will have to be less than the minimum switch cur-

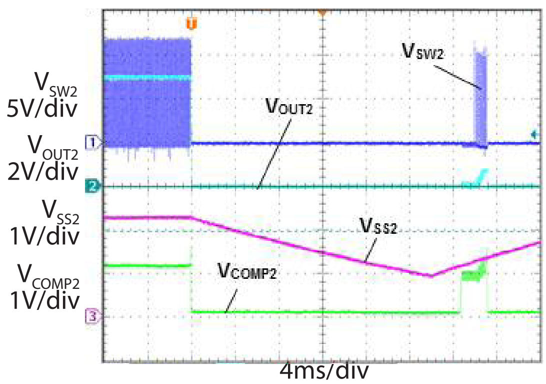
Applications Information (Continued)

rent limit. This places a minimum limit on C_{SS}:

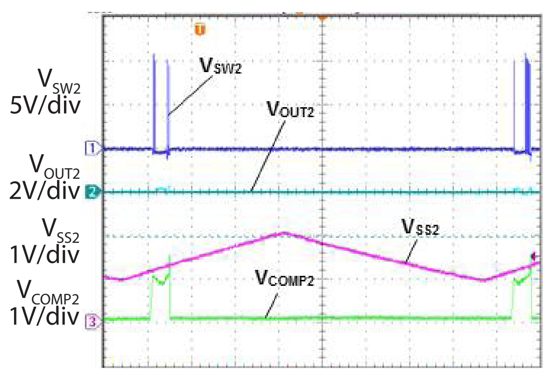
$$C_{SS} > \frac{3.6\mu A \cdot C_{OUT}}{2 - I_{OUT}} \quad (11)$$

where I_{OUT} is in amperes.

Starting the SC2440A by turning on a bench power supply will require much larger soft-start capacitors. C_{SS} is best determined empirically because the rise time of a power supply can range from a few milliseconds to a few hundred milliseconds. With the maximum load applied, the output rise is observed using a 22nF for C_{SS}. Adjust C_{SS} until a linear V_{OUT} ramp is achieved.



(a)



4ms/div
(b)

Figure 9. Overload Hiccup of the 5V Output Channel in Figure 1.
(a) Overload shutdown is triggered when I_{OUT2} is increased from 0.5A to 2.8A. The converter attempts to restart after a time out.
(b) The regulator output is shorted to ground. The converter switches only for a short duration over a hiccup cycle. As a result, short circuit power dissipation is very low.

Overload / Short-Circuit Protection

As described in the "General Description", comparator ILIM (Figure 2) limits the switch current on a cycle-by-cycle basis, restricting the available regulator output current to the load. This causes the output voltage to fall and the COMP voltage to rise. If overload persists, then COMP will be clamped and the regulator will undergo shutdown and restart (hiccup). Hiccup is triggered when an over-current condition causes clamping of the error amplifier output. The time taken for V_{COMP} to rise from its regulating voltage to the clamp level is the delay time before shutdown. A very short over-current condition is therefore ignored. Figure 9(a) captures the initial overload shutdown and the subsequent time out and retry. Clamping of the error amplifier output and C_{SS} discharge are evident.

If the regulator output is shorted to ground, then the COMP voltage will rise to its 1.7V upper clamp. The regulator will quickly reach its cycle-by-cycle current limit. As described in the "General Description", the regulator will shut off and undergo hiccup regardless whether soft-start is completed. The regulator restarts normally after the short at its output is removed. Short-circuit startup waveforms are captured in Figure 9(b). The converter switches only for a short period of time over a hiccup cycle. Short circuit power dissipation is substantially reduced.

Power Good Indicators

The PGOOD pins (Pins 11 and 14) are the open-collector outputs of the power good comparators. These slow comparators are incorporated with a small hysteresis. The FB low-to-high trip voltage of the power good comparators is 90% of the final regulation voltage. A pull-up resistor from each PGOOD pin to the input supply or the regulator output sets the PGOOD logic high voltage.

The power good comparator output becomes valid provided that V_{IN} is above 0.9V. In shutdown the power good output is actively pulled low. A power good pull-up resistor tied to the input will therefore increase current drain during shutdown. Tying the power good pull-up resistor to the regulator output is preferred, as this will minimize the shutdown supply current. In shutdown there is no voltage at the switching regulator output or current in the

Applications Information (Continued)

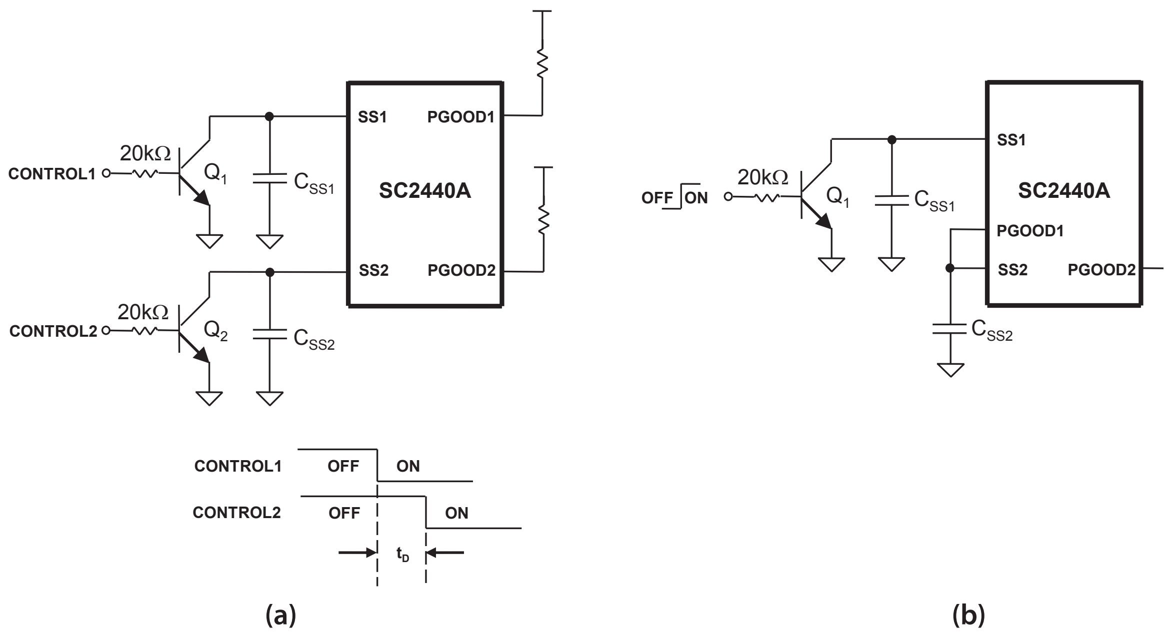


Figure 10. Sequencing the Outputs by (a) Delaying Release of one Channel Relative to the Other and (b) Using the PGOOD of one Channel to Control the Other.

PGOOD pull-up resistor. If the PGOOD output high level (= V_{OUT}) is unacceptably low, then tying the power good pull-up resistor to the input or to a separate power supply will be the only choice.

Sequencing the Outputs

As mentioned above, pulling either soft-start pin low with an external transistor shuts off the corresponding regulator (Figure 10). Releasing the soft-start pin enables that channel and allows it to start. Delaying the release of the soft-start pin of one channel with respect to the other is a straightforward way of sequencing the outputs. Figure 10(a) shows this method using two external transistors Q_1 and Q_2. Q_1 is turned off first, allowing channel 1 to start. Channel 2 is then enabled after time t_D.

The PGOOD output of one channel can also be used in conjunction with the soft-start pin of the other channel to delay start of that regulator. This method is depicted in Figure 10(b). SS2 is pulled low and channel 2 is kept off until the channel 1 output rises to 90% of its set voltage.

Loop Compensation

Each step-down switching regulator in the SC2440A requires a simple Type-2 compensation network (Figure 11) for stable operation. C_Z and R_Z form a compensating zero. This zero nulls out the effect of two low-frequency poles in the feedback loop and allows the loop amplitude response to cross unity gain at -20 dB/decade. Increasing

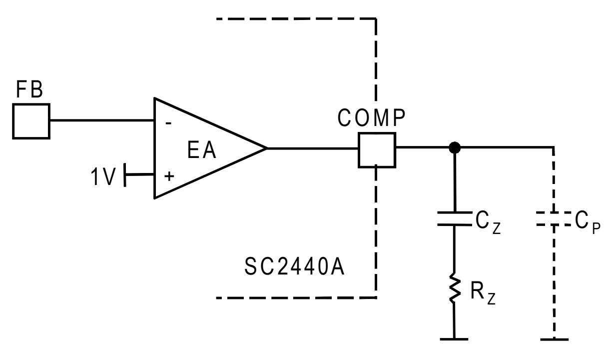


Figure 11. Compensation Network for Each Regulator.

Applications Information (Continued)

R_Z increases the mid-band loop gain and the crossover frequency. However the converter becomes less stable. Using a linear equivalent model and setting the loop gain crossover frequency to one-tenth the switching frequency, R_Z can be calculated:

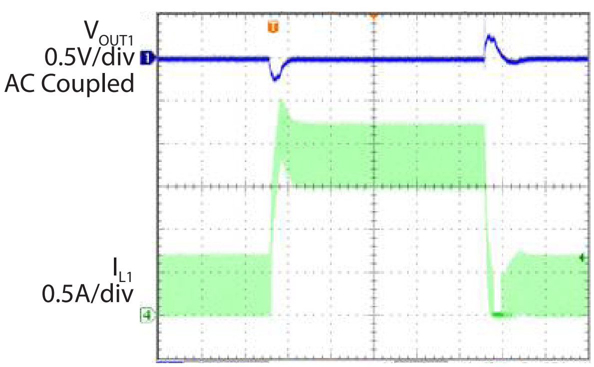
$$R_Z = 217 \cdot f \cdot C_{OUT} V_{OUT} \tag{12}$$

where R_Z is in Ω.

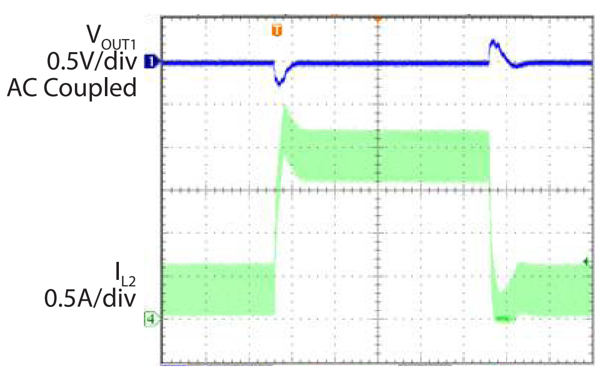
C_Z can be determined by setting the zero frequency to one-fifth of the loop gain crossover frequency:

$$C_Z = \frac{7.96}{f \cdot R_Z} \tag{13}$$

where C_Z is Farads.



(a)



(b)

**Figure 12. Load Transient Response of the Converter in Figure 1.
(a) Channel 1 (3.3V) Load Transient Response, I_{OUT1} is switched between 0.3A and 1.8A.
(d) Channel 2 (5V) Load Transient Response, I_{OUT2} is switched between 0.3A and 1.8A.**

The capacitor C_P from COMP to ground rolls off the loop gain at high frequency. C_P is generally not required for stability. In some cases, the addition of a small capacitor (10 to 22pF) from the COMP pin to ground eliminates SW falling edge jitter.

R_Z and C_Z calculated above are based upon a linear equivalent circuit which does not model the non-linear nature of switching regulators very well. It is imperative to verify loop compensation by checking regulator load transient response. With the largest load step pertinent to the application applied, the regulator output voltage and the inductor current are observed. These transient waveforms should not show any ringing or excessive overshoot (see Figures 12(a) and 12(b) for examples of stable load transient waveforms.). If necessary, adjust R_Z until a stable transient is obtained. The $R_Z C_Z$ product is to be kept constant during tuning.

Board Layout Considerations

In a step-down switching regulator, the input bypass capacitor, the main power switch and the freewheeling diode carry pulse currents with high $\frac{di}{dt}$ (Figure 13). For jitter-free operation, the size of the loop formed by these components should be minimized. Since the power switches are already integrated within the SC2440A, con-

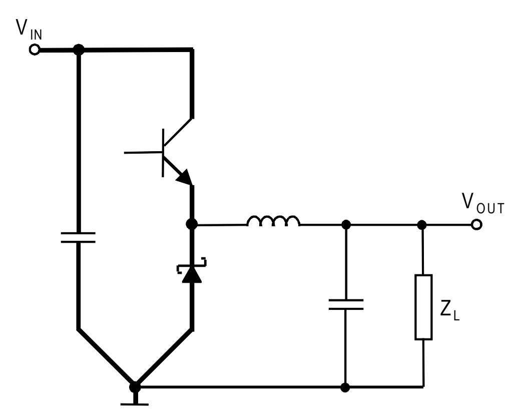


Figure 13. Fast Switching Current Paths in a Step-down Converter. The input capacitor and the freewheeling diode should be placed close to the part for improved switching performance.

Applications Information (Continued)

necting the anodes of both freewheeling diodes close to the negative terminal of the input bypass capacitor minimizes size of the switched current loop. The input bypass capacitors should be placed close to the IN pins. Shortening the traces of the SW and BST nodes reduces the parasitic trace inductance at these nodes. This not only reduces EMI but also decreases switching voltage spikes at these nodes.

Figure 14 shows an example of external component placement around the SC2440A. The input bypass capacitor C_{15}, the output filtering capacitors and the freewheeling diodes are grounded on the power ground plane. The feedback resistor dividers, the compensation networks and the soft-start capacitors are to be tied to analog ground. The frequency-setting resistor R_9 is placed next to the ROSC pin and is also connected to analog ground.

The exposed pad should be soldered to a large power ground plane as the ground copper acts as a heat sink for the device. To ensure proper adhesion to the ground plane, avoid using large vias directly under the device. In Figure 14(a) two 12mil vias are placed at the edge of the underside pad.

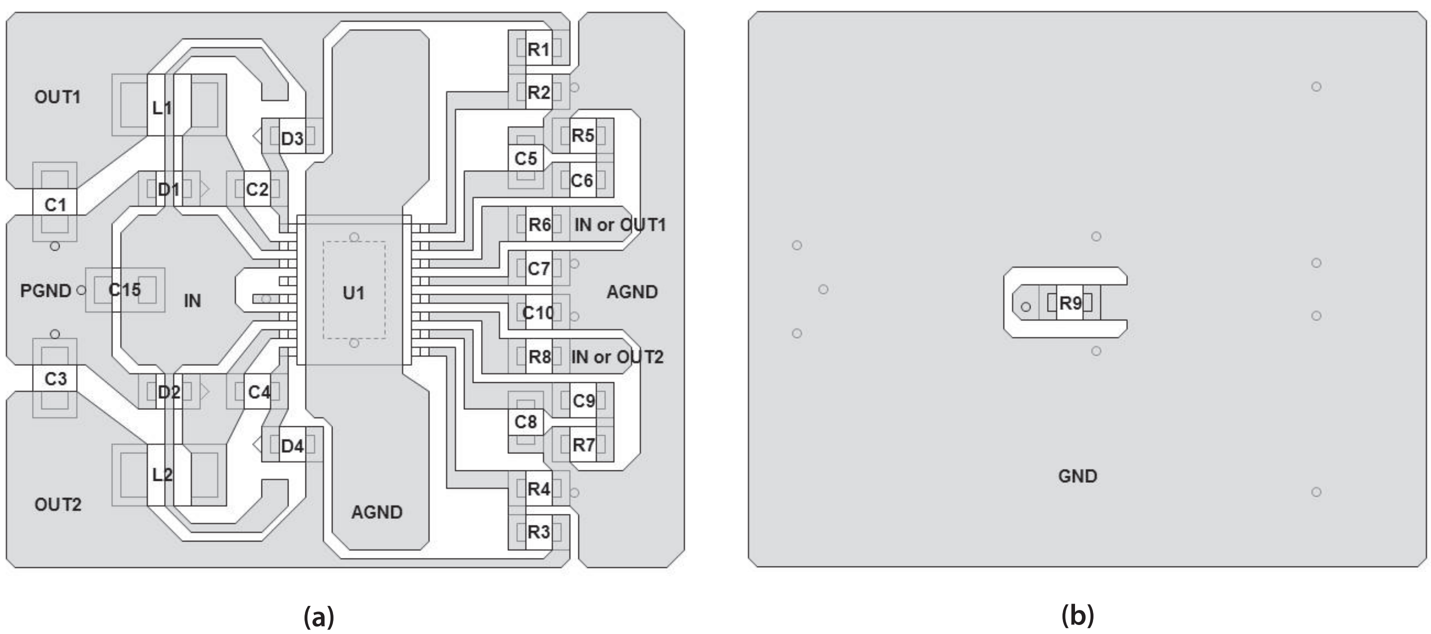
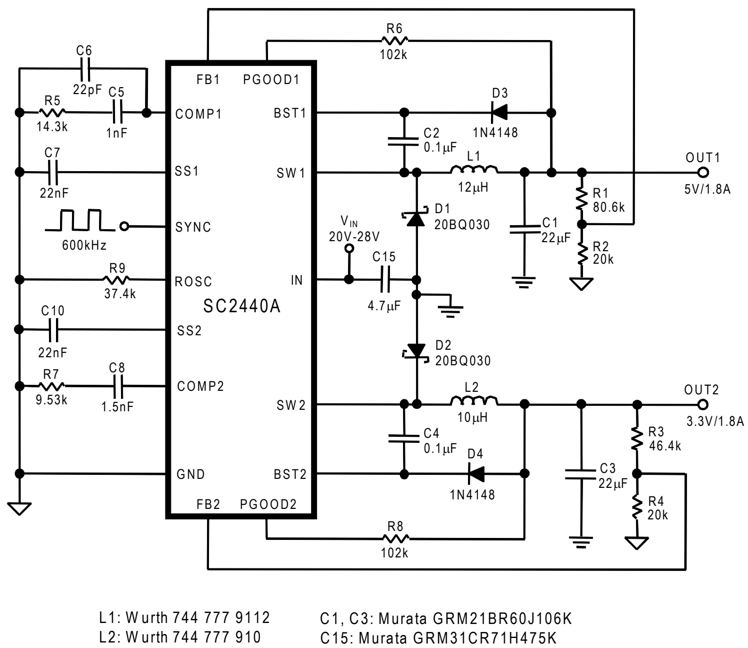
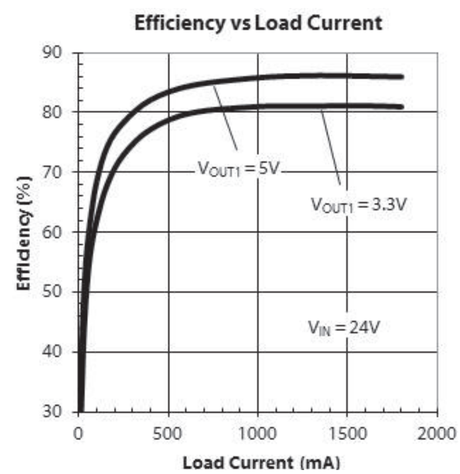


Figure 14. Suggested PCB Layout for the SC2440A (a) Top Layer and (b) Bottom Layer

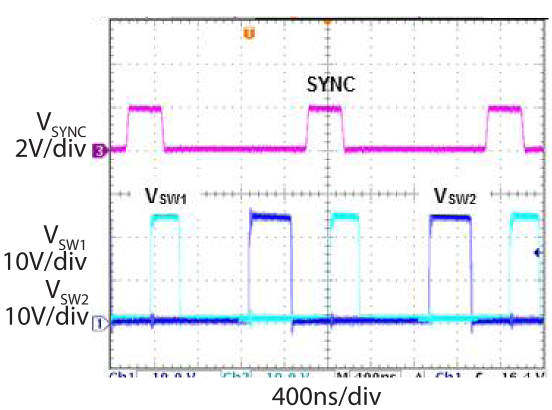
Typical Application Circuits (Continued)



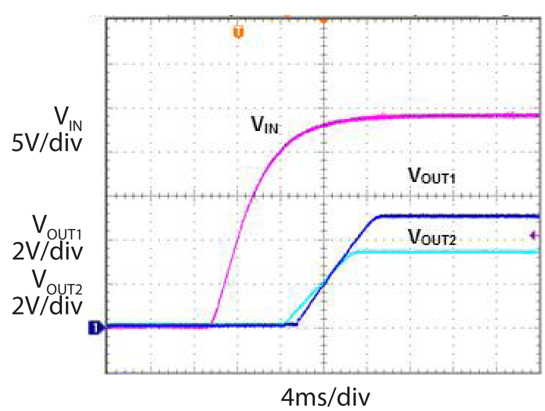
(a)



(b)



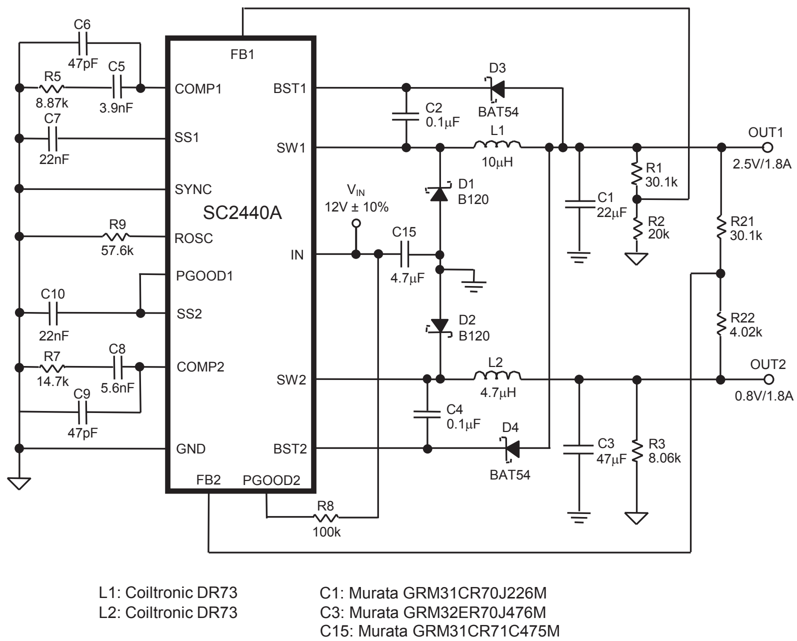
(c)



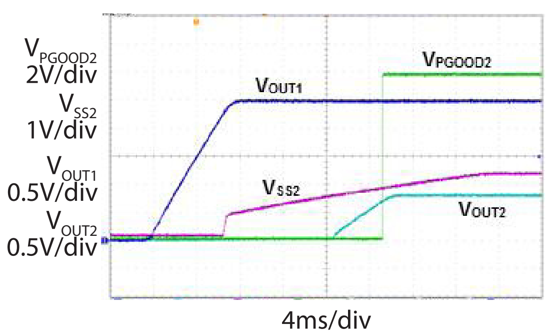
(d)

Figure 15. (a) Synchronized 600kHz 24V to 5V and 3.3V Dual Step-down Converter. The free-running frequency of the regulator is set to 580kHz.
(b) Efficiency
(c) Switching Waveforms. V_{IN} = 24V, I_{OUT1} = I_{OUT2} = 1A.
(d) Start-up Waveforms. V_{IN} = 24V, I_{OUT1} = I_{OUT2} = 0.5A.

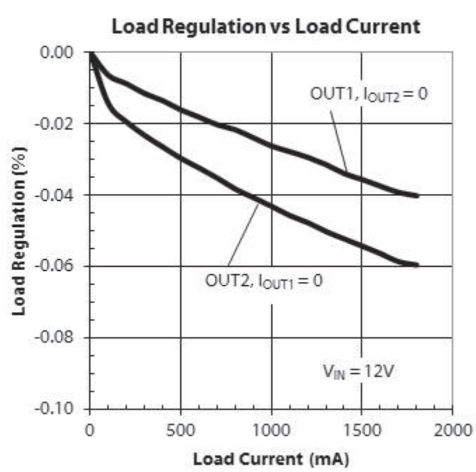
Typical Application Circuits (Continued)



(a)



(b)



(c)

Figure 16. Stepping Down to a Voltage Lower Than the Feedback Voltage.
(a) 400kHz 12V to 2.5V and 0.8V Step-down Converter.
R_3 is a pre-load to shunt the current from R_{21} and R_{22} before PGOOD1 releases SS2.
(b) Start-up waveform ($I_{OUT1} = I_{OUT2} = 1A$).
(c) Channel 2 load regulation is slightly below that of channel 1 because V_{FB2} is derived from V_{OUT1}.

Typical Application Circuits (Continued)

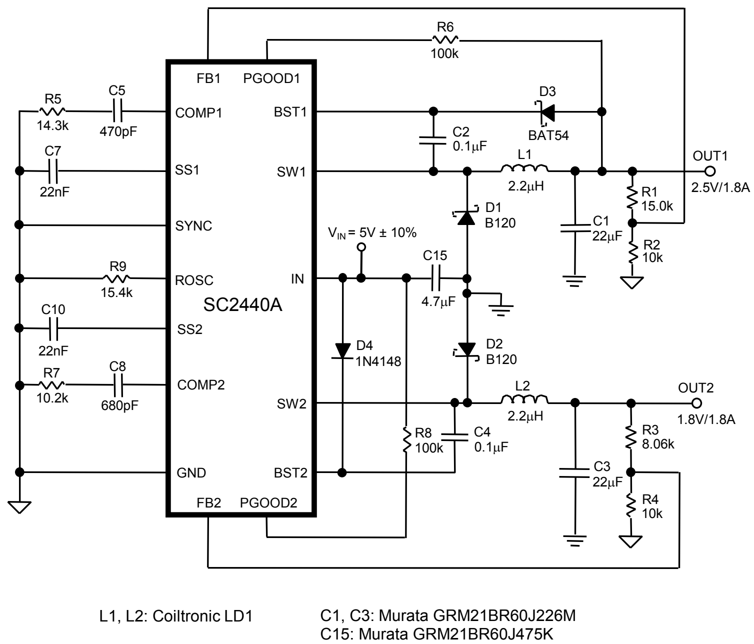


Figure 17. 1.2MHz 5V to 2.5V and 1.8V Step-down Converter.

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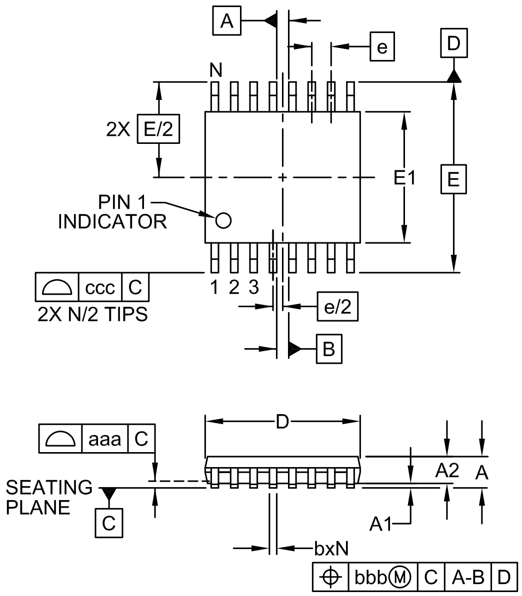
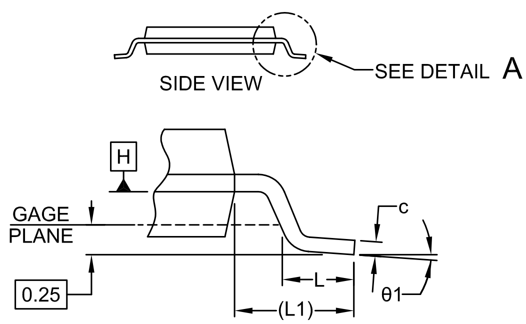
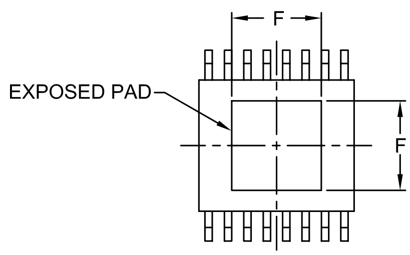
Outline Drawing – TSSOP-16 EDP



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.001	-	.006	0.025	-	0.15
A2	.031	-	.041	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.004	-	.008	0.09	-	0.20
D	.193	.197	.201	4.90	5.00	5.10
E1	.169	.173	.177	4.30	4.40	4.50
E		.252 BSC			6.40 BSC	
e		.0256 BSC			0.65 BSC	
F	.112	.118	.122	2.85	3.00	3.10
L	.018	.024	.030	0.45	0.60	0.75
L1		(.039)			(1.0)	
N		16			16	
θ1	0°	-	8°	0°	-	8°
aaa		.004			0.10	
bbb		.004			0.10	
ccc		.008			0.20	



DETAIL A



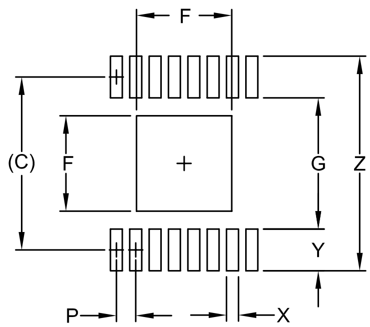
BOTTOM VIEW

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

SEMTECH

Land Pattern – TSSOP-16 EDP



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
F	.126	3.20
G	.161	4.10
P	.0256	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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