SC3203

3A EcoSpeed® Step-Down Regulator with Power Save

POWER MANAGEMENT

Features

- Input voltage — 9V to 16V
  - Programmable VIN UVLO
- Output voltage adjustable from 0.75V to 7.5V
- Output current — Up to 3A
- Internal reference — ± 2%
- Supports ceramic capacitors
- Low component count
- Power good output (open-drain)
- Low RDS_{ON} mosfets
  - 65mΩ low-side/100mΩ high-side
- ENABLE input
  - Programmable VIN UVLO and hysteresis
- VIN Under-Voltage Lock Out
- 500kHz switching frequency
- Adaptive on-time control:
  - Excellent transient response
  - Pseudo-fixed frequency during CCM
- Fault protection features:
  - Over-current/Over-voltage/Under-voltage
  - Over-temperature
  - Automatic Restart (Hiccup)
- Internal soft-start
- Start-up into pre-bias output
- Power Save and Smart Power Save
- Internal LDO for bias voltage
- SOIC8-EP5 lead-free package
- WEEE and RoHS compliant and halogen-free

Description

The SC3203 is an integrated, synchronous 3A EcoSpeed® step-down regulator. It incorporates Semtech's advanced, patented adaptive on-time architecture to achieve best-in-class dynamic performance using point-of-load applications. The input voltage range is 9V to 16V, and the output voltage is adjustable from 0.75V to 7.5V. The device features an internal LDO and automatic PSAVE mode for high efficiency across the output load range.

Switching frequency is internally programmed to 500kHz. Semtech's adaptive on-time control provides pseudo-fixed frequency operation in continuous conduction combined with excellent transient performance.

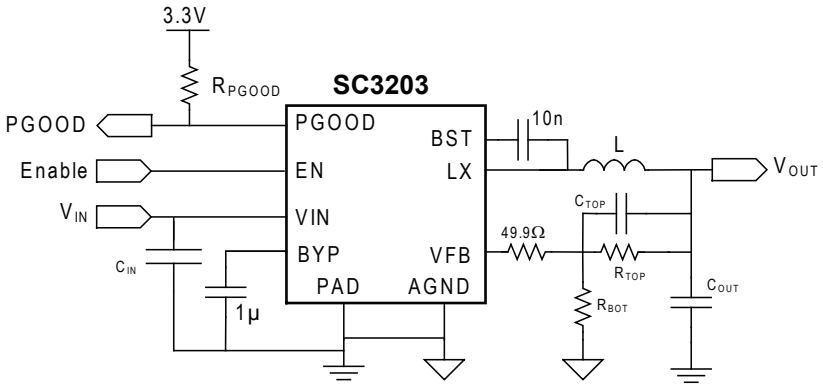
Additional features include cycle-by-cycle current limit, soft start, output over voltage and over temperature protection, and automatic fault recovery. The open-drain PGOOD pin provides output status.

The device is available in a lead-free SOIC8-EP5 package.

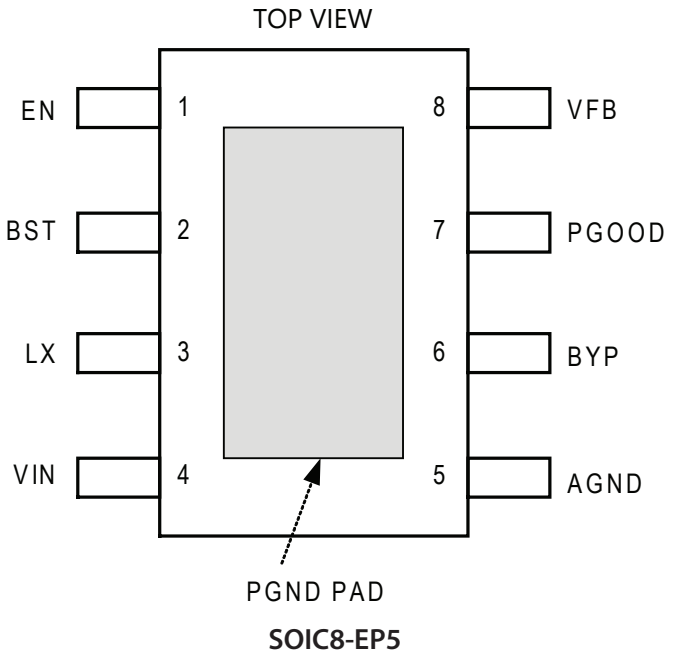
Applications

- Consumer Electronics, DTV and Set-top Boxes
- Networking Equipment, Embedded Systems
- Medical Equipment, Office Automation
- Instrumentation, Portable Systems
- Point of Load Converters

Typical Application Circuit



Pin Configuration



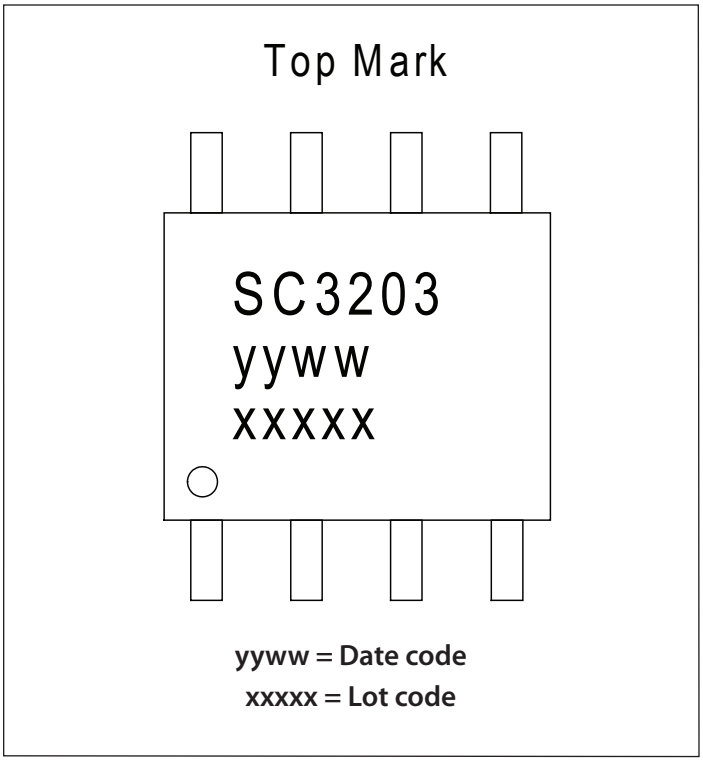
SOIC8-EP5

Ordering Information

Device [1][2]	Package
SC3203SETRC	SOIC8-EP5
SC3203EVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



yyww = Date code
xxxxx = Lot code

Absolute Maximum Ratings

LX to PGND (V) ..... -0.3 to +18
EN to PGND (V) ..... -0.3 to +18
VIN to PGND (V) ..... -0.3 to +18
BST to LX (V) ..... -0.3 to +6.0
BST to PGND (V) ..... -0.3 to +23
BYP to PGND (V) ..... -0.3 to +6.0
PGOOD to AGND (V) ..... -0.3 to +6.0
VFB to AGND (V) ..... -0.3 to BYP +0.3
AGND to PGND (V) ..... -0.3 to 0.3
Maximum Peak Inductor Current (A) 5.0
Peak IR Reflow Temperature (°C) 260
BST to LX Capacitance (nF) 15
ESD Protection Level (kV)(1) 5kV

Recommended Operating Conditions

Supply Input Voltage (V) ..... 9 to 16
Maximum Continuous Output Current (A) 3.0
Maximum Peak Inductor Current (A) 4.0

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal Resistance Junction to Ambient(2) (°C/W) 36
Thermal Resistance Junction to Case(2) (°C/W) 5.5

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114-B.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, T_A=+25°C for Typ, -40°C to +85°C for Min and Max, T_J < 125°C, per detailed application circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supply					
VIN UVLO Threshold	VIN rising edge, EN = VIN		4.40	4.55	V
	Hysteresis, EN = VIN		0.30		V
VIN Supply Current	V_{EN} = 0V			10	µA
	No switching, I_{OUT} = 0A, VFB 5% higher than the VFB On-time Threshold		0.35		mA
Controller					
VFB On-Time Threshold Accuracy		736	750	766	mV
VFB Input Bias Current			0.2		µA

Electrical Characteristics (continued)

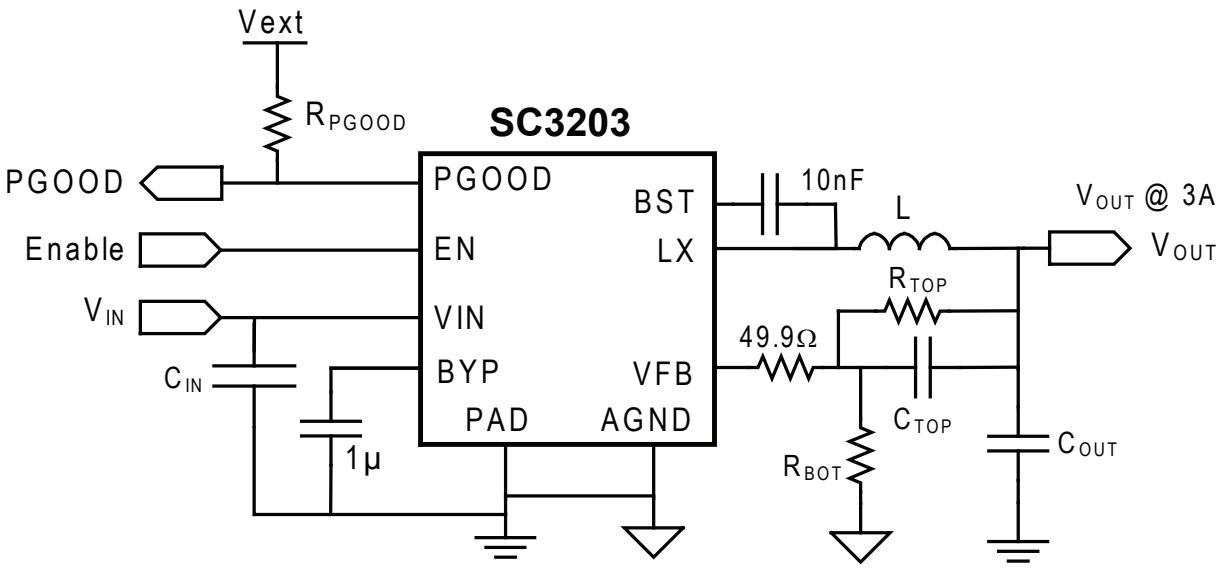
Parameter	Conditions	Min	Typ	Max	Units
Timing					
On-time accuracy	VIN = 12V, VOUT = 3.3V	476	560	644	ns
Minimum Off-Time			260		ns
Automatic Restart Cycle Time			32		ms
Soft start					
Soft start Time	From PWM Switching to Output Regulation		1.8		ms
Current Sense					
Zero-Crossing Detector Threshold	LX - PGND	-10	0	+10	mV
Fault Protection					
Output Under-Voltage Threshold	VFB with respect to nominal, 8 Consecutive Switching Cycles		75		$\%V_{REF}$
Output Over-Voltage Threshold	VFB with respect to nominal		120		$\%V_{REF}$
Smart PowerSave Protection Threshold	VFB with respect to nominal		110		$\%V_{REF}$
OV, UV Fault Noise Immunity Delay			2.5		µs
Over-Temperature Shutdown			160		°C
PGOOD Output					
PGOOD Startup Delay Time	From EN rising edge to PGOOD high		3.3		ms
PGOOD Under-voltage Threshold	FB rising edge		90		%
	FB falling edge		85		%
PGOOD Over-voltage Threshold	FB rising edge		120		%
Enable Input[1]					
EN Input Logic High Threshold (V_{EN_BYP})	VIN = 12V; EN rising edge; BYP on; Switcher off		1.0		V
EN Input Logic High Threshold (V_{EN_ON})	VIN = 12V; EN rising edge; BYP on, Switcher on		1.5		V
EN Input Voltage Hysteresis	Hysteresis at V_{EN_ON} threshold		100		mV
EN Input Current Hysteresis	Hysteresis at V_{EN_ON} threshold		1.75		µA
EN Input Bias Current	V_{EN} = 12V	-1		10	µA
EN Input Resistance	EN $\leq V_{EN\_ON}$ Threshold; EN rising edge		810		kΩ

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Boost Switch					
BST Switch On-Resistance	BYP = 5V		12		Ω
Internal Power mosfets					
Current Limit	Inductor Valley Current Limit, LDO=5V	3.0	3.75	4.5	A
High Side LX Leakage Current	VIN=16V, LX=0V, High Side mosfet off		1	5	µA
Switch Resistance	High Side		100		mΩ
	Low Side		65		

Note:
(1) See Applications Information for a description of the EN input operation.

Detailed Application Circuit

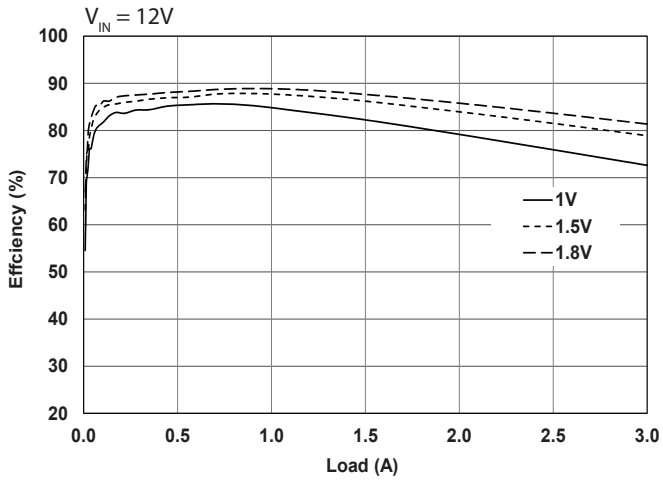


Component Selection

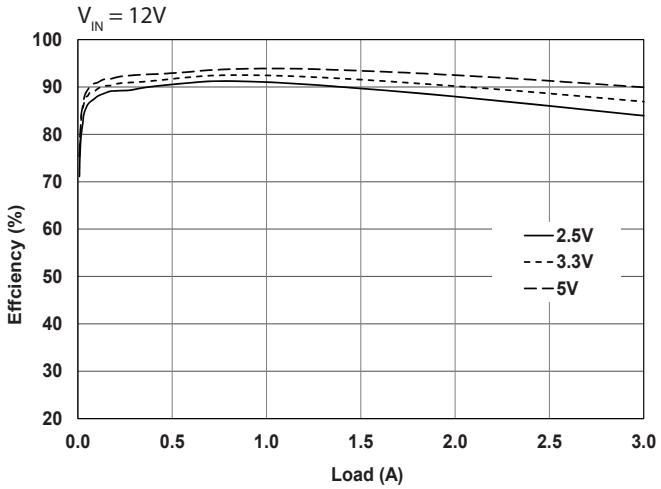
V_{OUT} (V)	0.9V	1.0V	1.1V	1.2V	1.5V	1.8V	2.5V	3.3V	5.0V
L (µH)	2.2						4.7		
C_{OUT} (µF)	2x22uF X5R, 0805 case, 10V						2x10uF X5R, 0805 case, 10V		
R_{TOP} (kΩ)	39.2	66.5	31.6	30.1	24.3	20.5	19.6	16.5	26.1
R_{BOT} (kΩ)	200	200	69.8	51.1	24.9	15	8.66	4.99	4.75
C_{TOP} (pF)	22	18	27	33	39	47	68	82	82

Typical Characteristics

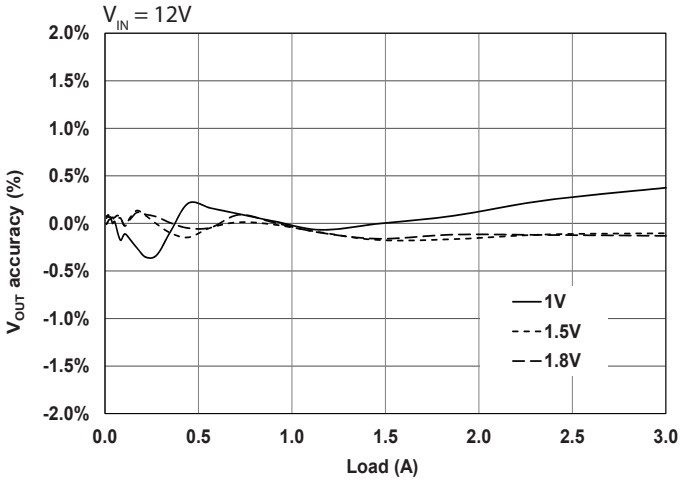
Efficiency vs Load — 1V, 1.5V, 1.8V output



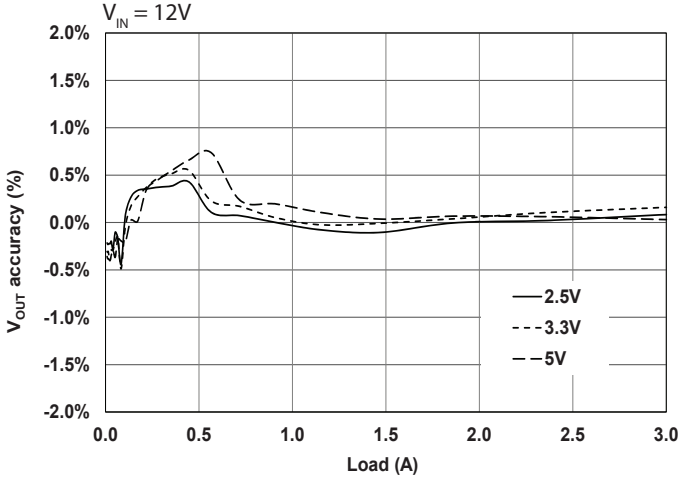
Efficiency vs Load — 2.5V, 3.3V, 5V output



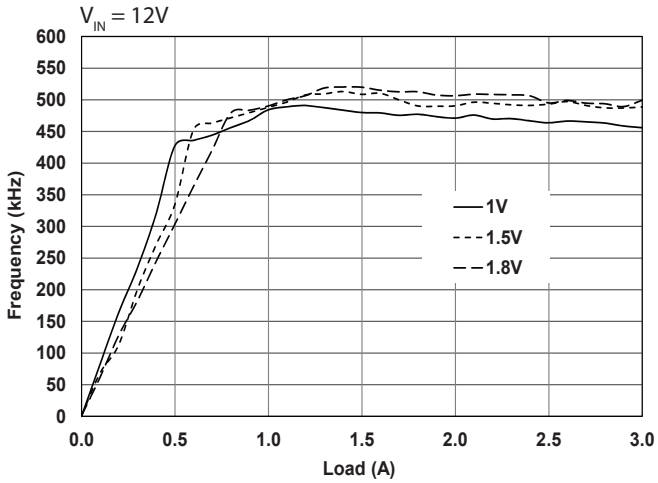
Load Regulation - 1V, 1.5V, 1.8V output



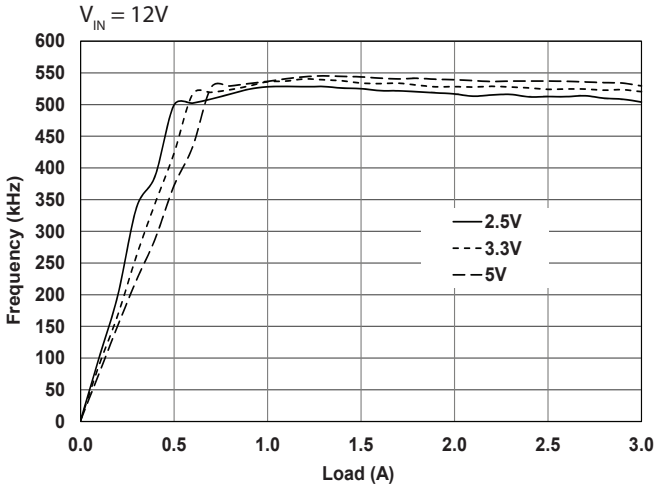
Load Regulation - 2.5V, 3.3V, 5V output



Switching Frequency vs Load - 1V, 1.5V, 1.8V

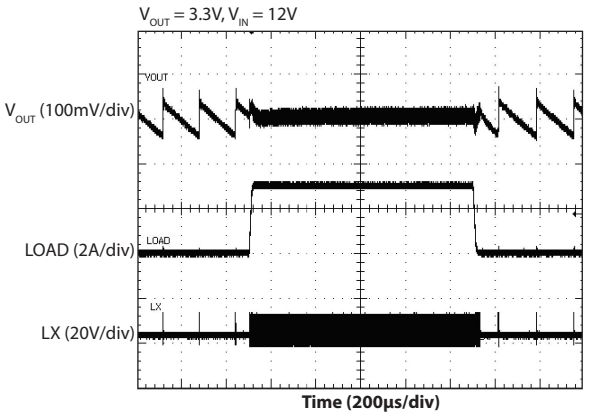


Switching Frequency vs Load - 2.5V, 3.3V, 5V

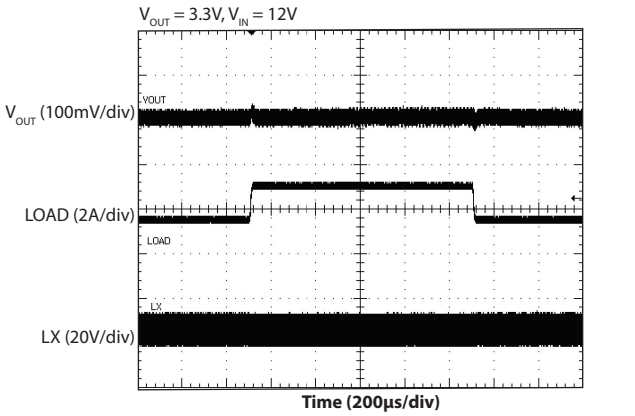


Typical Characteristics (continued)

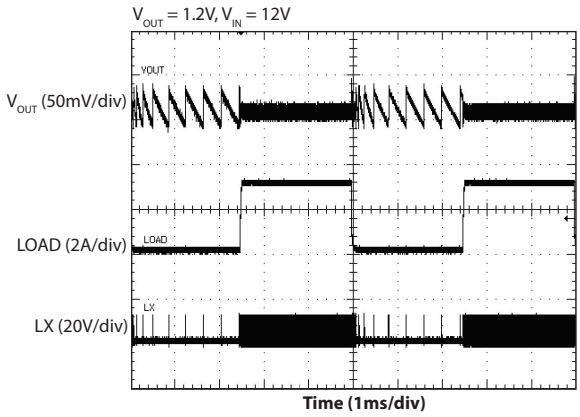
Load Transient, 0A to 3A to 0A - 3.3V$_{OUT}$



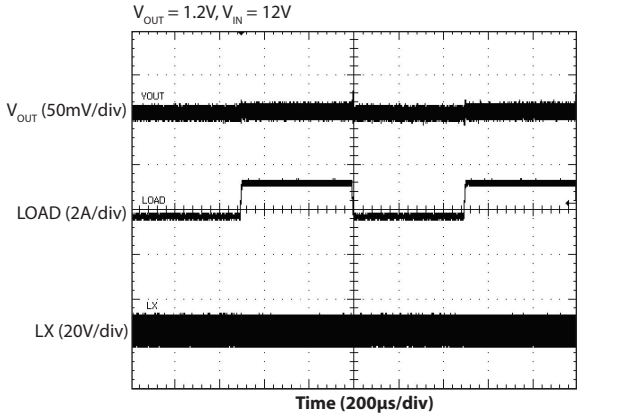
Load Transient, 1.5A to 3A to 1.5A - 3.3V$_{OUT}$



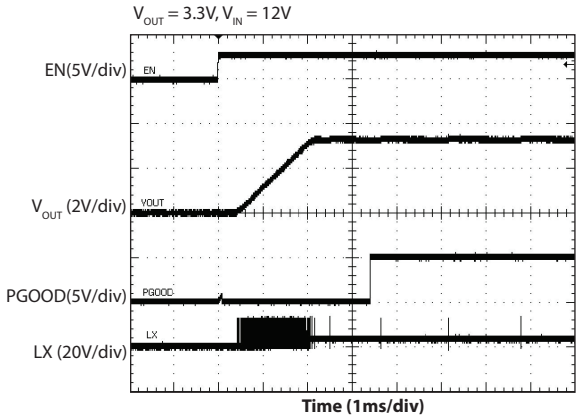
Load Transient, 0A to 3A to 0A - 1.5V$_{OUT}$



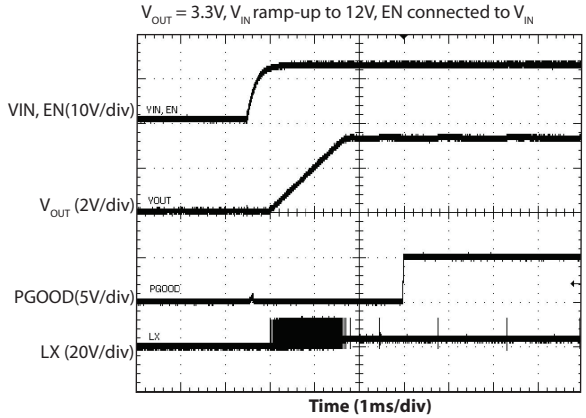
Load Transient, 1.5A to 3A to 1.5A - 1.5V$_{OUT}$



Startup - EN controlled



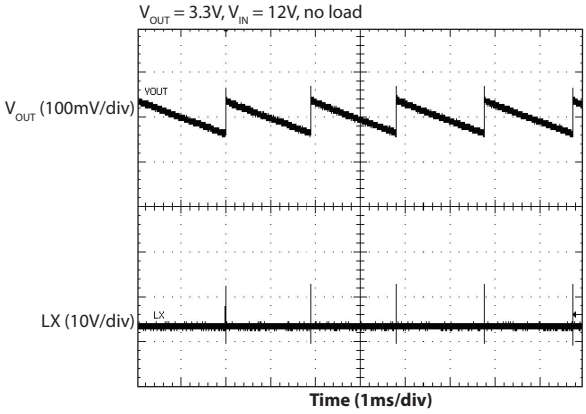
Startup - V_{IN} ramp



Typical Characteristics (continued)

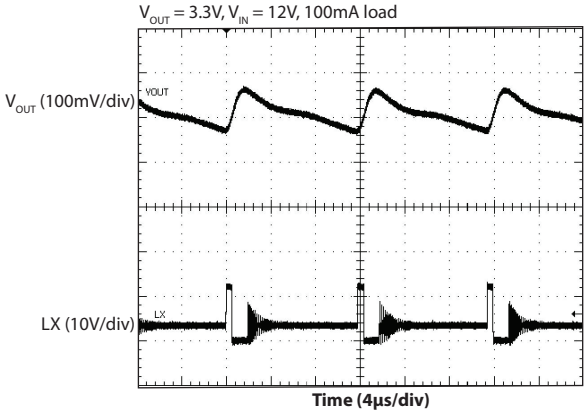
Power Save Switching - No Load

V_{OUT} = 3.3V, V_{IN} = 12V, no load



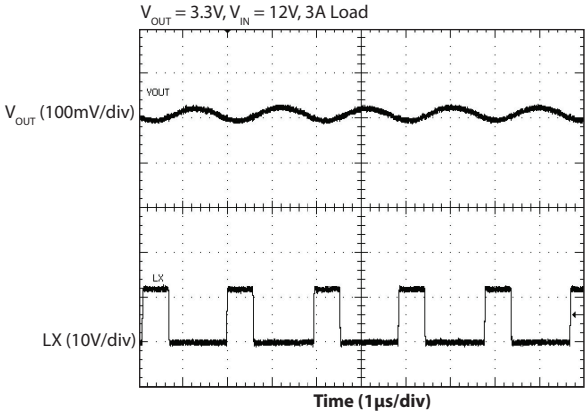
Power Save Switching - 100mA Load

V_{OUT} = 3.3V, V_{IN} = 12V, 100mA load



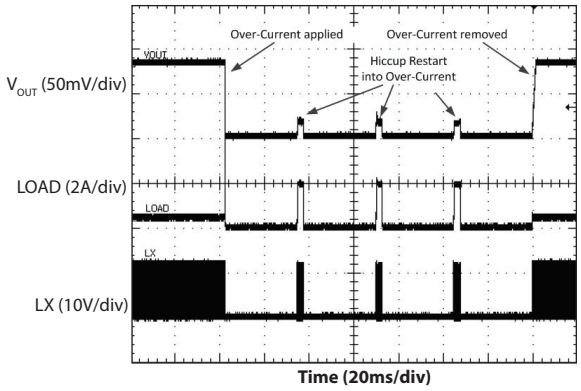
Continuous Mode Switching - 3A Load

V_{OUT} = 3.3V, V_{IN} = 12V, 3A Load



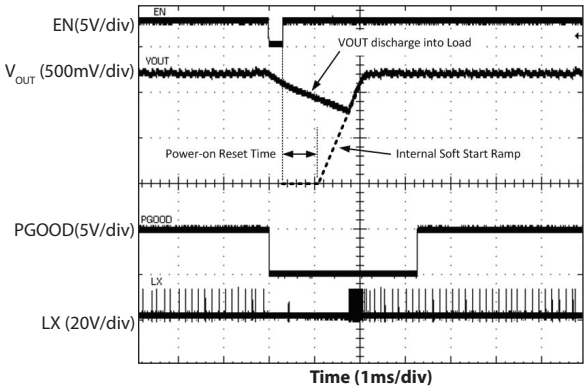
Hiccup Recovery from Over-Current

V_{OUT} = 1.2V, V_{IN} = 12V



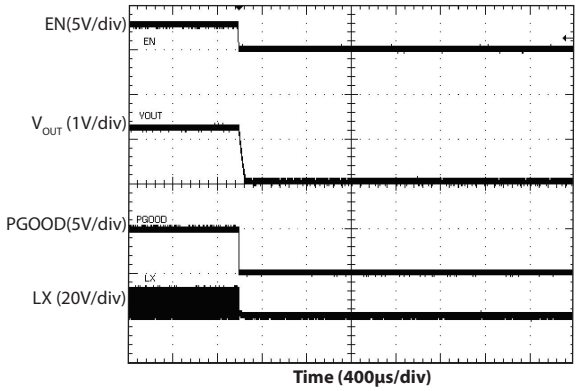
Pre-bias Startup

V_{OUT} = 1.2V, V_{IN} = 12V, Load = 10mA



Shutdown via EN control

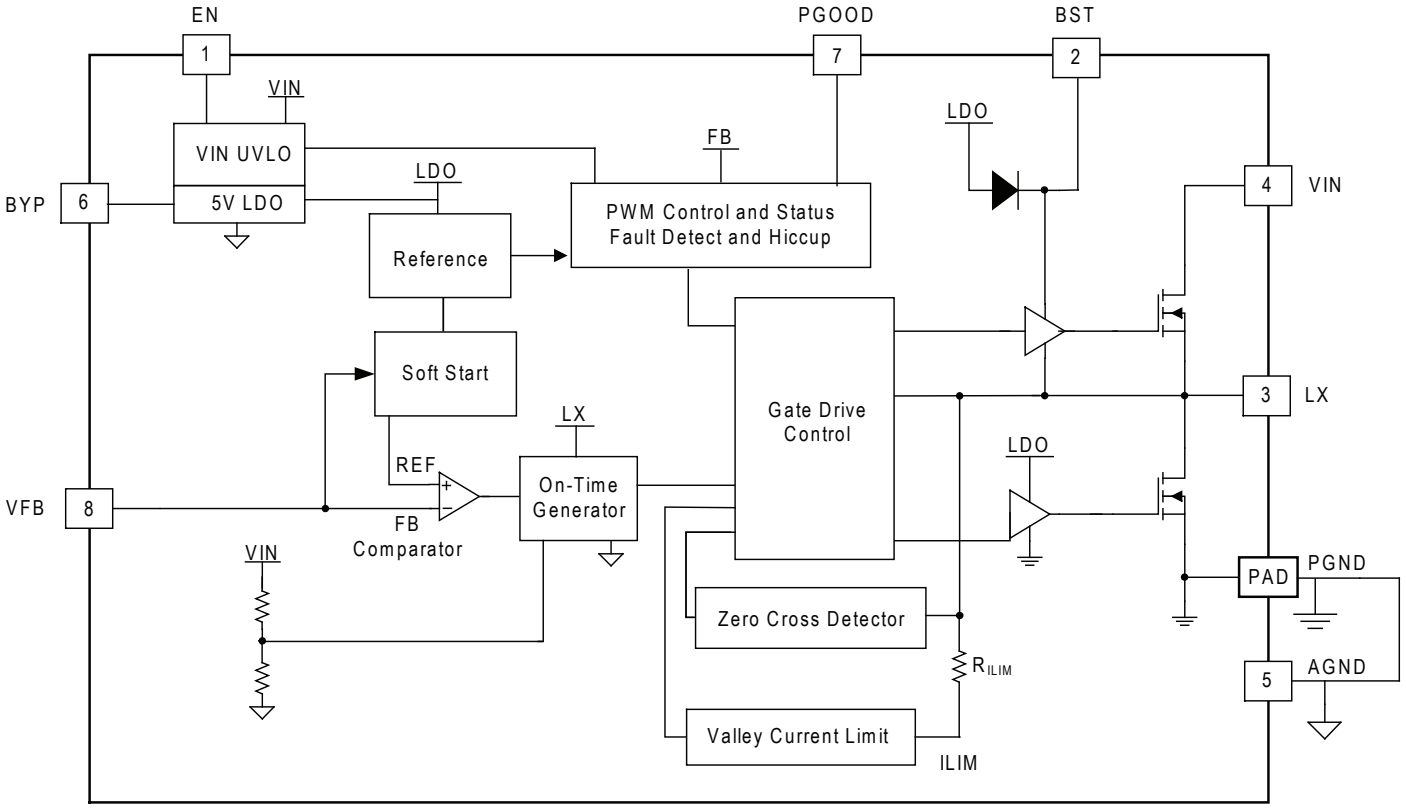
V_{OUT} = 1.2V, V_{IN} = 12V, Load = 1A



Pin Descriptions

Pin #	Pin Name	Pin Function
1	EN	Enable input for switching regulator —Pull EN high to enable the LDO and PWM. Connect to PGND to disable the PWM. Connect a resistor divider from VIN to program the external VIN Under-voltage threshold.
2	BST	Boost Supply pin — Connect a 10nF capacitor between BST and LX to develop the floating voltage for the high-side gate drive.
3	LX	Switching (phase) node. LX is also the sense point for the Zero Current Detector.
4	VIN	Power input for the High Side Mosfet and for the input to the LDO. VIN is the also sense point for the internal VIN Under-voltage Lockout and the VIN input for the On-time Generator.
5	AGND	Ground for the internal analog circuitry. Connect this directly to the PAD for the PGND connection.
6	BYP	Bypass pin for the internal 5V LDO which supplies bias voltage for the analog and gate drive circuits— A 1uF decoupling capacitor is required — The LDO is enabled when the EN pin exceeds typically 1V.
7	PGOOD	Open-drain Power Good output.
8	VFB	Feedback input — Connect this pin to a resistor/capacitor divider between the output voltage and AGND. See the Table on the Typical Application Circuit for recommended values.
PAD	PGND	Power ground connection. PAD is ground for the power circuits of the IC. The PGND pad should connect directly to the AGND pin, see Layout Guidelines.

Block Diagram



Applications Information

Synchronous Buck Converter

The SC3203 is a step down synchronous buck DC-DC regulator. The device supports 3A operation at high efficiency in an SOIC-8 package. The buck regulator employs pseudo-fixed frequency adaptive on-time control. The 500kHz operating frequency enables the user to optimize the design for minimal board space and optimum efficiency. The adaptive on-time control provides fast transient response and allows reduced size for the power filter.

Input Voltage Range

The SC3203 operates over the input range of 9V to 16V. The internal LDO generates a fixed 5V output that provides bias power for the device.

Adaptive On-time Control

The pseudo-fixed frequency, adaptive on-time control is shown in Figure 1. The ripple voltage generated at the output capacitor is divided down by the feedback resistor network and used as a PWM ramp signal. When the FB pin falls to the FB threshold a single on-time pulse for the high-side mosfet Q1 is triggered.

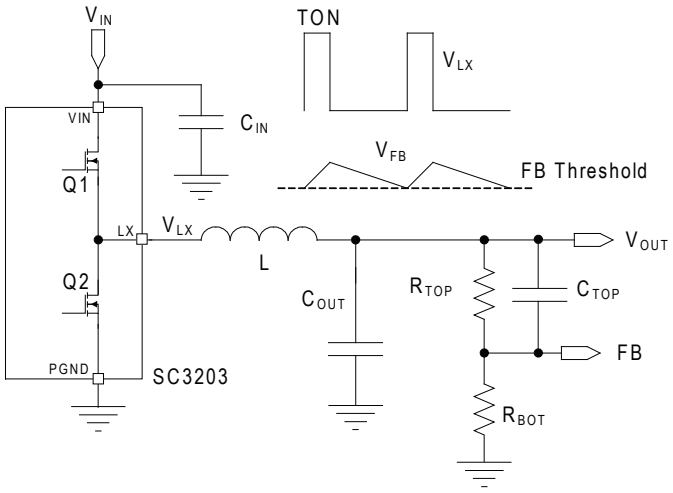


Figure 1 — Adaptive On-time Control

One-Shot Timer and Operating Frequency

When the FB pin falls to the FB Threshold (750mV), the device sends a single on-time pulse to the high-side mosfet.

The on-time pulse width is determined by the DC voltage of LX and by V_{IN}. The pulse width is proportional to the DC voltage of LX and inversely proportional to the input voltage. With this adaptive on-time design, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition. The on-time is approximated by the following equation:

$$t_{ON} = \frac{V_{LX}}{V_{IN} \times 500kHz}$$

When the on-time completes, the low-side mosfet Q2 (Figure 1) is turned on. Q2 must stay on for the minimum off-time of 260nsec, and remains on until one of the following occurs:

- V_{FB} falls below the 750mV reference. If this occurs, Q2 turns off and Q1 turns on for another high-side on-time.
- If operating in PSAVE mode, Q2 turns off if the inductor current falls to zero. If the FB pin is above the 750mV reference, both Q2 and Q1 remain off, and the output current is supplied by the output capacitor.

V_{OUT} Voltage Selection

The output voltage is regulated by comparing the voltage at the FB pin to the internal 750mV reference voltage, see Figure 2.

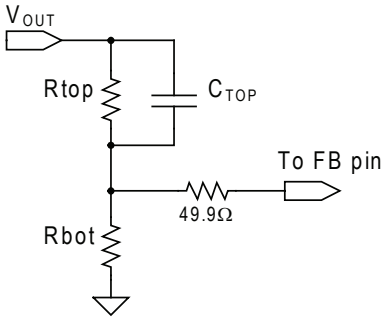


Figure 2 — Output Voltage Selection

Applications Information (continued)

The output voltage is approximated by the following equation:

$$V_{OUT} = 0.75 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

Note that the Adaptive On-time control regulates the valley of the FB ripple voltage, not the DC value. In practice the DC value of FB and V_{OUT} can be slightly higher than the value predicted by DC equations; this is easily corrected by reducing the value of R_{TOP} slightly. For recommended values of the FB components for different VOUTs, see the Table in the Detailed Application Circuit.

Continuous Mode Operation

The SC3203 operates in CCM (Continuous Conduction Mode) when the load current exceeds 50% of the inductor ripple current (Figure 3). In this mode one of the power mosfets is always on, with no intentional dead time other than to avoid cross-conduction. This mode of operation results in typically 500kHz operation.

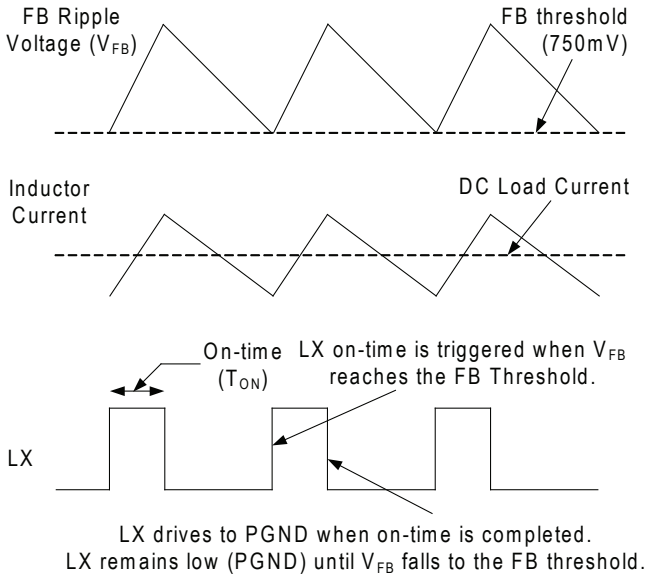


Figure 3 — Continuous Mode Operation

Power-save Operation

At light loads the SC3203 enters power-save mode to improve efficiency. During the low-side on-time, the internal zero-cross comparator monitors inductor current via the LX voltage across the low-side mosfet. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save (PSave) mode.

In PSave mode, after the high-side on-time has completed and the low-side mosfet is on, the low-side is turned off when the inductor current reaches zero. At this time both mosfets remain off until V_{FB} drops to the 750mV threshold. While the mosfets are off, the load is supplied by the output capacitor. Figure 4 shows power-save operation at light loads.

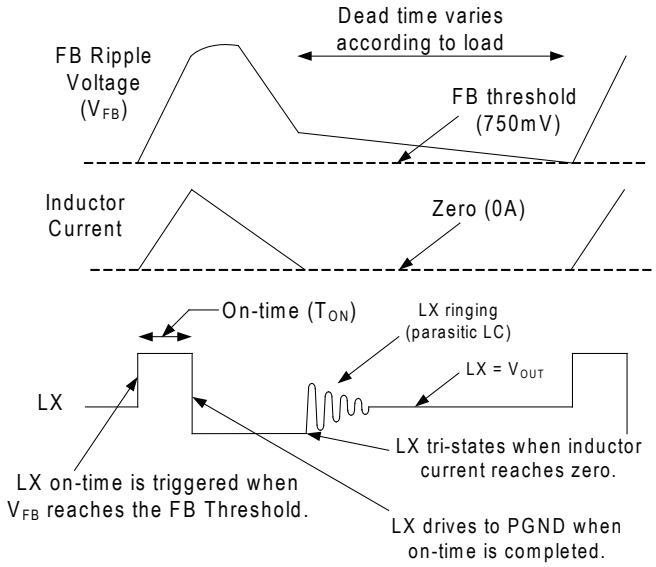


Figure 4 — Power-save Operation

While operating in power-save mode, after each high-side on-time, the low-side turns on for at least the minimum 260nsec off-time. After this, if the inductor current has not reached zero and the FB pin falls below the FB threshold, power-save operation is terminated. The controller immediately generates a high-side on-time and returns to Continuous Mode Operation, resulting in a rapid response to large step load increases.

Applications Information (continued)

Smart Power Save Protection

Loads or circuits which are connected to more than one DC source may leak current from a higher voltage into a lower voltage. If the SC3203 provides the lower voltage and is operating in PSave mode, this leakage can cause V_{OUT} to slowly rise during the dead-time when both mosfets are off. If the leakage is high it can drive V_{OUT} up to the over-voltage threshold, resulting in a shutdown.

Smart power save prevents this condition. When the FB pin exceeds 10% above nominal (exceeds 825mV), the device immediately disables power-save and turns on the low-side mosfet. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 750mV trip point, a normal on-time switching cycle begins. Typically the device will return to normal power-save operation.

This method prevents a hard OVP shutdown and also cycles energy from V_{OUT} back to V_{IN}. Figure 5 shows typical Smart PSave operation.

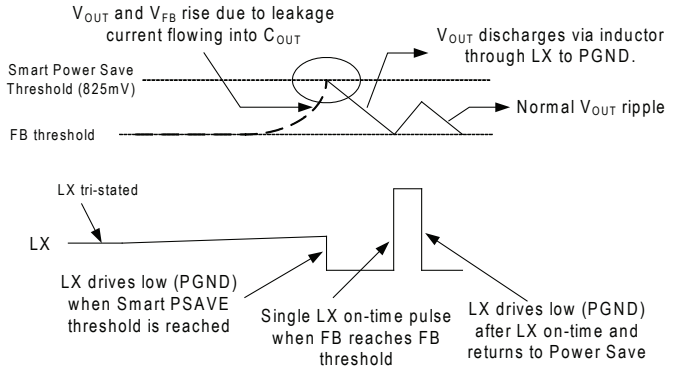


Figure 5 — Smart Power Save

Current Limit Protection

Current limiting is accomplished by sensing the low-side mosfet current. If this mosfet current exceeds the Current Limit value (typically 3.75A), the mosfet is kept on. The controller will not allow another high-side on-time until the current in the low-side mosfet falls to 3.75A. This method controls the inductor valley current as shown by ILIM in Figure 6.

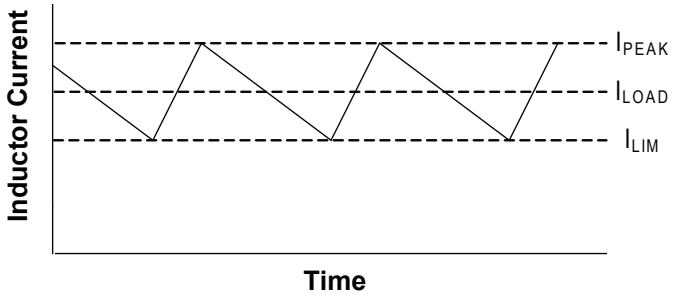


Figure 6 — Valley Current Limit

Enable Input and VIN UVLO

The EN input is used to enable or disable the switching regulator. The EN pin has two thresholds. The first threshold at typically 1V activates the internal LDO. The second threshold at 1.5V turns on the switcher.

The EN input also features a programmable input Under-Voltage Lockout (VIN UVLO). A resistor divider to the EN pin allows the user to select a VIN point at which the switcher will turn off. The EN circuit is shown in Figure 7.

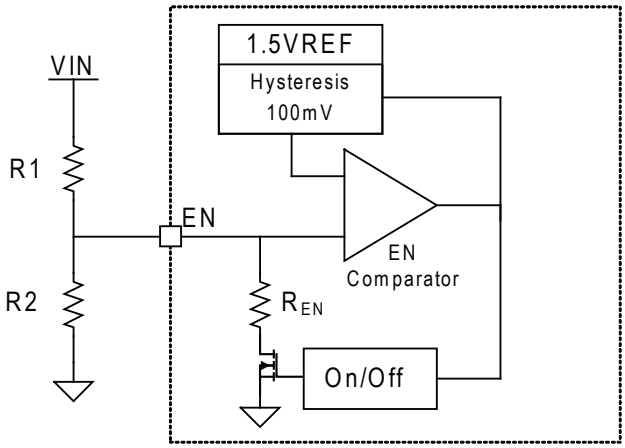


Figure 7 — Enable Input Circuit

Applications Information (continued)

When the EN input is below 1.5V, the switcher is off. mosfet Q1 is on and resistor REN is connected to the EN pin. When the EN pin reaches 1.5V, the comparator output drives high and the switcher is enabled. mosfet Q1 is then switched off, removing R_{EN} from the circuit which immediately raises the voltage at the EN pin and provides VIN hysteresis. An additional hysteresis of 100mV is provided internally at the comparator input.

The equations for selecting the VIN_ON and VIN_OFF thresholds are shown below. Note that R_{EN} has a typical value of 810kΩ and tolerance of +/- 20%.

$$VIN\_ON = (1.5V) \times \left(1 + \frac{R1}{R2} + \frac{R1}{REN}\right)$$

$$VIN\_OFF = (1.4V) \times \left(1 + \frac{R1}{R2}\right)$$

Soft Start of PWM Regulator

Soft start is achieved in the PWM regulator by ramping the internal FB Comparator reference from zero to 750mV. When the ramp voltage reaches 750mV, the ramp is ignored and the FB comparator switches over to a fixed 750mV threshold. During soft start the FB pin follows the internal ramp, which limits the start-up inrush current and provides a controlled soft start profile for a wide range of applications. Typical soft start ramp time is 1.8msec.

During soft start the regulator turns off the low-side mosfet during any cycle if the inductor current falls to zero. This prevents negative inductor current, allowing the device to start into a pre-biased output with negligible drooping on the output.

Power Good Output

The Power Good (PGood) output is an open-drain indicator. The output is open (high impedance) when the output is within normal regulation. During startup the PGood output is held low at AGND while the output ramps up. If the output reaches normal levels, the PGood output will switch to high (open circuit) typically 3.3msec after the EN pin drives high to begin a soft start cycle.

On startup, the FB rising edge threshold for PGood is 750mV -10% (675mV). Once PGood drives high, the FB pin must fall to 750mV -15% (638mV) before the PGood output will drive low.

Output Over-Voltage Protection

OVP (Over-Voltage Protection) becomes active as soon as the switcher is enabled. The OVP threshold is set at 750mV + 20% (900mV). When the FB pin exceeds the 900mV the low-side mosfet turns on. It will remain on while the low-side current is negative (remain on while current flows out of the LX pin). When the low-side current reaches zero or becomes positive (current into the LX pin), the low-side mosfet turns off and the LX pin is tri-stated. LX remains tri-stated until the FB pin falls below the 750mV +15% (863mV), which starts the Hiccup Mode timer and forces a 32msec delay before a new soft start cycle begins.

The PGOOD output also drives low when the FB pin exceeds the OVP threshold.

Output Under-Voltage Protection

When the FB pin falls to 75% of its nominal voltage (falls to 563mV) for eight consecutive clock cycles, the mosfets are turned off and the controller enters Hiccup Mode operation. Under-Voltage faults are normally caused by an output overload; the controller will automatically recover on the next soft start cycle after the overload is removed.

Over-Temperature Protection

If the internal temperature rises to 160°C the device will shut down. The device remains off until the temperature drops to 150°C, which starts the Hiccup Mode timer and forces a 32msec delay before a new soft start cycle begins.

Hiccup Mode (Automatic Fault Recovery)

The SC3203 includes Hiccup Mode fault protection. If the switcher output shuts down due to a fault condition, the device remains off until the fault condition is removed, which begins the 32ms Hiccup Mode timer. After 32msec

Applications Information (continued)

has passed a new soft start cycle is attempted. After soft start, if the output is still in a fault condition the switcher will again shut down and wait another 32msec before attempting the next soft-start. The 32msec delay between soft start cycles reduces power loss and heating in the power components.

Note that an external VIN UVLO event is treated internally as a fault condition and triggers the Hiccup Mode feature. This will lead to a delay on restart when VIN has recovered to a normal level. The EN pin can rise above the VIN UVLO threshold but the controller must complete a 32msec time-out before the switcher will start up. The same delay also occurs for OVP and Over-Temperature shut down.

BYP Regulator

The SC3203 has an internal regulator that supplies the bias voltage for the PWM controller. Although this voltage is available externally, the BYP regulator is designed for internal use only. The BYP pin requires a 1µF bypass capacitor. When the EN pin exceeds typically 1V, the BYP regulator is enabled and goes through a start-up sequence.

During start-up while the BYP output voltage remains below 4V, the BYP short-circuit protection is active and limits the current to typically 35mA. After BYP exceeds 4.0V the LDO operates in voltage regulation mode with output current limited to typically 100mA (see Figure 9).

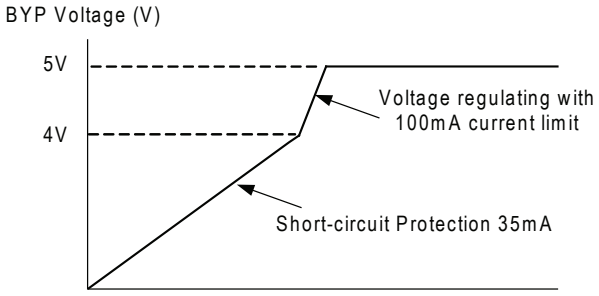


Figure 9 — LDO Start-Up

BYP UVLO and POR

The BYP UVLO (Under-Voltage Lock-Out) circuitry inhibits switching and tri-states the power mosfets until the BYP voltage rises above 4.0V. An internal POR (Power-On Reset) occurs when BYP exceeds 4.0V, which resets the fault latch and enables the soft start ramp. The SC3203 then begins a soft start cycle. The PWM will shut off if BYP falls below 3.7V.

Boost Supply

The Boost supply provides bias for the high-side mosfet driver. Connect a 10nF between Boost and LX. Larger values of Boost capacitance should not be used, the Boost driver circuit is designed for 10nF.

PCB Layout Guidelines

The optimum layout for the SC3203 is shown in Figure 12. This layout shows an integrated mosfet buck regulator with a maximum current of 3A. The total PCB area is approximately 19.1mm x 11.3mm.

- The VIN capacitor should be located immediately next to the VIN and PGND pins, and mounted on the same side of the pcb. Use wide traces or copper areas to connect between the capacitor and the IC pins.
- Place the inductor near the LX pin and route directly to the pin using wide, short traces.
- A 1µF BYP capacitor should be located at and directly connected to the BYP and AGND pins, and mounted on the same side of the pcb.
- A 0.01 µF Boost capacitor should be located at and directly connected to the BST and LX pins, and mounted on the same side of the pcb.
- Using the placement shown below, the power Ground plane can be a solid area that directly connects the ground points for CIN, COUT, the PGND PAD, and AGND pin.
- Connect the AGND pin directly to the PGND pad. For the RBOT connection to ground, route this to the AGND pin while avoiding the high-noise current path between CIN, the PGND PAD, and COUT.
- The FB trace and FB components should not be placed or routed near the high-noise switching nodes (LX, BST, VIN). Do not route FB traces under or near the inductor: magnetic fields from the inductor can induce switching noise into the FB signal and cause erratic operation.

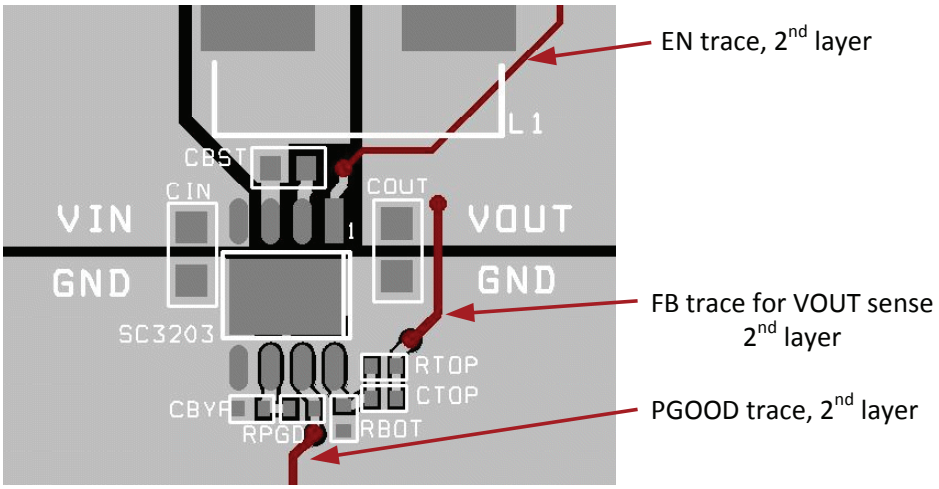
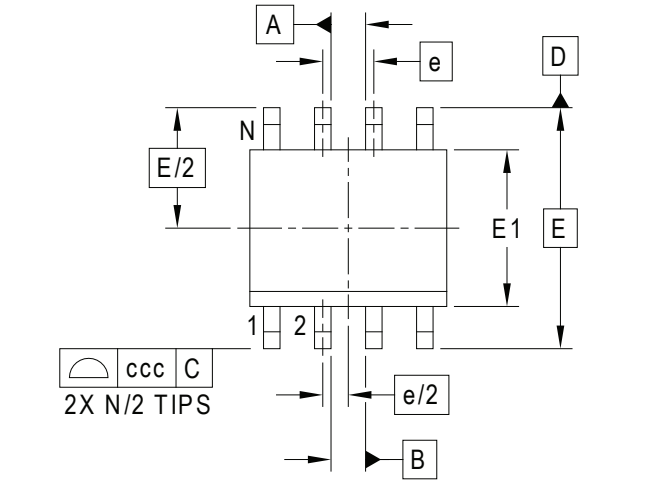
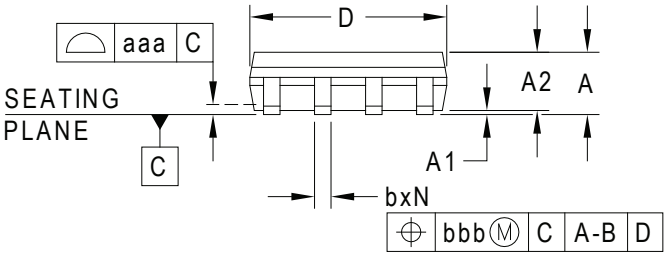


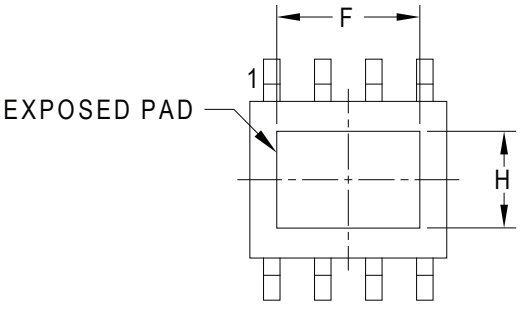
Figure 12 — PCB Layout

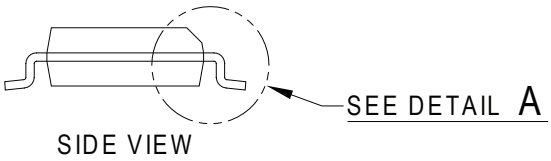
Outline Drawing — SOIC8-EP5

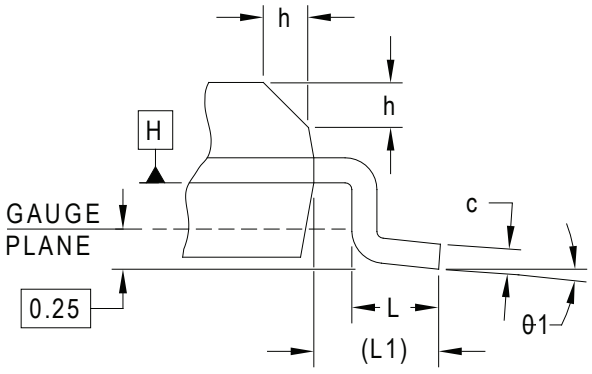




DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.25	-	1.75
A1	0.00	-	0.15
A2	1.25	-	1.65
b	0.31	-	0.51
c	0.17	-	0.25
D	4.80	4.90	5.00
E	6.00 BSC		
E1	3.80	3.90	4.00
e	1.27 BSC		
F	2.95	-	3.85
H	2.15	-	2.70
h	0.25	-	0.50
L	0.40	0.72	1.27
L1	(1.05)		
N	8		
θ1	0°	-	8°
aaa	0.10		
bbb	0.25		
ccc	0.25		





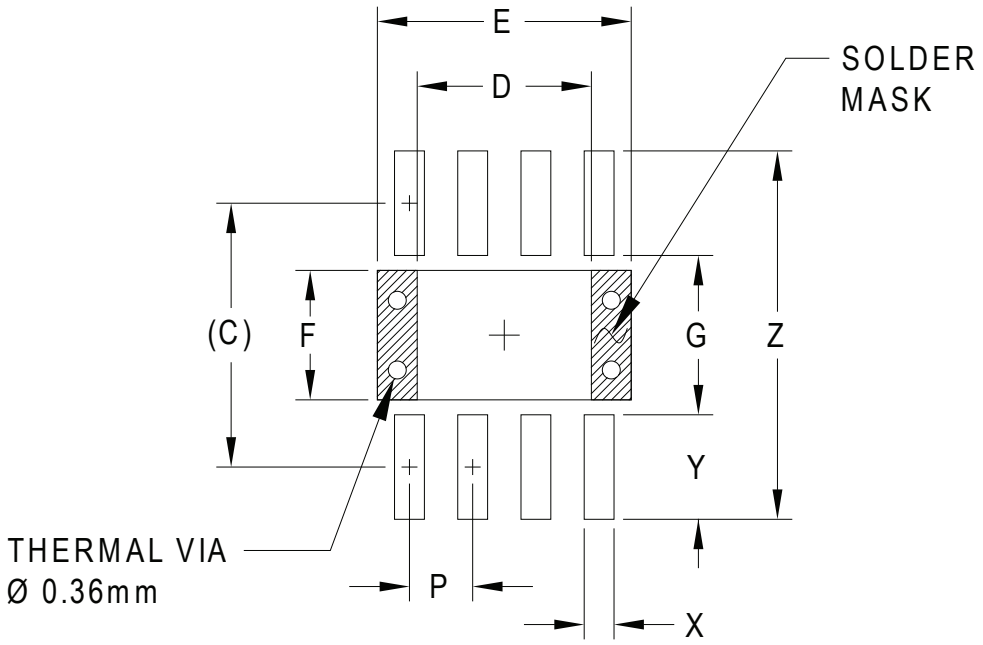


DETAIL A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H- .
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE MEASUREMENT OF DIMENSION "F" DOES NOT INCLUDE EXPOSED TIE BAR.

Land Pattern — SOIC8-EP5



DIMENSIONS	
DIM	MILLIMETERS
C	(5.30)
D	3.50
E	5.10
F	2.60
G	3.20
P	1.27
X	0.60
Y	2.10
Z	7.40

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSE ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. REFERENCE IPC-SM-782A, SECTION 9.1, RLP NO. 300A.

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