SC493

EcoSpeed™ Step-down Controller with I²C Interface

Features

- Input supply voltage range — 3.0V to 28V
- Controller supply voltage range — 3.0V to 5.5V
- All ceramic solution enabled
- I²C interface
- Output voltage fine adjust control
- Output voltage margining
- Supports dynamic voltage transitions via the I²C interface
- Programmable power-on delay time and soft-start time
- EcoSpeed™ architecture with pseudo fixed-frequency adaptive on-time control
- Switching frequency programmable up to 1MHz
- Selectable power save, including ultrasonic
- Non-synchronous start-up into pre-biased loads
- Over-voltage/under-voltage fault protection
- Smart power save
- Power good Output
- Smart drive™
- Status register monitoring device operation
- Ultra-thin package — 3 x 3 x 0.6 (mm), 20 pin MLPQ-UT
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Printers
- Computer peripherals

Description

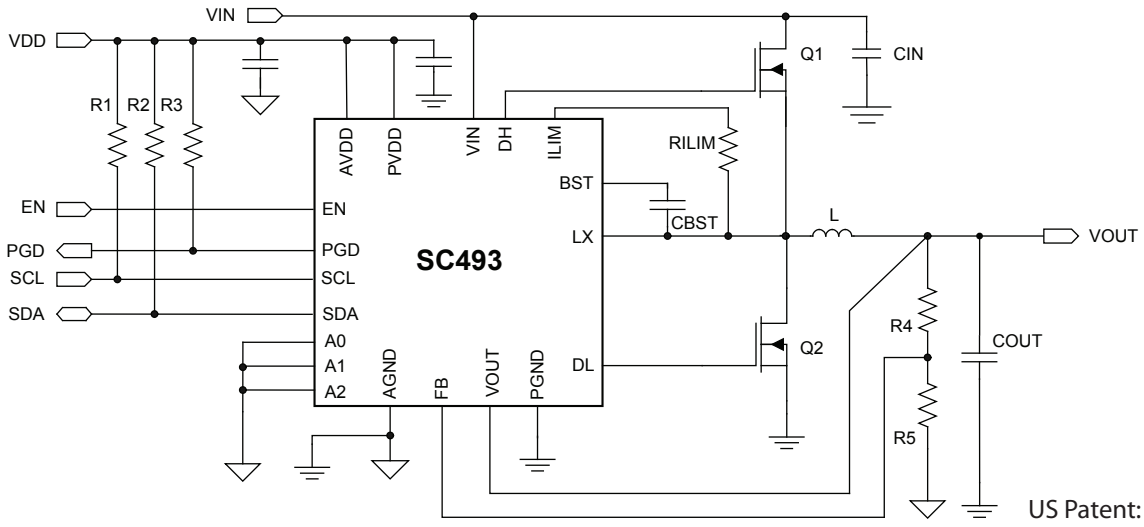
The SC493 is a synchronous EcoSpeed™ buck power supply controller. It features an I²C interface and a bootstrap switch in a space-saving MLPQ 3X3-20 pin package. The SC493 uses Semtech's advanced patented adaptive on-time control architecture to provide excellent light load efficiency and fast transient response with small external components.

The I²C interface is used to program the output voltage offset, the power-on delay time, the soft-start time, the power save operating mode, and it can enable/disable the controller. Additionally, a status register provides information on device state and faults.

The controller is capable of operating with all ceramic solutions and switching frequencies up to 1MHz. The programmable frequency and selectable power save mode offer the flexibility to optimize the controller for high efficiency and small size. The power save mode can be enabled to maximize efficiency over the entire load range (PSAVE), or switched to ultrasonic mode to set the minimum frequency to the desired value (UPSAVE). Power save mode can be disabled for operation in continuous conduction mode at all loads.

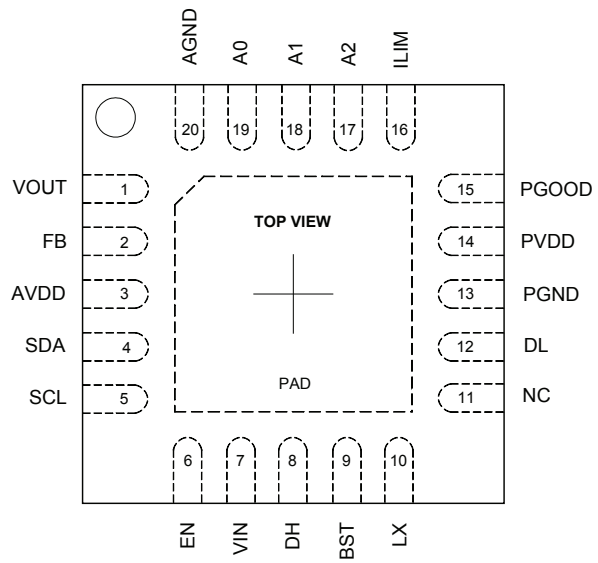
Additional features include output voltage margining, cycle-by-cycle current limit, output voltage soft-start, over and under-voltage protection, controller over-temperature protection, and output voltage soft-shutdown when disabled. The SC493 also provides a power good output.

Typical Application Circuit



US Patent: 7,714,547 B2

Pin Configuration



MLPQ-UT-20 3X3, 20 LEAD

θ_{JA}=40°C/W

Ordering Information

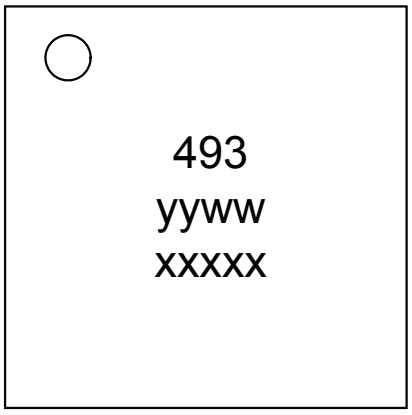
Device	Package
SC493ULTRT(1)(2)	MLPQ-UT-20 3X3
SC493EVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Lead-free packaging only. Device is WEEE and RoHS compliant, and halogen-free.

Marking Information



yyww = Date Code

xxxxx = Semtech Lot No.

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Absolute Maximum Ratings

BST to LX (V) ..... -0.3 to +6.0
BST to PGND (V) ..... -0.3 to +35
LX to PGND (V) ..... -0.3 to +30
PVDD to PGND (V) ..... -0.3 to +6.0
VIN to PGND (V)..... -0.3 to +30
AVDD to AGND (V) ..... -0.3 to +6.0
AGND to PGND (V)..... -0.3 to +0.3
All other pins to AGND (V)..... -0.3 to AVDD +0.3
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Ambient Temperature (°C)..... -40 to +85
Input Voltage VIN (V)..... 3.0 to 28
Controller Supply Voltage AVDD, PVDD (V)..... 3.0 to 5.5
Output Voltage (V)..... 0.5 to 5.0

Thermal Information

Storage Temperature (°C)..... -65 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal Resistance, Junction to Ambient[2] (°C/W) 40
Peak IR Reflow Temperature (10s to 30s) (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:

(1) Tested according to JEDEC standard JESD22-A114-B.

(2) Calculated from package in still air, mounted to 3 x 4.5(in.) 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Test Condition (unless otherwise noted): V_{VDD}[1]=5V, V_{IN}=5V, $T_{J(MAX)}$ = 125°C. Typ. values at 25°C, Min. and Max. at -40°C < T_A < 85°C, V_{FBadj} = 0%.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
VDD[1] Input Voltage	VDD		3.0		5.5	V
VDD[1] UVLO Threshold	VDD_{UVLO}	VDD rising		2.8		V
VDD[1] UVLO Hysteresis	VDD_{UVLO_HYS}			0.2		V
VDD[1] Supply Current	I_{VDD}	Shut down, EN pin = 0V		0.1	2	µA
		I²C Standby, controller disabled		150		µA
		No switching, PSAVE, FB>0.5V		1000		µA
		f_{sw} = 25kHz, UPSAVE		2		mA
		Operating f_{sw}= 250kHz, no load		10		mA
Switch-mode Controller						
FB On-Time Threshold	V_{VFB_TON}	Static VIN and Load, no offset via I²C	0.496	0.5	0.504	V
On-Time Accuracy	t_{ON}	Deviation from the ideal on-time to meet the set switching frequency	-10		10	%
Minimum On Time	t_{ON_MIN}			100		ns
Minimum Off Time	t_{OFF_MIN}			250		ns

Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Startup						
Initialization Time [2]	t_{INIT}	Delay before the I^2C bus and the Power-on delay ramp are enabled			1	ms
Soft-Start Time Accuracy	t_{SS}		-20		+20	%
Power-on Delay Time Accuracy	t_{DLY}		-20		+20	%
Powersave						
Zero-Crossing Detector Threshold	VT_{ZC}	V_{LX} - PGND	-3	0	+3	mV
UPSV mode Frequency	f_{UPSV}	UPSV enabled, UPSV1 = 1, UPSV0 = 1	20	25	30	kHz
Power Good						
PGD Rising Threshold	VT_{PGD_RISE}	FB with respect to set point, under voltage, and over voltage		90/120		%
PGD Falling Threshold	VT_{PGD_FALL}	FB with respect to set point, under voltage, and over voltage		80/110		%
PGD Leakage	$ILEAK_{PGD}$	Device operating, no fault, V_{PGD}=V_{VDD} [1]			1	µA
PGD Output Low Voltage	V_{PGD_LOW}	I_{PGD}=3mA			0.4	V
Fault Protection						
I_{LIM} Source Current	I_{LIM}		9	10	11	µA
I_{LIM} Temperature Coefficient	TC_{ILIM}			3000		ppm
I_{LIM} Comparator Offset	$VOFF_{ILIM}$		-10	0	+10	mV
Output Under-Voltage Fault	VT_{UV}	FB with respect to set point, 8 consecutive switching cycles		70		%
Output Over-Voltage Fault	VT_{OV}	FB with respect to set point rising/ falling		120		%
Over-Voltage Fault Delay[2]	t_{DLY_OV}			5		µs
Smart Power-save Protection Threshold[2]	$VT_{SMRTPSV}$	FB with respect to set point rising		110		%
Over-Temperature Shutdown	T_{OT}	Rising T_J		160		°C
Over-Temperature Hysteresis	T_{OT_HYS}			10		°C
Analog Inputs and Outputs						
V_{OUT} Input Resistance	R_{VOUT}	Controller enabled		500k		Ω
		Controller disabled/internal load enabled		10		

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Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Digital Input Electrical Specifications (A0, A1, A2, EN)						
Input High Threshold	V_{IH}	V_{VDD}(1) = 5.5V	1.6			V
Input Low Threshold	V_{IL}	V_{VDD}(1) = 3.0V			0.4	V
Input High Current	I_{IH}	V_{VDD}(1) = 5.5V	-1		+1	µA
Input Low Current	I_{IL}	V_{VDD}(1) = 5.5V	-1		+1	µA
I²C Interface Interface complies with slave mode I²C interface as described by Philips I²C specifications version 2.1 dated January, 2000						
Digital Input Voltage Low	V_{B-IL}				0.4	V
Digital Input Voltage High	V_{B-IH}		1.6			V
SDA Output Low Level	V_{SDA_LOW}	I_{DN}(SDA) ≤ 3mA			0.4	V
Digital Input Current	I_{B-IN}		-0.2		+0.2	µA
Hysteresis of Schmitt Trigger Inputs	V_{HYS}			0.1		V
Maximum Glitch Pulse Rejection	t_{SP}			50		ns
I/O Pin Capacitance	C_{IN}			10		pF
I²C Timing						
Clock Frequency	f_{SCL}			400	440	kHz
SCL Low Period (2)	t_{LOW}		1300			ns
SCL High Period (2)	t_{HIGH}		600			ns
Data Hold Time (2)	t_{HD_DAT}		0			ns
Data Setup Time (2)	t_{SU_DAT}		100			ns
Setup Time for Repeated START Condition (2)	t_{SU_STA}		600			ns
Hold Time for Repeated START Condition (2)	t_{HD_STA}		600			ns
Setup Time for STOP Condition (2)	t_{SU_STO}		600			ns
Bus-Free Time Between STOP and START (2)	t_{BUF}		1300			ns

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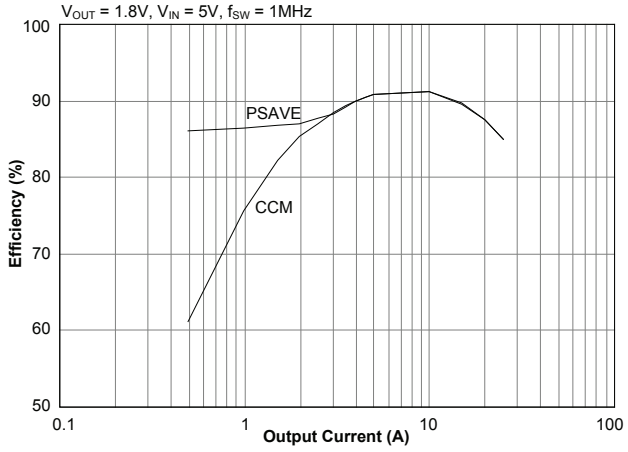
Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Gate Drivers						
Shoot-Through Protection Delay(2)	t_{PROT}	DH or DL Rising		30		ns
DL Pull-Down Resistance	R_{DL_DOWN}	DL Low		0.3	0.6	Ω
DL Sink Current	I_{DL_SINK}	V_{DL} = 2.5V		8.3		A
DL Pull-Up Resistance	R_{DL_UP}	DL High		1	2	Ω
DL Source Current	I_{DL_SOURCE}	V_{DL} = 2.5V		2.5		A
DH Pull-Down Resistance	R_{DH_DOWN}	DH Low, BST-LX = 5V		0.6	1.2	Ω
DH Sink Current	I_{DH_SINK}	V_{DH-LX} = 2.5V		4.2		A
DH Pull-Up Resistance	R_{DH_UP}	DH High, BST-LX = 5V		1	2	Ω
DH Source Current	I_{DH_SOURCE}	V_{DH-LX} = 2.5V		2.5		A

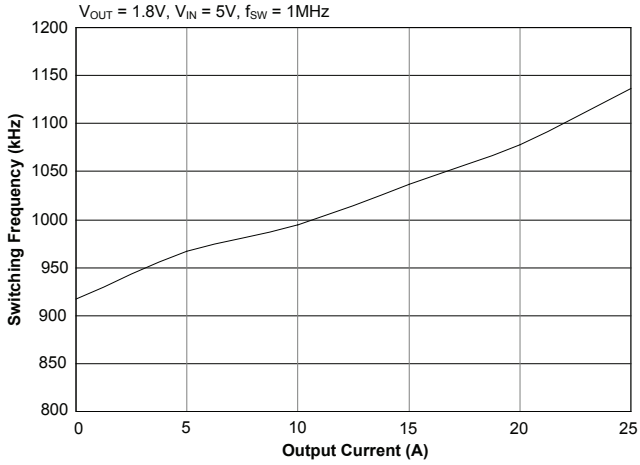
Note:
(1) VDD refers to both AVDD and PVDD
(2) Guaranteed by design.

Typical Characteristics

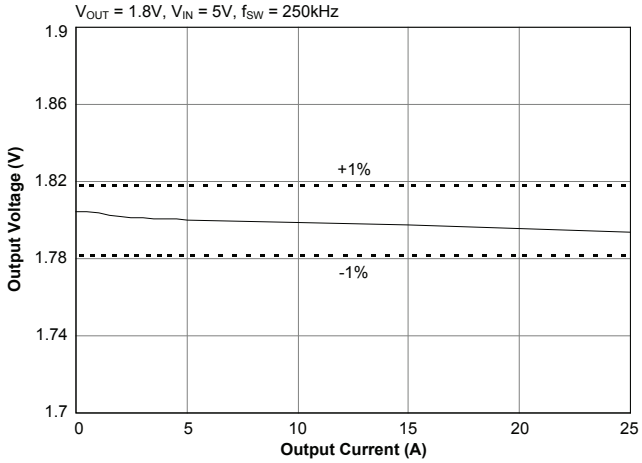
Efficiency vs Load — CCM and PSAVE



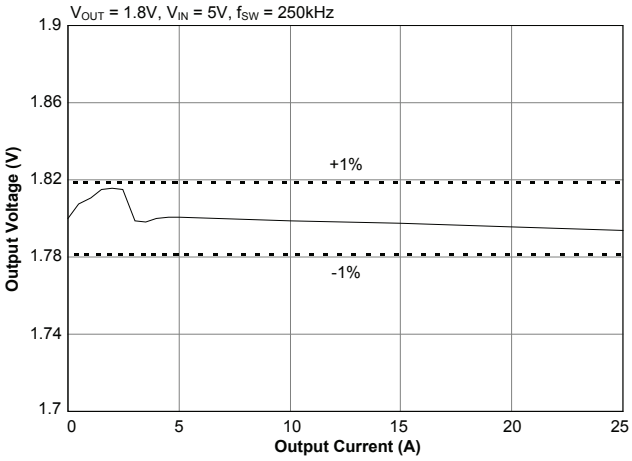
Switching Frequency vs. Load — CCM



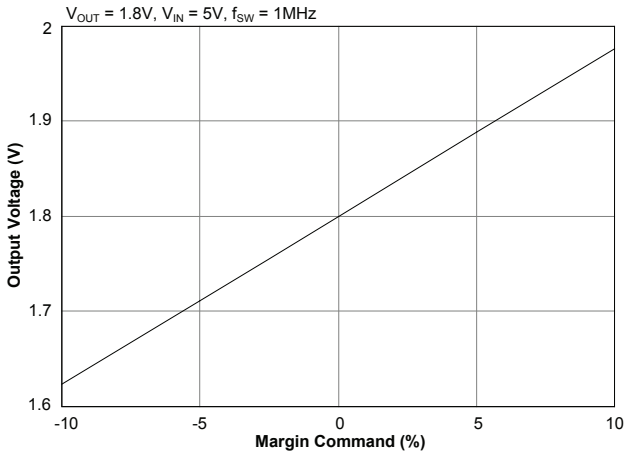
Load Regulation — CCM



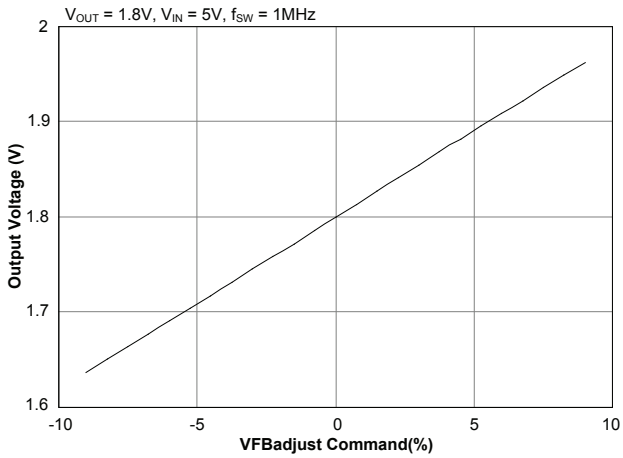
Load Regulation — PSAVE



Output Voltage vs. Margin — CCM



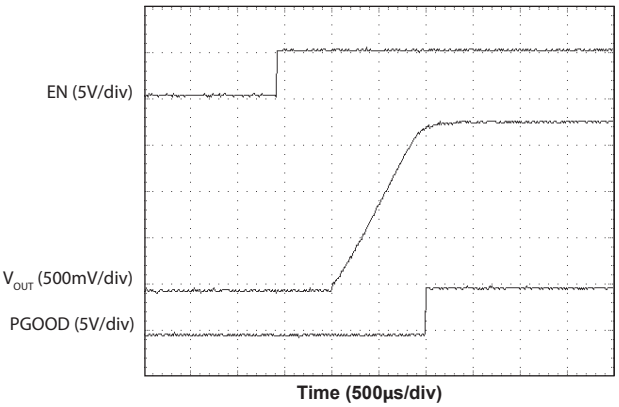
Output Voltage vs. VFBadj — CCM



Typical Characteristics (continued)

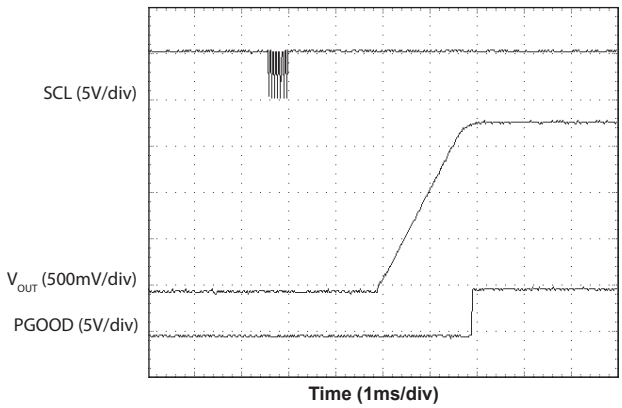
Soft Start — EN Pin

V_{IN} = 5V, V_{OUT} = 1.8V, Soft Start = 1ms, Power-on Delay = 0ms



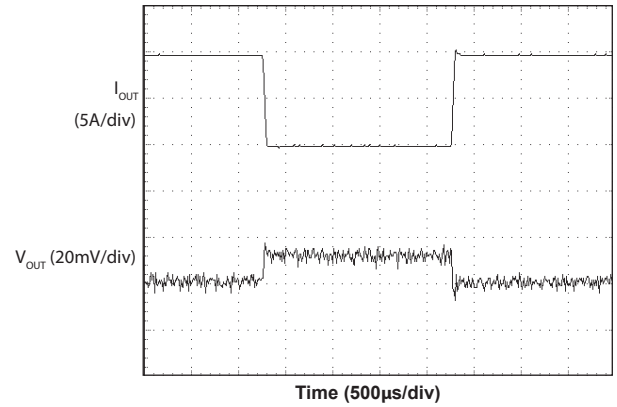
Soft Start — I²C

V_{IN} = 5V, V_{OUT} = 1.8V, Soft Start = 2ms, Power-on Delay = 2ms



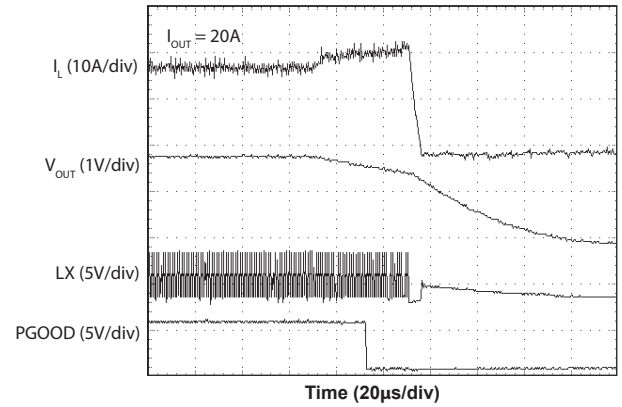
Load Transient Response

V_{IN} = 5V, V_{OUT} = 1.2V, f_{SW} = 1MHz, L = 0.2µH, C = 220µF



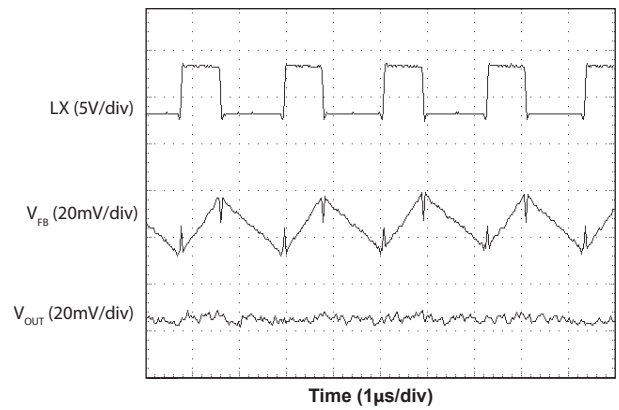
Output Over Current Response — Normal Operation

V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 1MHz, L = 0.2µH, C = 1000µF



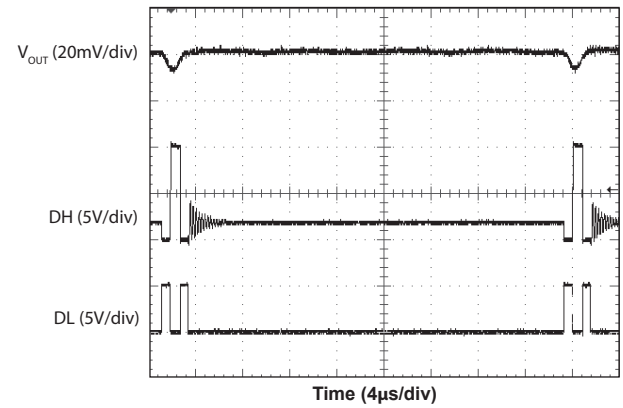
Switching — Forced Continuous Mode

V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 1MHz, Load = 3A



Switching — Ultrasonic PSAVE Mode

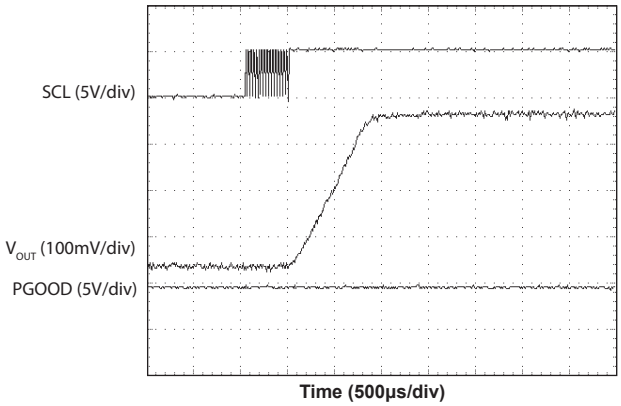
V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 500kHz, No load



Typical Characteristics (continued)

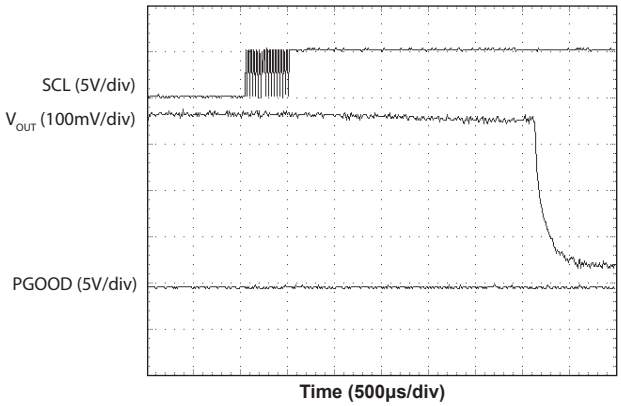
Slew-Up — CCM, No Load, EnIntLd=0/1

V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 1MHz, VFBadj command change -9% to +9%



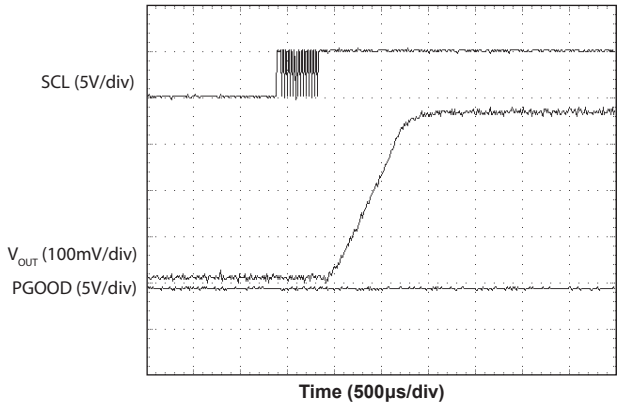
Slew-Down — CCM, No Load, EnIntLd=0

V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 1MHz, VFBadj command change +9% to -9%



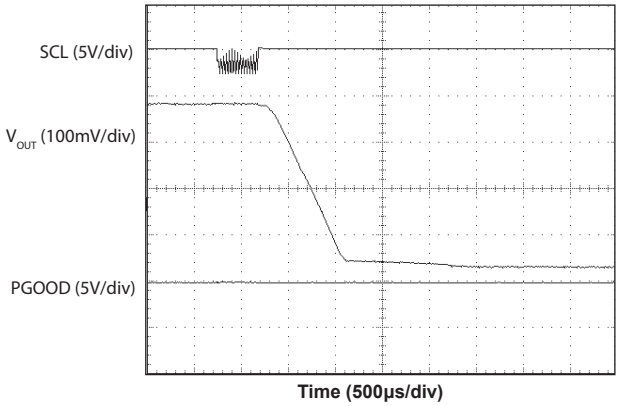
Slew-Up — CCM, No Load, EnIntLd=0/1

V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 1MHz, Margin command change -10% to +10%



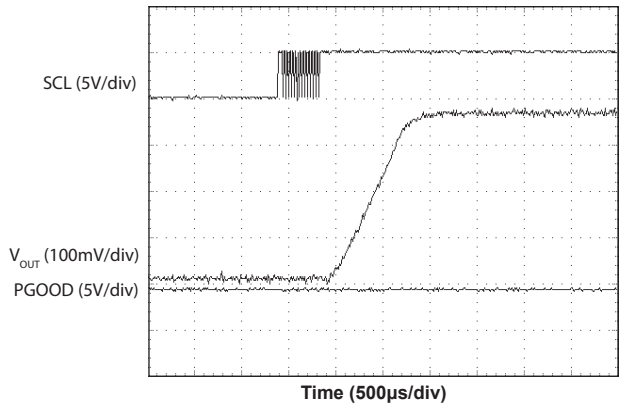
Slew-Down — CCM, No Load, EnIntLd=1

V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 1MHz, Margin command change +10% to -10%



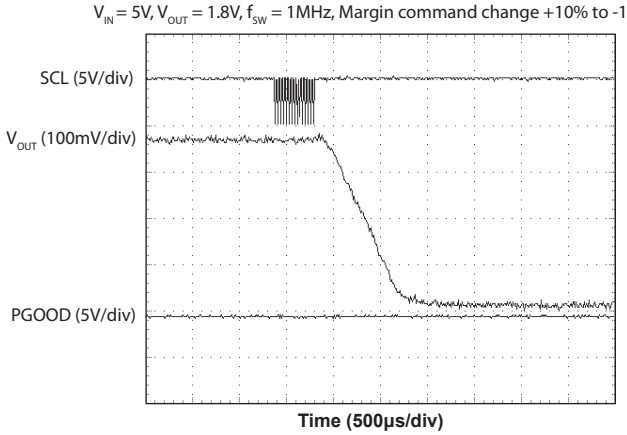
Slew-Up — CCM, 3A Load, EnIntLd=0/1

V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 1MHz, Margin command change -10% to +10%



Slew-Down — CCM, 3A Load, EnIntLd=0/1

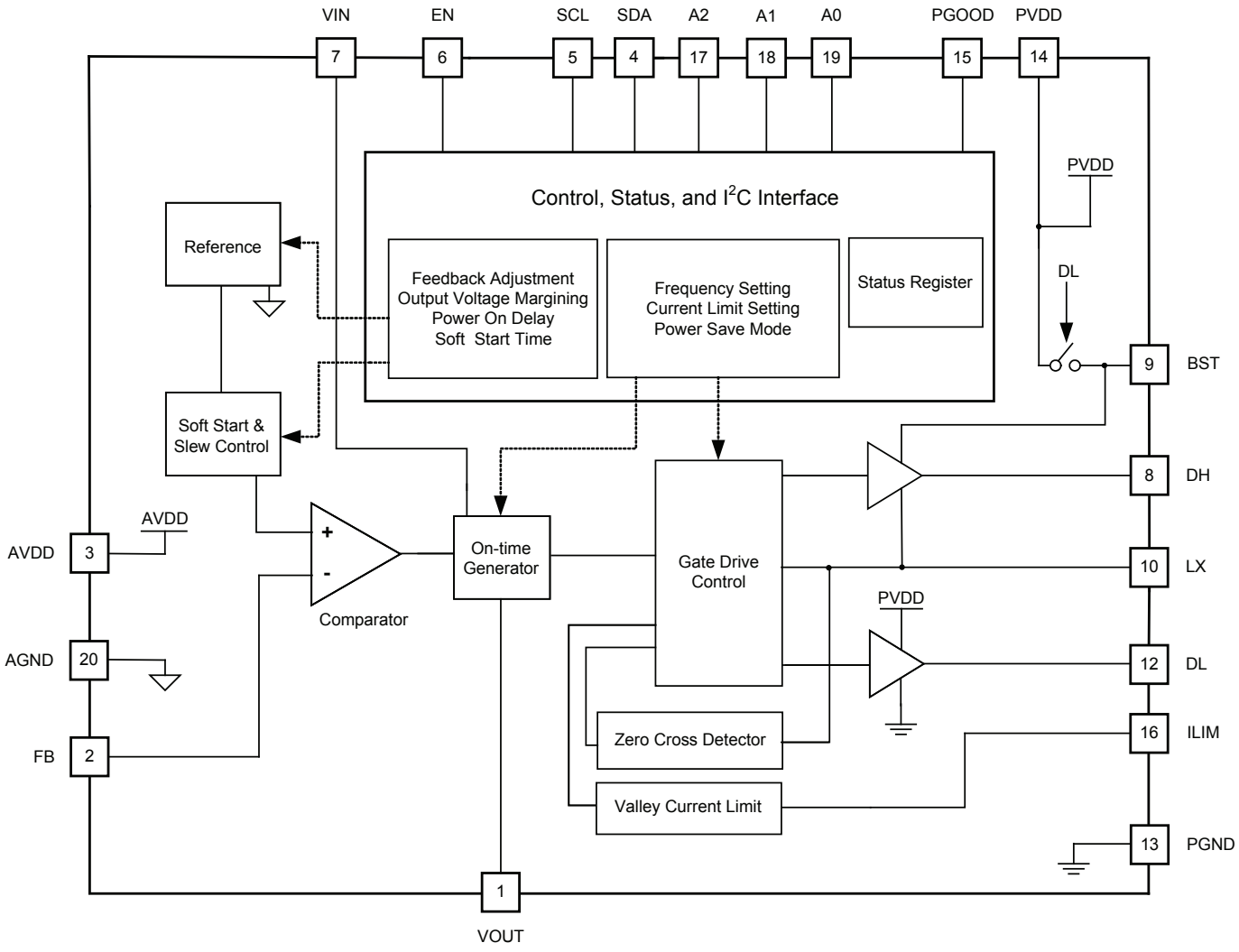
V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 1MHz, Margin command change +10% to -10%



Pin Descriptions

Pin #	Pin Name	Pin Function
1	VOUT	Output voltage
2	FB	Feedback pin
3	AVDD	Chip supply voltage
4	SDA	I^2C data input/output
5	SCL	I^2C clock input
6	EN	Enable pin
7	VIN	Power stage input voltage
8	DH	High side gate driver pin
9	BST	Bootstrap pin — a capacitor is connected from BST to LX to develop the bias voltage for the high side gate drive.
10	LX	Switching (phase) node — connect to the switching side of the power inductor.
11	NC	No Connect
12	DL	Low side gate driver pin
13	PGND	Power ground
14	PVDD	Supply voltage for driver
15	PGOOD	Power good
16	ILIM	Current limit sense point — to program the current limit connect a resistor from ILIM to LX
17	A2	Input for bit 2 of the I^2C device address
18	A1	Input for bit 1 of the I^2C device address
19	A0	Input for bit 0 of the I^2C device address
20	AGND	Analog ground
	PAD	Thermal pad for heat sinking purposes — connect to ground plane using multiple vias — not connected internally.

Block Diagram



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Applications Information

General Description

The SC493 is a step down synchronous buck DC-DC controller optimized for use in 3.3V/5V input small form-factor applications. It has the following key features:

- I²C control over output voltage offset, margining, power-on delay, switching frequency, soft-start duration, and power save mode.
- Integrated bootstrap switch
- Programmable switching frequency from 250kHz to 1MHz to optimize board space and efficiency.
- Protection features — over-current, over-voltage, under-voltage, and over-temperature
- Power save operation — low quiescent current and ultrasonic power save
- Status and flag bits for diagnosis and protection purposes
- Supports 25A operation

I²C Compatible Interface Functions

The I²C interface can be used to read & write the following functions:

- Shutdown/Start-up of output
- Power-on delay and soft-start duration
- Output voltage offset and margining
- Power save mode
- Switching frequency

Additionally, the I²C interface can be used to read status and flag bits for the following functions:

- Under voltage
- Over voltage
- Over temperature
- Current limit
- Brown out
- Did not start
- Discontinuous mode
- Power good

Status and Flag Bits

The status and flag bits are used to indicate the status of the converter. The status bits always indicate the current state of the converter — the status bit becomes high when the specified condition happens and turns low when the specified condition disappears. The flag bits also become high when the specified condition happens, but will not turn low when the specified condition disappears. For the above mentioned status and flag bits, only discontinuous mode and power good are status bits, the rest of them are all flag bits. The flag bits remain set until one of the following events occurs:

- The input voltage is cycled
- EN pin is cycled
- CLF bit is set

Enable/Disable

The converter is enabled by applying power to VDD (VDD when used refers to AVDD and PVDD together) and VIN, and pulling the EN pin high. The output voltage will rise to the voltage programmed by the FB pin and the external FB network. Pulling the EN pin low turns the converter off and clears all flag bits. The converter can also be turned on/off via the I²C interface. When the EN pin is high, setting the ENSW bit low will turn off the converter, but the flag bits will not be cleared. Setting the ENSW bit back high will turn on the converter again.

Diagnosis and Protection Features

When the device detects fault conditions, the SC493 sets the flag bits indicating what fault conditions have occurred. In addition, depending upon what kind of faults have been detected, the SC493 will provide appropriate actions to safeguard the device from catastrophic failures. The following paragraphs describe how these fault conditions are handled by the SC493.

Did Not Start Indication

If the FB voltage does not rise to 90% of nominal voltage after the converter is enabled, the soft-start duration has passed, and the power good delay has elapsed, the Did Not Start (DNS) flag bit is set. Note that the converter does not latch off just because this bit is set.

Output Over Voltage Protection

When the FB pin voltage exceeds 120% of the nominal voltage, DL goes high, forcing the low-side MOSFET on, and the OVO flag bit is set. The low side MOSFET stays on (and the high side MOSFET remains off) until the output voltage comes back into regulation. However, the CLF bit will successfully clear the OVO flag as soon as the FB falls below 120% of the normal voltage. The converter does not

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Applications Information (continued)

latch off just because this bit is set. The PGD output is driven low when the FB pin is above 120% of the nominal voltage and returns to high when the FB pin is below 110% of the nominal voltage.

Output Over Current Protection

The SC493 features adjustable current limit capability. The $R_{DS(ON)}$ of the external low side MOSFET is used as the current sensing element. The over current limit is set by R_{ILIM} (connected externally). Internally there is a 10µA current source that feeds the ILIM pin when the low side MOSFET has turned on. This current flows through the R_{ILIM} resistor and creates a voltage drop across it. When the low side MOSFET turns on, the inductor current flowing through it creats a voltage across the MOSFET due to its $R_{DS(ON)}$. If this voltage drop exceeds the voltage across the R_{ILIM} resistor, current limit will activate. This prevents the high side MOSFET from turning on until the voltage drop across the low side MOSFET falls below the voltage across the R_{ILIM} resistor. This effectively sets a valley current limit of R_{ILIM} x 10µA/$R_{DS(ON)}$. Please note that $R_{DS(ON)}$ of the MOSFET is dependent on the V_{GS} voltage (equals to PVDD applied to SC493). The ILIM flag bit is set whenever current limit occurs. The converter does not latch off just because this bit is set.

Output Under Voltage Protection

The output under voltage condition occurs with or without current limit. The output under voltage without current limit is normally a result of low input voltage. The controller will look at the inductor current to differentiate these two situations and respond accordingly. After PGD is asserted, if the FB voltage falls below the PGD falling threshold (80%) and current limit does not happen simultaneously, the Brown Out (BO) flag bit is set. This indicates an output under voltage has happened because of low input voltage. The converter does not latch off just because the BO bit is set. After PGD is asserted, if FB voltage falls below 70% of the nominal voltage for 8 consecutive current limited switching cycles, the UVO flag bit is set. This latches the converter off, with both the high side and low side MOSFETs turned off.

To restart, either the EN pin or ENSW register bit must be set low and then back to high.

Over Temperature Protection

When the temperature of the device reaches the over temperature rising threshold, the OT flag bit is set, turning off both high side and low side MOSFETs. After the temperature of the device drops to the over temperature falling threshold, the converter restarts as if the device has been enabled. The converter will go through power-on delay and soft start.

Synchronous Buck Converter Operation, Benefits, and Features

The SC493 employs pseudo-fixed frequency adaptive on-time control. This control method allows fast transient response thereby lowering the size of the power components needed in the system.

The on time is determined by an internal one-shot with a period proportional to the output voltage and inversely proportional to the input voltage. The output ripple voltage generated by the ESR of the output capacitance is used as the PWM ramp signal. This ripple voltage determines the off time for the controller.

For the SC493 the operating frequency range is from 250kHz to 1MHz , programmable via the I^2C interface.

Adaptive on-time control has significant advantages over traditional control methods. Some of the advantages of the adaptive on-time control are:

- No error amplifier, which reduces external components used for compensation
- Predictable frequency spread because of adaptive on-time architecture
- Fast transient response — operation with minimum output capacitance
- Overall superior performance compared to fixed frequency architectures

On-Time One-Shot Generator (TON)

Adaptive on-time controllers like the SC493 have an internal on-time one-shot generator. The one-shot timer uses an internal comparator and a capacitor. The positive input of the comparator is a voltage proportional to the output voltage and the negative input is connected to the capacitor charged by a current proportional to the input voltage. The TON time is the time required to charge this

Applications Information (continued)

capacitor from 0V to the voltage at the positive input. This makes the on-time proportional to the output voltage and inversely proportional to the input voltage, providing a near-constant switching frequency when the input and output voltage vary. A second comparator compares the voltage at the feedback pin to a fixed internal reference voltage to determine when to turn on the high side MOSFET.

Power-on Delay Programming

The power-on delay is programmable via the I²C interface. The power-on delay is defined as the time from when the ENSW bit is set to when the PWM control is enabled and the part begins switching. At the end of the power-on delay time, the PWM control circuit is enabled in a phased manner to ensure proper operation. The phased enabling of internal circuitry adds up to 48µs to the power-on delay time. On start-up (controller enabled by applying power and driving the EN pin high). The controller can take up to 1ms for internal initialization following which the power-on delay is applied.

Soft-Start Operation and Programming

Soft-start is achieved in the PWM controller by using an internal voltage ramp as the reference for the FB Comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 500mV in ~ 2mV increments, using an internal oscillator. When the ramp voltage reaches 500mV, the ramp is ignored and the FB comparator switches over to a fixed 500mV threshold. During soft-start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled soft-start profile for a wide range of applications. Soft-start programmability is achieved by changing the frequency of the oscillator. The soft-start ramp reaches 500mV in 90% of the programmed soft-start time. The remaining 10% of the programmed soft-start time is used to allow the system to stabilize before enabling the PGOOD comparator to drive the PGOOD pin high.

During soft-start the controller turns off the low-side MOSFET on any cycle if the inductor current falls to zero. This prevents negative inductor current, allowing the device to start into a pre-biased output.

Frequency Programming

The nominal switching frequency in continuous conduction mode is programmable via the I²C interface. The switching frequency is changed to the programmed value by scaling the on time as needed.

Power Save Mode Programming

The SC493 provides selectable power-save operation at light loads. When register bits PSV1,0 are set to 01 or 10 the power save mode is enabled. With power save enabled, the zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET. If the inductor current falls to zero for 8 consecutive cycles then the controller enters power save and turns off the low-side FET on each subsequent cycle as long as the current crosses zero. If the inductor current does not reach zero for 8 consecutive switching cycles the controller immediately exits power save. The controller counts zero crossings and therefore the converter can sink current as long as the current does not cross zero on 8 consecutive consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps.

The SC493 can also be operated in forced Continuous Conduction Mode (CCM) by setting PSV1,0 = 00 or 11. With these settings the device will not enter PSAVE and operates at programmed frequency even at light loads. This feature provides user flexibility for system design. Figure 1 shows operation under power save and continuous conduction mode at light loads.

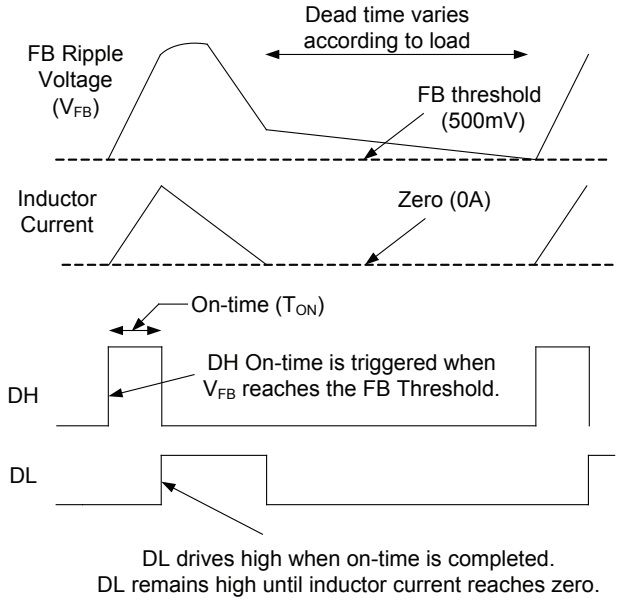


Figure 1 — Power-save Operation

Applications Information (continued)

Ultrasonic Power-save

When ultrasonic PSAVE is enabled (PSV1,0 =10) the minimum operating frequency in power save for the SC493 is set by UPSV1,0 bits . This is accomplished by using a built-in timer that detects the time between consecutive high-side gate pulses.

As soon as the time exceeds the the programmed upper limit, the bottom gate is turned on. This prevents the controller from going below the set limit in frequency when the power save is enabled. Figure 2 shows ultrasonic power-save operation.

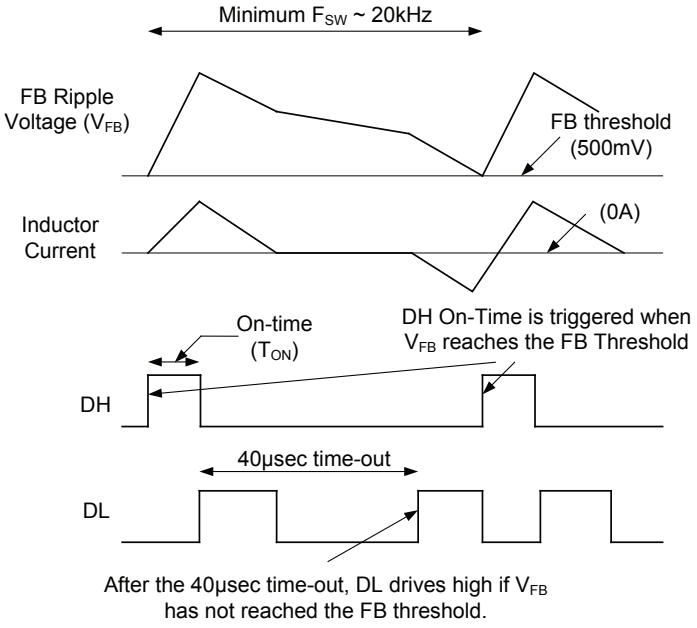


Figure 2 — Ultrasonic Power-save (UPSV 1,0 = 11)

Power Good Output

The Power Good (PGD) output is an open-drain output which requires a pull-up resistor. When the FB voltage falls lower than 80% (typical) of the nominal voltage, PGD is pulled low. It is held low until the FB voltage rises above 90% (typical) of the nominal voltage. PGD is held low during start-up and will not be allowed to transition high until soft-start is completed. PGD also transitions low if the FB voltage rises above 120% (typical) of the nominal voltage, it is held low until the FB voltage drops below 110% (typical) of the nominal voltage.

UVLO and POR

Under-Voltage Lockout (UVLO) circuitry inhibits switching and tri-states the output until VDD rises above 2.8V. An internal Power-On Reset (POR) occurs until VDD exceeds 2.8V, which resets the internal registers, enables the I^2C interface, and resets the soft-start circuitry.

Smart Power-save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold. Smart power-save prevents this condition. When the FB voltage exceeds 10% above nominal (exceeds 550mV), the device immediately disables power-save, and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 500mV trip point, a normal T_{ON} switching cycle begins. This method prevents an OVP fault and also cycles energy from V_{OUT} back to V_{IN}. The device will return to power-save operation on the next switching cycle if the load remains light. Smart Power-Save allows the user to minimize operating power by allowing the use of power save mode in load conditions that would normally require the use of forced continuous conduction mode. Figure 3 shows typical waveforms for the Smart Power-save feature.

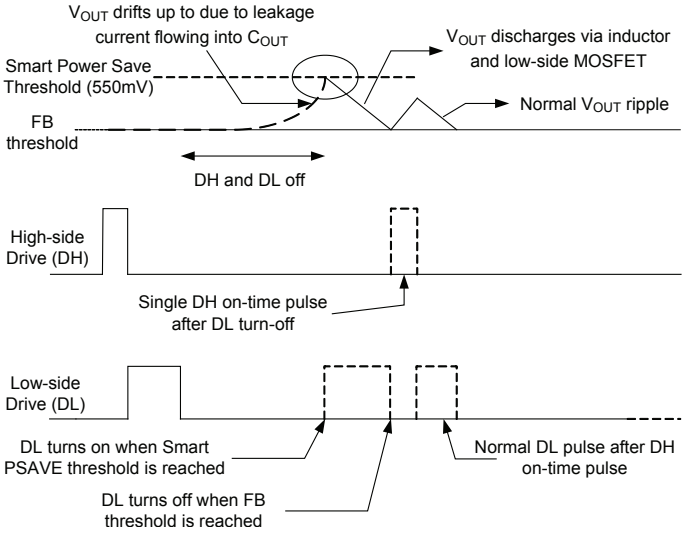


Figure 3 — Smart Power-save

Applications Information (continued)

Dynamic Output Voltage Control

SC493 allows changing the output voltage when the part is already switching. Whenever the output voltage is changed via margining or by fine adjust, the controller changes the internal reference by small intermediate steps using 32us per step. This ensures that the output keeps up with internal slewing and excessive current does not build up in the inductor. The faults are blanked till the end of the slewing. Blanking is released when 8 switching cycles occur after the end of internal slewing since the switching cycles indicate that the part is in regulation. The part is enabled to operate in DCM mode to prevent negative current build up in the inductor when slewing down. The part returns to the previous operational state (DCM or CCM) at the end of blanking.

Since the controller operates in DCM, it depends on the load to discharge the output when slewing down. Therefore, no switching cycles may occur if the load is very light and the output will not keep pace with the internal slew. In such cases, the blanking at the end of slewing will end after a 1ms timeout whether any switching cycles occur or not and the part will return to its previous operational state.

For applications that need to have the output slew down at the same rate as the internal slewing, register bit Enable Internal Load (EnIntLd) can be set. This activates an internal 10Ω pull down on Vout when the part is slewing down. This resistance discharges the output capacitor and helps the output keep pace with internal slewing. To help maximize efficiency, the pulldown will not activate when slewing up even if the feature is enabled via register settings.

When the internal pull down is enabled, it is active only for the time it takes the internal reference to reach its target. For example, when slewing from VFBadjust of +9% to 0%, the pull down is active only for 12 x 32µs = 384µs. In applications with large output capacitors, this time may not be sufficient to discharge the output to keep up with the internal reference. Therefore, the output can be higher than the desired regulation value at the end of the slewing sequence. If the part was in DCM before slewing began, the output will stay at the higher value at the end of the sequence. If there is no load, the output will return to the desired value very slowly. In such applications, to ensure that the controller quickly brings the output voltage into regulation, it is recommended that either PSAVE be disabled or set to ultrasonic before the output is slewed. This will ensure that the low side MOSFET will turn back on at the end of the slewing sequence even if there is no load and bring the output voltage back into regulation. Figure 4 demonstrates this with a 1000µF output capacitor and with psave disabled before slewing from VFBadj = +9% to VFBadj = -9%.

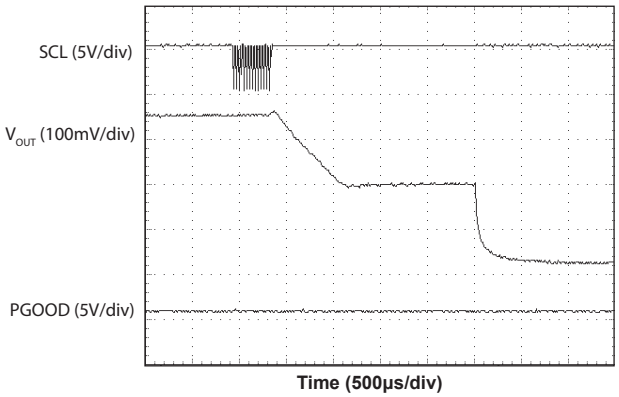


Figure 4 — Slew Down in CCM with Large Output Capacitors

Soft-shutdown

SC493 features a soft-shutdown feature: whenever switching is disabled, an internal 10Ω pull-down activates on the Vout pin which discharges the output capacitor and holds Vout low. The pull-down stays active even if the EN pin is subsequently driven low. Note that the pull-down will not activate if EN pin has not been high after power has been applied or power is cycled with EN pin low.

SmartDrive™

For each DH pulse, the DH driver initially turns on the high-side MOSFET at a slower speed, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off and the LX voltage has risen 0.5V above PGND, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching noise while maintaining high efficiency, reducing the need for snubbers or series resistors in the gate drive.

Applications Information (continued)

Power Stage Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design:

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal limitations which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

Inductor Selection

Low inductor values result in smaller size but create higher ripple current, and are less efficient because of that ripple current flowing in the inductor. Higher inductor values will reduce the ripple current/voltage and are more efficient, but are larger and more costly. The inductor selection is based upon the ripple current which is typically set between 20% and 50% of the maximum load current. Cost, size, output ripple, and efficiency are all used in the selection process. The equation for determining the inductance is shown by the next equation.

$$L = \frac{(V_{IN} - V_{OUT}) \times t_{ON}}{I_{RIPPLE}}$$

Output Capacitor Selection

Two parameters need to be determined in order to select the output capacitor — the output capacitance and the capacitor ESR. These two parameters are determined based upon the dynamic and the static regulation requirements. On a load step, the maximum duty ratio that is implemented is calculated according to the next equation.

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF(MIN)}}$$

If a maximum load step occurs instantly, the voltage undershoot can be derived by the next equation.

$$V_{UV} = \frac{(\Delta I)^2 \times L}{2 \times C \times ((D_{MAX} \times V_{IN}) - V_{OUT})}$$

For load release, the worst case happens when the maximum load release occurs at the same time as the high side turns on. The over-shoot in this situation can be derived by the next equation.

$$V_{OV} = \frac{L \times (\Delta I)^2}{2 \times C \times V_{OUT}} + \frac{(\Delta I) \times t_{ON}}{2 \times C}$$

Using the previous two equations, the output capacitor can be calculated based upon the required performance metrics (under-shoot or over-shoot voltage during the transient). Note that the above equations show the worst case analysis. In practice, the load normally changes with certain slew rate limits, so the required capacitance value may be much smaller than the value calculated using these equations.

Input Capacitor Selection

The input capacitor should be chosen to handle the RMS ripple current of a synchronous buck converter. This value is shown by the next equation.

$$I_{RMS} = \sqrt{(1 - D) \times I_{IN}^{\ 2} + D \times (I_{OUT} - I_{IN})^2}$$

where

$$D = \frac{V_{OUT}}{V_{IN}}, \quad I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN}}$$

When the input voltage is also used as VDD, it is desirable to limit the input voltage ripple to less than 20mV. The input voltage ripple can be calculated by the next equation.

$$V_{IN\_RIPPLE} = (I_{OUT} - I_{IN}) \times \frac{t_{ON}}{C_{IN}}$$

Applications Information (continued)

Stability Considerations

Unstable operation occurs in two related but distinctly different ways — double-pulsing and fast-feedback loop instability. Double-pulsing occurs due to switching noise seen at the FB input or because the FB ramp voltage is too low. This causes the high side to turn on prematurely after the 250ns minimum off-time has been completed. Double-pulsing will result in higher ripple voltage at the output, but in most applications will not adversely affect operation. However, In some cases double-pulsing can indicate the presence of loop instability, which is caused by insufficient ESR.

The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Over one cycle of ringing after the initial step is an indication that the ESR should be increased. One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is output voltage droop with load.

The on-time control regulates the valley of the output ripple voltage. This ripple voltage consists of a term generated by the ESR of the output capacitor and a term based upon the capacitance charging and discharging during the switching cycle. A minimum ESR is required to generate the required ripple voltage for regulation. For stability the ESR zero of the output capacitor should be lower than approximately one-third of the switching frequency. The formula for minimum ESR is shown by the next equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{SW}}$$

Where f_{SW} is the switching frequency.

For applications using ceramic output capacitors, the ESR is normally too small to meet the above ESR criteria. In these applications it is necessary to add a small virtual ESR network composed of two capacitors and one resistor, as shown in the Figure 5.

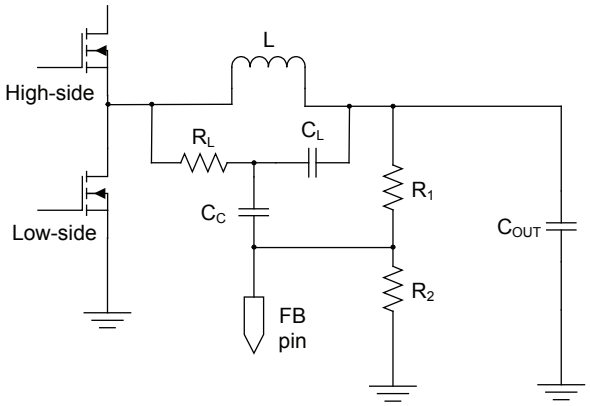


Figure 5 – Virtual ESR Network

This network creates a ramp voltage across C_L which is analogous to the ramp voltage generated across the ESR of a standard capacitor. This ramp is then capacitively coupled into the FB pin via capacitor C_C. This circuit is analyzed as follows. The AC equivalent circuit used to calculate the injected signal at FB pin is shown in Figure 6 (without considering the output ripple voltage).

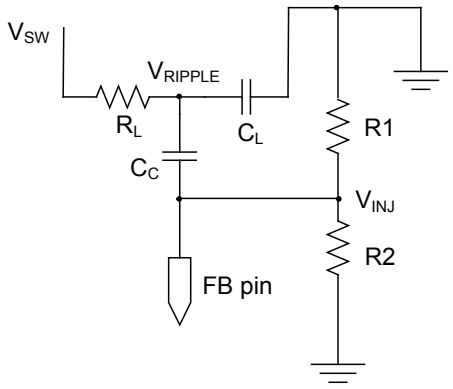


Figure 6 – AC Equivalent Circuit

The DC voltage at V_{RIPPLE} is the same as V_{SW}, which is the same as V_{OUT}. The current through resistance R_L during the on time is shown by the next equation.

Applications Information (continued)

$$I_{INJ} = \frac{V_{IN} - V_{OUT}}{R_L}$$

The following describes one way to design the virtual ESR circuit.

$$C_L \geq C_C >> \frac{1}{2\pi \times f_{SW} \times \left(\frac{R_1 \times R_2}{R_1 + R_2}\right)}$$

The current through resistance R_L will all go through C_L and the voltage change through capacitor C_L will be shown by the next equation.

$$V_{INJ} \approx \frac{V_{IN} - V_{OUT}}{R_L} \times \frac{t_{ON}}{C_L}$$

All of this voltage will be coupled into the FB pin if the rules previously stated are followed. Note that the output ripple voltage has not been taken into account. The output voltage ripple will also be coupled through the C_L and C_C path into the FB pin. The ripple voltage at the output due to the output capacitance (ignoring the capacitance ESR) is shown by the next equation.

$$V_{COUT\_RIPPLE} \approx \frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}$$

The ripple due to the capacitance ESR alone is shown by the next equation.

$$V_{ESR\_RIPPLE} = I_{RIPPLE} \text{ x } R_{ESR}$$

The output ripple voltage due to output capacitance has a 90° phase lag with respect to the ripple voltage generated by the virtual ESR. The actual ripple voltage seen at the FB pin (VFB_RIPPLE) can be approximated by the next equation.

$$V_{FB\_RIPPLE} = \sqrt{(V_{INJ} + V_{ESR\_RIPPLE})^2 + V_{COUT\_RIPPLE}^{\ 2}}$$

Resistor Divider Selection

The DC voltage at the FB pin is shown by the next equation.

$$V_{FB} \approx 0.5V + \frac{V_{FB\_RIPPLE}}{2}$$

The resistor divider value should be selected using the next equation.

$$\frac{V_{OUT}}{V_{FB}} = \frac{R_1 + R_2}{R_2}$$

Applications Information (continued)

Layout Guidelines

The switching converter can be an EMI source if the circuitry is not properly laid out on the PCB. The suggested layout guidelines are shown in Figure 7. The following are several simple rules that should be followed to prevent EMI issues.

1. The ground connection between the input capacitor, the output capacitor, and the MOSFET ground should use a short and wide trace. This can reduce the resistive losses and high frequency ringing due to stray inductance.
2. Both the high side loop and low side loop should use short traces. The high side loop includes the input capacitors, the high side MOSFET, the inductor, and the output capacitors. The low side loop includes the low side MOSFET, the inductor, and the output capacitors.
3. The LX trace should be short, since it is the main noise source of the circuit. All sensitive analog signals should be routed away from the LX trace.
4. Standard techniques such as snubbers can also be used to remove the high frequency ringing at the phase node.

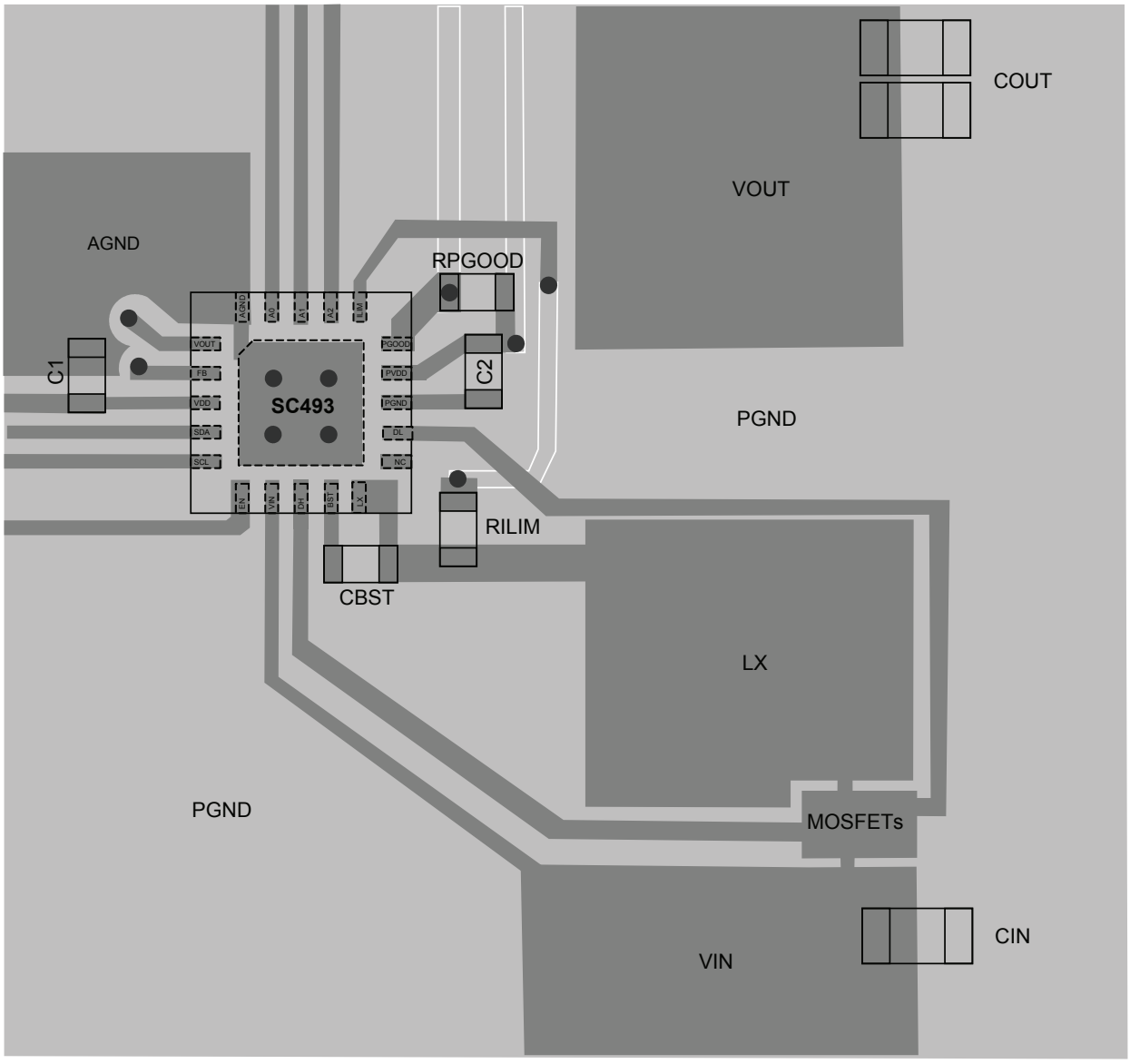


Figure 7 — Suggested Layout Guidelines

Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Access	Reset	Description
00h	PGD	DCM	DNS	BO	ILIM	OT	OVO	UVO	RO	40h	Status Register
01h	0(1)	0(1)	0(1)	0(1)	0(1)	EnIntLd	CLF	ENSW	R/W	01h	Control Register 1
02h	0(1)	0(1)	UPSV0	POD2	POD1	POD0	Freq1	Freq0	R/W	20h	Control Register 2
03h	0(1)	0(1)	UPSV1	SST2	SST1	SST0	PSV1	PSV0	R/W	2Eh	Control Register 3
04h	0(1)	0(1)	0(1)	VFBadj4	VFBadj3	VFBadj2	VFBadj1	VFBadj0	R/W	0Fh	Control Register 4
06h	0(1)	0(1)	1(2)	1(2)	1(2)	Margin2	Margin1	Margin0	R/W	3Bh	Control Register 6

Notes:
(1) Always write 0
(2) Always write 1

Definition of Registers and Bits

Status and Flag Bits Description — Register 0

A status bit reflects the current state of the converter. It becomes high when the specified condition has occurred and turns low when the specified condition has disappeared. A flag bit becomes high when the specified condition has occurred and will not turn low when the specified condition has disappeared.

Name	Bit	Definition	Description
UVO	00h[0]	Under Voltage Output Flag	Flag bit when high indicates that the output voltage fell below 70% of the regulation level while being current limited.
OVO	00h[1]	Over Voltage Output Flag	Flag bit when high indicates output voltage has been above the regulation level by 20%.
OT	00h[2]	Over Temperature Flag	Flag bit when high indicates that the over temperature circuit has tripped.
ILIM	00h[3]	Output Current Limit Flag	Flag bit when high indicates that the inductor current threshold has been reached.
BO	00h[4]	Brown Out Flag	Flag bit when high indicates that the FB voltage has fallen below PGD falling threshold (80%) with the device not in current limit. This normally means the output under voltage has been caused by low input voltage.
DNS	00h[5]	Did Not Start Flag	Flag bit when high indicates that the FB voltage did not reach the power good rising threshold (90%) within the predetermined time. This time interval is the programmed soft start time. The power good delay is 10% of the programmed soft start time.
DCM	00h[6]	Discontinuous Mode Status	Status bit when high indicates that the part is operating in discontinuous mode. The part is only permitted to operate in DCM if PSAVE or UPSAVE is enabled. The part also enters into DCM mode before the soft start process is complete. Therefore, in the shut down state and during the soft start process, this bit is also set.
PGD	00h[7]	Power Good Status	Status bit when high indicates that the PGD pin is not being pulled low and therefore the output is within regulation by $\pm$20%.

Definition of Registers and Bits (continued)

Switching and Status Control — Register 1

Name	Bit	Description	Description
ENSW	01h[0]	Enable Switching	This bits controls whether the output is enabled or not. 0: The output is disabled, both high side and low side switches are off. 1: power-on delay and soft start process can start when this bit is 1 and the EN pin is pulled high.
CLF	01h[1]	Clear Fault Status	Set to clear fault indicator flags (UVO, OVO, OT, ILIM, BO, & DNS). This bit is self clearing.
EnIntLd	01h{2}	Enable Internal Load	Set to enable internal pull down on VOUT when slewing down.

Timing Control — Registers 2 and 3

These registers provide software control over key timing parameters of the controller: frequency setting (Freq), Power-On Delay (POD) time, Soft-Start Time (SST) setting, power save (PSV) mode control, and minimum switching frequency in Ultrasonic Power Save (UPSV) mode. The details of each setting are listed in the table below.

Name	Bit	Definition	Description
Freq1 Freq0	02h [1:0]	Frequency Setting	2 bits that control the switching frequency from 250kHz to 1MHz. 00 : 250kHz 01 : 500kHz 10 : 750kHz 11 : 1MHz
POD2 POD1 POD0	02h [4:2]	Power-on Delay Time	3 bits that control the power-on delay from 0µs to 16ms. 000 : 0µs 001 : 250µs 010 : 500µs 011 : 1000µs 100 : 2ms 101 : 4ms 110 : 8ms 111 : 16ms
SST2 SST1 SST0	03h [4:2]	Soft Start Time Setting	3 bits that control the soft start time from 250µs to 16ms. 000 : 250µs 001 : 500µs 010 : 1000µs 011 : 2ms 100 : 4ms 101 : 8ms 110 : 16ms 111 : 16ms
PSV1 PSV0	03h [1:0]	Power Save Mode Control	These bits control whether the device is permitted to enter power save when input, output, and load conditions dictate. If permitted to enter power save, they also control what mode of power save the part can enter. 00 : PSAVE is disabled 01 : PSAVE enabled (low I_Q, no ultrasonic mode) 10 : UPSAVE enabled (ultrasonic mode) 11 : PSAVE is disabled

Definition of Registers and Bits (continued)

Name	Bit	Definition	Description
UPSV1 UPSV0	03h [5] 02h [5]	Ultrasonic Power Save Frequency	2 bits that control the nominal minimum switching frequency in ultrasonic mode. 00 : 6.25kHz 01 : 12.5kHz 10 : 18.75kHz 11 : 25kHz

Output Voltage Control — Registers 4 and 6

These registers provide fine & coarse control over the output voltage. Margin bits can vary the the output by +/-10% in 5% steps. VFBadj can move the output by +/-9% in 0.75% steps. When both registers are used together, the change in the output voltage is determined by the multiplication of the 2 settings, i.e., setting Margin to +10% with +9% VFBadj will change the output by +19.9% whereas a setting Margin to +10% with -9% VFBadj will change the output by +0.1%.

Name	Bit	Definition	Description
VFBadj4 VFBadj3 VFBadj4 VFBadj1 VFBadj0	04h[4:0]	Output Voltage Adjustment	000xx : -9% 00100 : -8.25% 00101 : -7.50% 00110 : -6.75% 00111 : -6% 01000 : -5.25% 01001 : -4.50% 01010 : -3.75% 01011 : -3% 01100 : -2.25% 01101 : -1.50% 01110 : -0.75% 01111 : -0% 10000 : -0% 10001 : +0.75% 10010 : +1.50% 10011 : +2.25% 10100 : +3% 10101 : +3.75% 10110 : +4.50% 10111 : +5.25% 11000 : +6% 11001 : +6.75% 11010 : +7.50% 11011 : +8.25% 111xx : +9%
Margin1 Margin0	06h[2:0]	Margin Control	These bits control whether margining is disabled, set to high or set to low. 000 : Margining disabled 001 : Set output to 10% below set value 010 : Set output to 5% below set value 011 : Margining disabled 100 : Margining disabled 101 : Set output to 5% above set value 110 : Set output to 10% above set value 111 : Margining disabled

Serial Interface

The I²C General Specification

The SC493 is a read-write slave-mode I²C device and complies with the Philips I²C standard Version 2.1, dated January 2000. The SC493 has six user-accessible internal 8-bit registers. The I²C interface has been designed for program flexibility, supporting direct format for write operation. Read operations are supported on both combined format and stop separated format. While there is no auto increment/decrement capability in the SC493 I²C logic, a tight software loop can be designed to randomly access the next register independent of which register was accessed first. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

SC493 Limitations to the I²C Specifications

The SC493 only recognizes seven bit addressing. This means that ten bit addressing and CBUS communication are not compatible. The device can operate in either standard mode (100kbit/s) or fast mode (400kbit/s).

Slave Address Assignment

The seven bit slave address is $0001A_2A_1A_0x$, where $A_2A_1A_0$ are set by the respective pins on the device. Bit 8 is the data direction bit: $0001A_2A_1A_00$ is used for a write operation, and $0001A_2A_1A_01$ is used for a read operation.

Supported Formats

The supported formats are described in the following subsections.

Direct Format — Write

The simplest format for an I²C write is direct format. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The I²C logic then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the appropriate 8 bit data byte. Once again the slave acknowledges and the master terminates the transfer with the stop condition [P].

Combined Format — Read

After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The I²C logic then acknowledges that it is being addressed, and the master responds with an 8 bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the previously addressed 8 bit data byte; the master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].

Stop Separated Reads

Stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The SC493 then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a stop or restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the SC493 with a read command. The device acknowledges this request and returns the data from the register location that had previously been set up.

SEMTECH

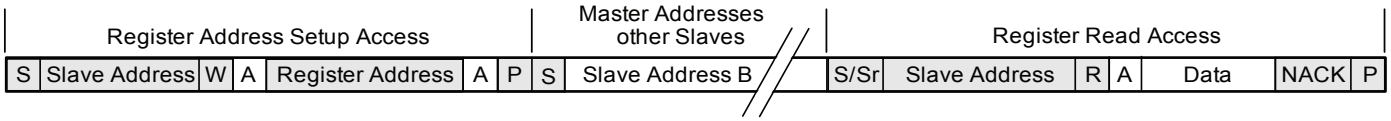
Serial Interface (continued)

I²C Direct Format Write

S – Start Condition
W – Write = '0'
A – Acknowledge (sent by slave)
P – Stop condition

Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

I²C Stop Separated Format Read



S – Start Condition
W – Write = '0'
R – Read = '1'
A – Acknowledge (sent by slave)
NAK – Non-Acknowledge (sent by master)
Sr – Repeated Start condition
P – Stop condition

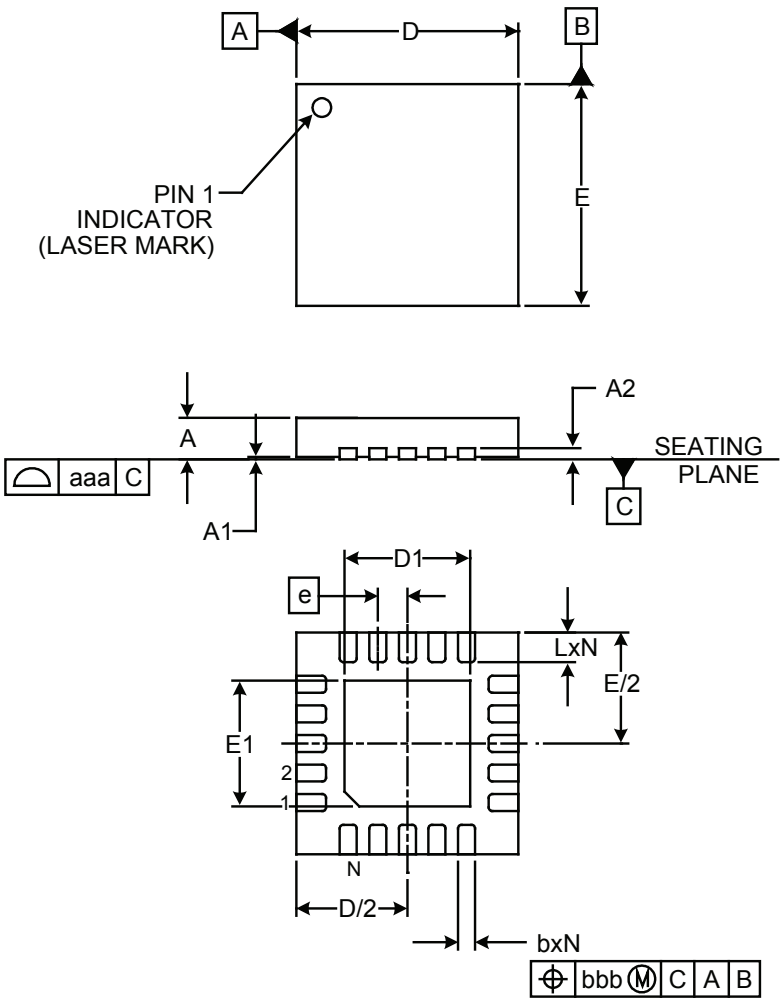
Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

I²C Combined Format Read

S – Start Condition
W – Write = '0'
R – Read = '1'
A – Acknowledge (sent by slave)
NAK – Non-Acknowledge (sent by master)
Sr – Repeated Start condition
P – Stop condition

Slave Address – 7-bit
Register address – 8-bit
Data – 8-bit

Outline Drawing - MLPQ-UT-20 3x3

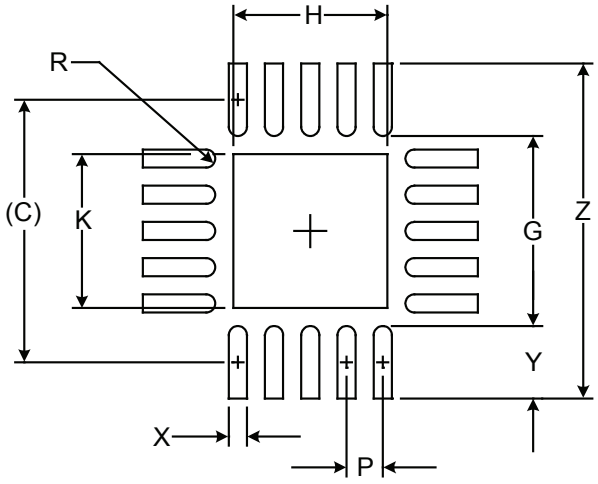


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.1524)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.016 BSC			0.40 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		20			20	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP is 1.90 x 190mm.

Land Pattern - MLPQ-UT-20 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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