Single-cell Li-Ion Charger Tri-Mode with Timer and NTC

Features

- Single input 30V protected charger
- Adapter, USB High, USB Low modes
- Charging by current regulation, voltage regulation, and thermal limiting
- Programmable currents from 70mA to 1A
- Fast-charge current regulation — 15% at 70mA, 9% at 700mA
- Constant voltage — 4.2V, 1% regulation
- Input voltage protection — 30V
- Current-limited adapter support capability — reduces power dissipation in charger IC
- USB modes automatically reduce charge current if needed to prevent USB Vbus overload
- Instantaneous CC-to-CV transition for faster charging
- Battery temperature NTC thermistor interface
- Multi-stage charge timer for safety and alternative termination, IEEE Std. 1725-2006 compliant
- Termination on current or timer — first to occur
- Soft-start reduces adapter or USB load transients
- High operating voltage range permits use of unregulated adapters
- Complies with CCSA YD/T 1591-2006
- High-current USB Dedicated Charger compatible
- Ultra-thin 2×2×0.6 (mm) MLPD package
- Lead-free and halogen-free
- WEEE and RoHS compliant

Applications

- Mobile phones
- Personal Media Players
- Personal Navigation Devices

Description

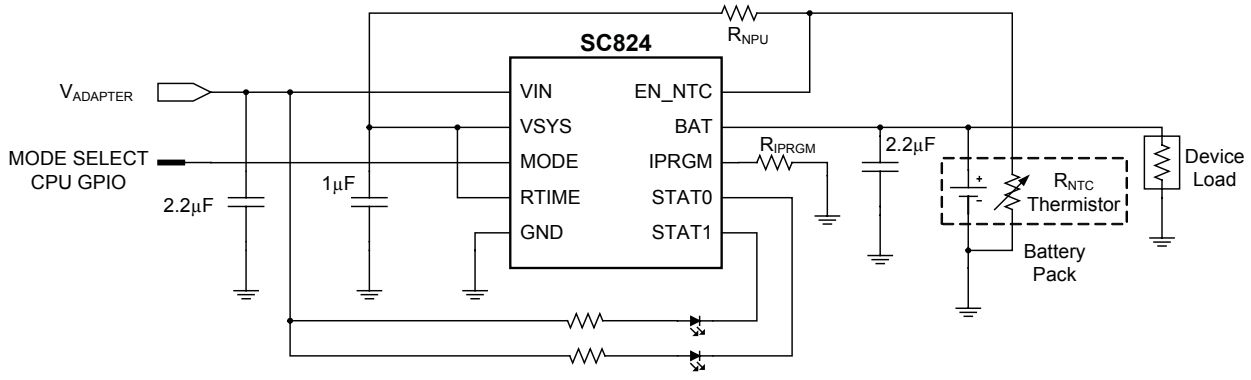
The SC824 is a single input triple mode (adapter/USB High, USB Low) linear single-cell Li-Ion battery charger in a 10 lead 2×2 (mm) MLPD ultra-thin package.

Charging begins automatically when an input source is applied to the charging input. The input is designed to survive sustained input voltage up to 30V to protect against hot plug overshoot and faulty charging adapters. Thermal limiting protects the SC824 from excessive power dissipation.

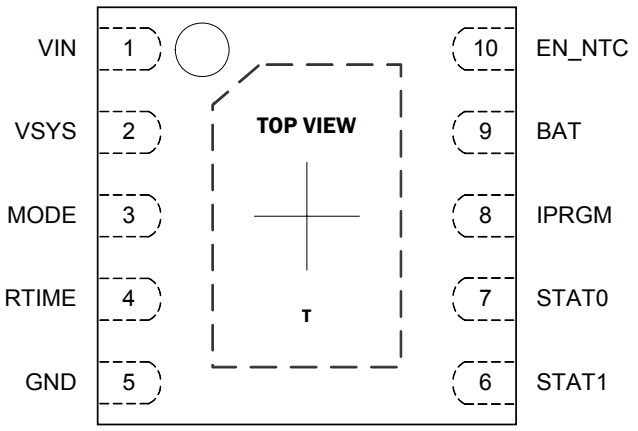
The SC824 provides three modes of charging: adapter mode, USB low power mode, and USB high power mode. Adapter mode charges up to 1A with the charging adapter operating either in voltage regulation or in current limit to obtain the lowest possible power dissipation. A single current programming pin is used to program precharge current, termination current, and fast-charge current in fixed proportions. The USB modes provide low and high power fast-charge currents. The two USB modes dynamically limit the charging load if necessary to automatically prevent overloading the USB Vbus supply.

The SC824 provides a battery NTC thermistor interface to disable charging when the battery temperature exceeds programmed thresholds. An optional programmable multi-stage charge timer protects against a faulty battery, or terminates charging on timeout if the system load is too great to terminate charging on current. A 45 minute top-off period following termination ensures a fully charged battery. The monitor state restarts a charge cycle if the battery discharges after the charger has turned off.

Typical Application Circuit



Pin Configuration



MLPD-UT10; 2×2, 10 LEAD

θ_{JA} = 68°C/W

Ordering Information

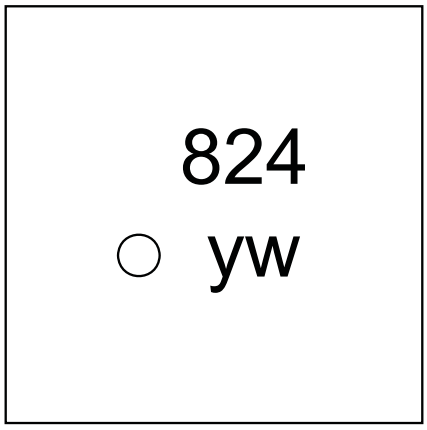
Device	Package
SC824ULTRT[1][2]	MLPD-UT-10 2×2
SC824EVB	Evaluation Board

Notes:

(1) Available in tape and reel only. A reel contains 3,000 devices.

(2) Lead-free packaging only. Device is WEEE and RoHS compliant, and halogen-free.

Marking Information



yw = Date Code

SEMTECH

Absolute Maximum Ratings

VIN, STAT0, STAT1 (V) ..... -0.3 to +30.0
VSYS, BAT (V) ..... -0.3 to +6.5
MODE (V) ..... -0.3 to (BAT + 0.3)
EN_NTC, RTIME, IPRGM (V) ..... -0.3 to (VSYS + 0.3)
VIN input current (A) 1.5
BAT, IPRGM Short to GND Duration ..... Continuous
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Operating Ambient Temperature (°C) ..... -40 to +85
VIN Adapter Mode Operating Voltage[2] (V) ... 4.36 to 8.20
VIN USB Modes Operating Voltage[2] (V) ..... 4.70 to 8.20

Thermal Information

Thermal Resistance, Junction to Ambient[3] (°C/W) 68
Maximum Junction Temperature (°C) ..... +150
Storage Temperature Range (°C) ..... -65 to +150
Peak IR Reflow Temperature (°C) ..... +260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Operating Voltage is the input voltage at which the charger is guaranteed to begin operation. These ranges apply to charging sources operating in voltage regulation. Charging sources operating in current limit may be pulled below these ranges by the charging load. Maximum operating voltage is the maximum Vsupply as defined in EIA/JEDEC Standard No. 78, paragraph 2.11.
(3) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Test Conditions: V_{VIN} = 5.00V [1], V_{BAT} = 3.70V unless specified; Typ values at 25°C; Min and Max at -40°C < T_A < 85°C, unless specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VIN Under-Voltage Lockout Rising Threshold	VT_{UVLO-R}		4.16	4.26	4.36	V
VIN Under-Voltage Lockout Falling Threshold [2]	VT_{UVLO-F}	$V_{VIN} > V_{BAT}$	2.70	2.85	3.00	V
VIN OVP Rising Threshold	VT_{OVP-R}			9.3	9.6	V
VIN OVP Falling Threshold	VT_{OVP-F}		8.2	8.5		V
VIN OVP Hysteresis	VT_{OVP-H}	$VT_{OVP-R} - VT_{OVP-F}$	500	800		mV
VIN Charging Disabled Operating Current	ICC_{VIN_DIS}	V_{EN_NTC} = 0V, V_{RTIME} = 0V		0.8	1.5	mA
VIN Charging Enabled Operating Current	ICC_{VIN_EN}	V_{EN_NTC} = 2.3V, V_{RTIME} = 0V, I_{BAT} = 1mA; excluding I_{BAT} and I_{IPRGM}		1.8	2.5	mA
Regulation Voltage	V_{CV}	I_{BAT} = 50mA, -40°C ≤ T_J ≤ 125°C	4.16	4.20	4.24	V
Voltage Load Regulation	V_{CV_LOAD}	1mA ≤ I_{BAT} ≤ 1A, -40°C ≤ T_J ≤ 125°C		-20		mV/A
BAT Re-charge Threshold	VT_{ReQ}	$V_{CV} - V_{BAT}$	60	100	140	mV
BAT Pre-charge Threshold (rising)	VT_{PreQ}		2.85	2.90	2.95	V

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Battery Leakage Current	$IBAT_{V0}$	$V_{BAT} = V_{CV}$, $V_{VIN} = 0V$, $V_{EN\_NTC} = 0V$		0.1	1	µA
	$IBAT_{DIS}$	$V_{BAT} = V_{CV}$, $V_{VIN} = 5V$, $V_{EN\_NTC} = 0V$		0.1	1	µA
	$IBAT_{MON}$	$V_{BAT} = V_{CV}$, $V_{EN\_NTC} = 2.3V$, $V_{RTIME} = 0V$ and charging terminated		0.1	1	µA
IPRGM Programming Resistor	R_{IPRGM}		2.05		29.4	kΩ
I_{BAT} Fast-Charge Current, adapter mode or USB High Power mode	I_{FQ}	$R_{IPRGM} = 2.94k\Omega$, $VT_{PreQ} < V_{BAT} < V_{CV}$ $R_{IPRGM} = 4.42k\Omega$, $VT_{PreQ} < V_{BAT} < V_{CV}$	643 427	694 462	745 497	mA
USB Low Power mode Fast-Charge current	I_{FQ_Low}	$R_{IPRGM} = 2.94k\Omega$, $VT_{PreQ} < V_{BAT} < V_{CV}$ $R_{IPRGM} = 4.42k\Omega$, $VT_{PreQ} < V_{BAT} < V_{CV}$	105 69	139 92	173 116	mA
I_{BAT} Pre-Charge Current	I_{PreQ}	$R_{IPRGM} = 2.94k\Omega$, $1.8V < V_{BAT} < VT_{PreQ}$ $R_{IPRGM} = 4.42k\Omega$, $1.8V < V_{BAT} < VT_{PreQ}$	105 69	139 92	173 116	mA
I_{BAT} Termination Current	I_{TERM}	$R_{IPRGM} = 2.94k\Omega$, $V_{BAT} = V_{CV}$ $R_{IPRGM} = 4.42k\Omega$, $V_{BAT} = V_{CV}$	59 38	69 46	80 55	mA
VIN - BAT Dropout Voltage	V_{DO}	$I_{BAT} = 700mA$, $0°C \le T_J \le 125°C$		0.4	0.6	V
IPRGM Fast-charge Regulated Voltage	V_{IPRGM_FQ}	$V_{VIN} = 5.0V$, $VT_{PreQ} < V_{BAT} < V_{CV}$		2.04		V
IPRGM Pre-charge Regulated Voltage	V_{IPRGM_PQ}	$V_{BAT} < VT_{PreQ}$		0.408		V
IPRGM Termination Threshold Voltage	VT_{IPRGM_TERM}	$V_{BAT} = V_{CV}$		0.204		V
VIN USB Modes Under-Voltage Load Regulation Limiting Voltage	V_{UVLR}	5mA ≤ VIN supply current limit ≤ 500mA, $V_{MODE} = 2V$, $R_{IPRGM} = 2.94k\Omega$ (694mA)	4.40	4.51	4.70	V
Thermal Limiting Threshold Temperature	T_{TL}			130		°C
Thermal Limit Rate	i_T	$T_J > T_{TL}$		-50		mA/ °C
VSYS Output Voltage	V_{VSYS}	$V_{VIN} \ge 5V$, $I_{VSYS} \le 1mA$		4.6		V
VSYS Output Current	I_{VSYS}				1	mA
EN_NTC Thresholds	RT_{NTC_DIS}	Charger Disable/Reset (Falling)	9	10	11.5	$\%V_{VSYS}$
	RT_{NTC_HF}	NTC Hot (Falling)	29	30	31	$\%V_{VSYS}$
	RT_{NTC_CR}	NTC Cold (Rising)	74	75	76	$\%V_{VSYS}$
	RT_{NTC_NBR}	No-Battery Mode select (Rising)	94	95	96	$\%V_{VSYS}$
EN_NTC Hysteresis	VT_{NTC_HYS}	$V_{VIN} = 5V$		45		mV
EN_NTC Disable/Reset Hold Time [3]	$t_{NTC\_DIS\_H}$	Momentary disable resets charger	500			ns

Electrical Characteristics (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RTIME Programming Resistor	R_{RTIME}		19.6		200	kΩ
RTIME Regulated Voltage	V_{RTIME}	R_{RTIME} = 130kΩ to GND		1.1		V
Precharge Fault Time-Out	t_{PreQF}	Internal Timer Only	38	45	52	mins
Constant Current (CC) Fault Time-Out	t_{CCF}	R_{RTIME} = 130kΩ to GND	8.5	10	11.5	hrs
		R_{RTIME} connected to VSYS (Int. Timer)	2.55	3	3.45	hrs
Constant Voltage (CV) Time-Out	t_{CV}	Internal Timer Only	2.55	3	3.45	hrs
Top-off Time-Out	t_{TO}	Internal Timer Only	38	45	52	mins
Charge-done Status Delay	t_{SD}	Internal Timer Only	17	20	23	s
MODE Input High Voltage Threshold	V_{IH}		1.6			V
MODE Input Mid Voltage Range	V_{IM}		0.65		1.3	V
MODE Input Low Voltage Threshold	V_{IL}				0.3	V
MODE Input High-range Input Current	I_{IH}	V_{MODE} = Min V_{IH}		23	75	µA
MODE Input Mid-range Load Limit	I_{IM}	Input will float to mid range when this load limit is observed.	-5		5	µA
MODE Input Low-range Input Current	I_{IL}	0V ≤ V_{MODE} ≤ Max V_{IL}	-25	-12		µA
MODE Input Monitor State Input Current	I_{MODE_MON}	V_{MODE} = V_{BAT} = V_{CV}, V_{EN_NTC} = 2.3V, V_{RTIME} = 0V and charging terminated			1	µA
MODE Input Leakage	I_{ILEAK}	V_{VIN} = 5V and V_{EN_NTC} = 0V, or V_{VIN} = 0V, V_{MODE} = V_{CV}			1	µA
STAT0, STAT1 Output Low Voltage	V_{STAT_LO}	I_{STATx_SINK} = 1mA			0.5	V
STAT0, STAT1 Output High Current	I_{STAT_HI}	V_{STATx} = 5V			1	µA

Notes:

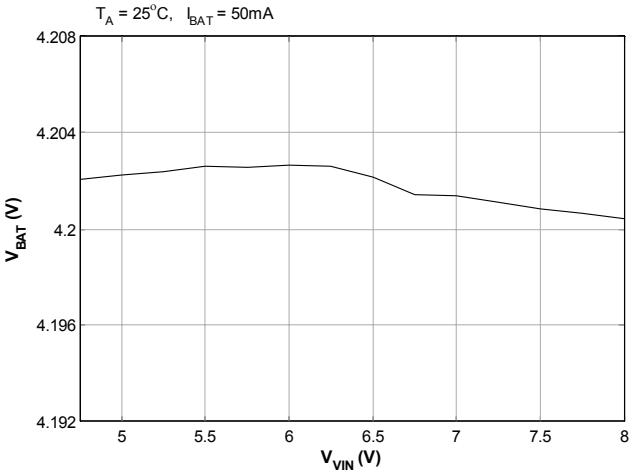
(1) Electrical Characteristics apply for V_{VIN} = 4.75V to 5.25V, but are tested only at V_{VIN} = 5.00V, unless noted.

(2) Sustained operation to VT_{UVLO-F} ≤ V_{VIN} is guaranteed only if a current limited charging source applied to VIN is pulled below VT_{UVLO-R} by the charging load in adapter mode; forced VIN voltage below VT_{UVLO-R} may in some cases result in regulation errors or other unexpected behavior.

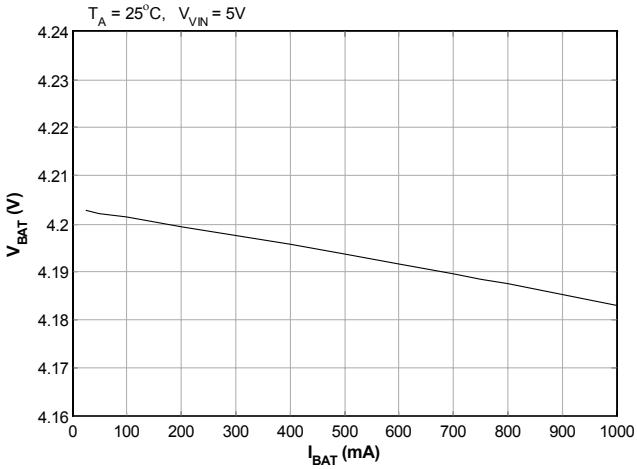
(3) Not tested. Guaranteed by design.

Typical Characteristics

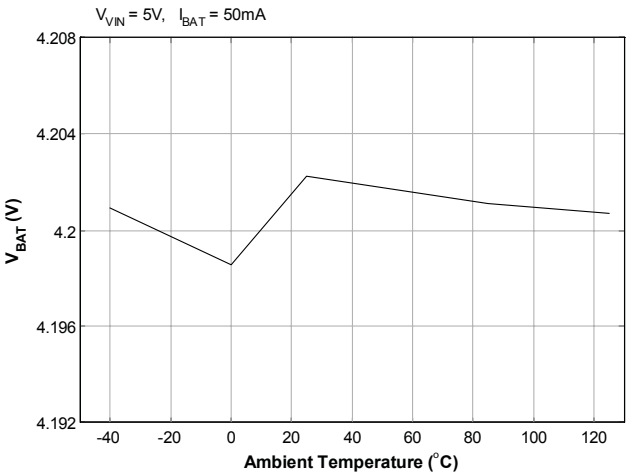
CV Line Regulation



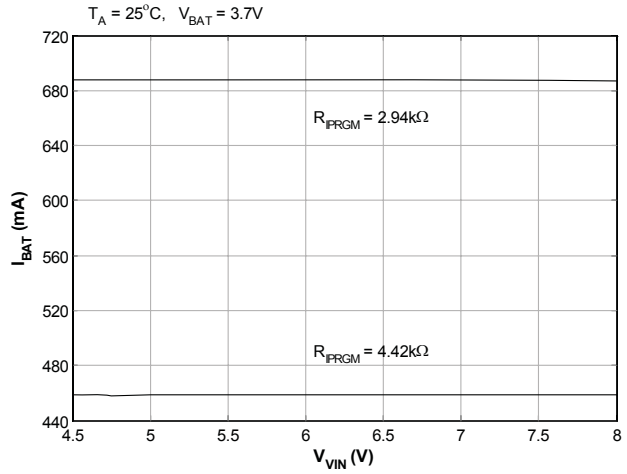
CV Load Regulation



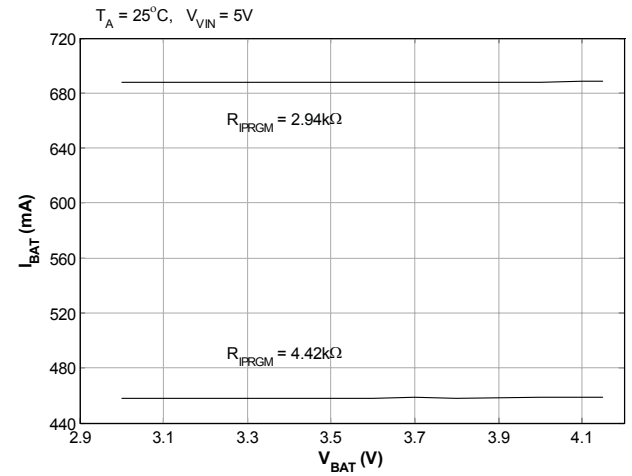
CV Temperature Regulation



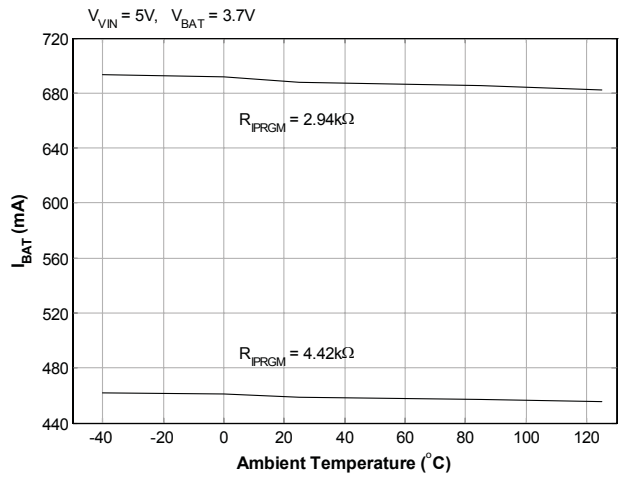
CC AD or USB High FQ Line Regulation



CC AD or USB High FQ V_{BAT} Regulation

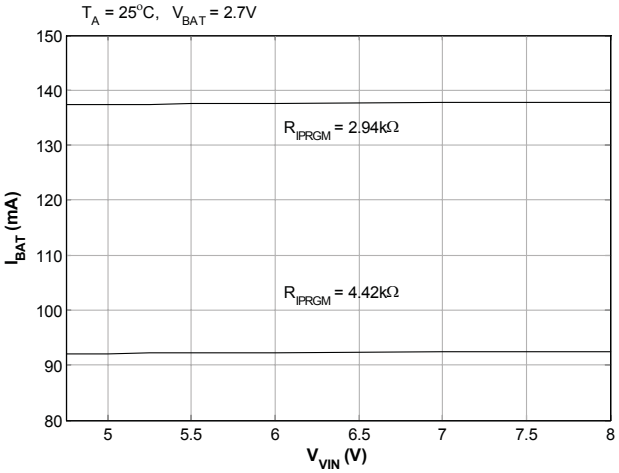


CC AD or USB High FQ Temperature Regulation

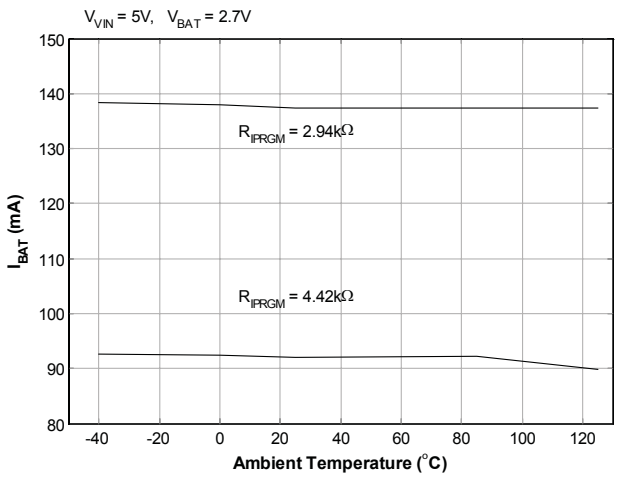


Typical Characteristics (continued)

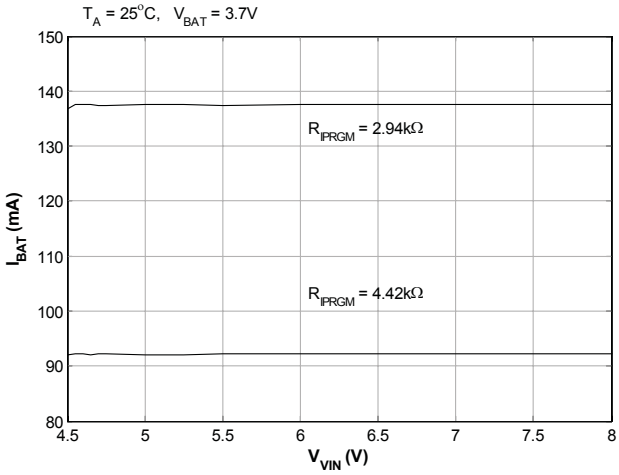
CC PQ Line Regulation



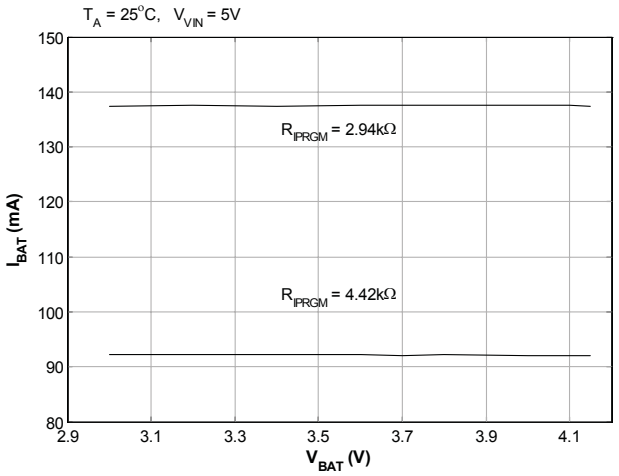
CC PQ Temperature Regulation



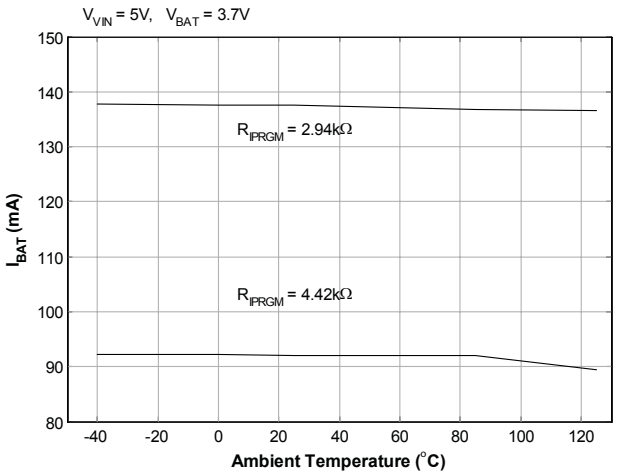
CC USB Low Power FQ Line Regulation



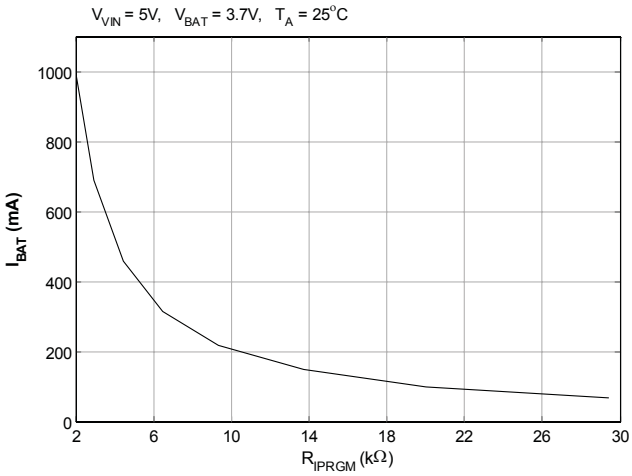
CC USB Low Power FQ V_{BAT} Regulation



CC USB Low Power FQ Temperature Regulation

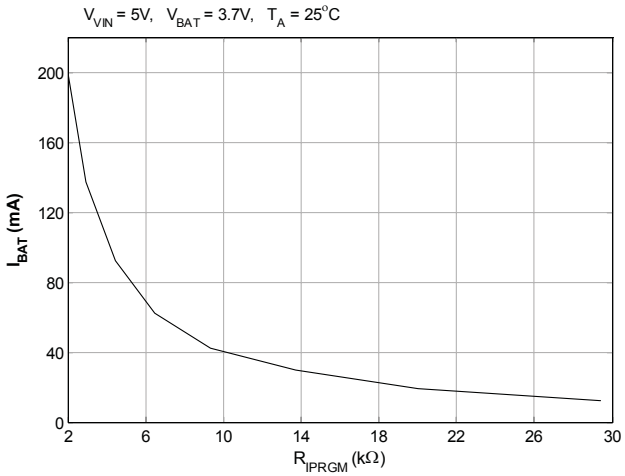


I_{FQ} vs. R_{IPRGM}, Adapter or USB High Power Modes

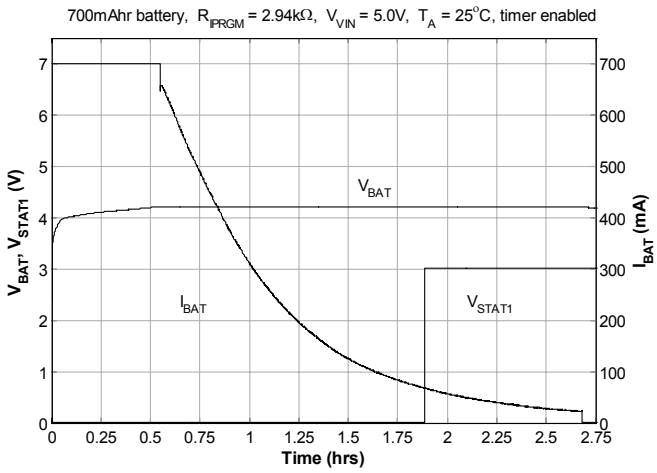


Typical Characteristics (continued)

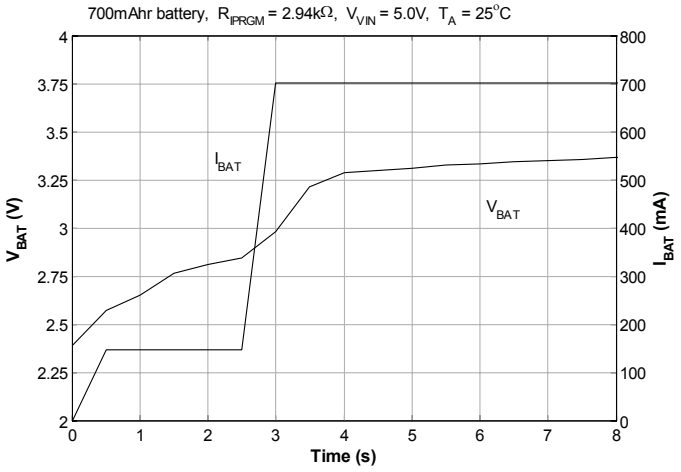
I_{PQ} vs. R_{IPRGM}; I_{FQ} vs. R_{IPRGM}, USB Low Power Mode



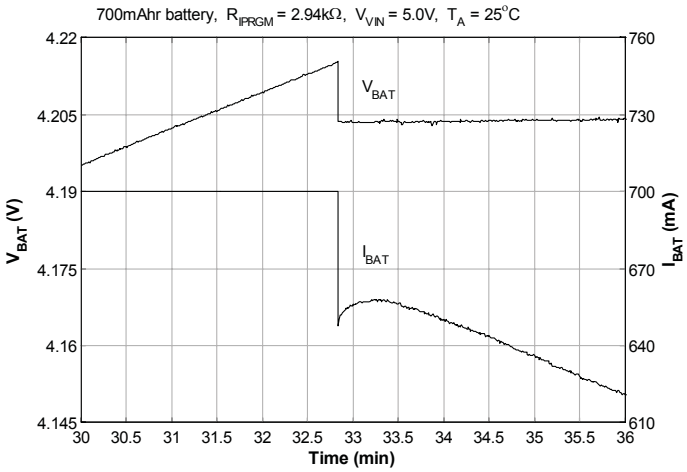
Charging Cycle Battery Voltage and Current



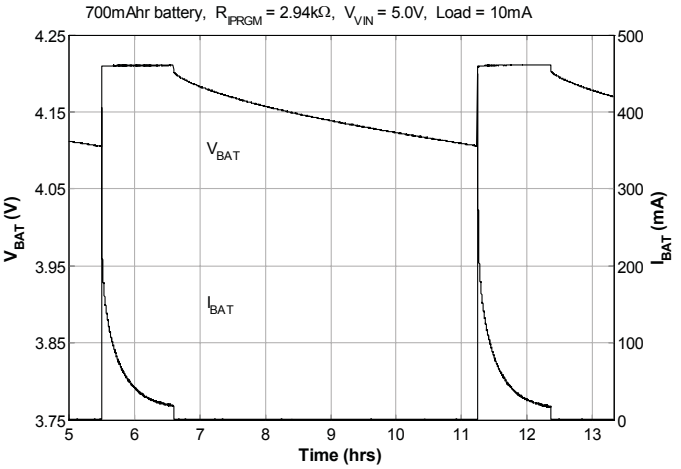
Pre-Charging Battery Voltage and Current



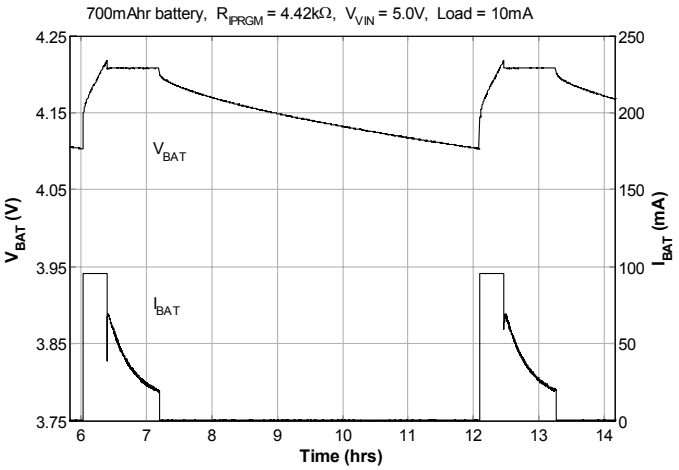
CC-to-CV Battery Voltage and Current



Re-Charge Cycle BAT Pin Voltage and Current

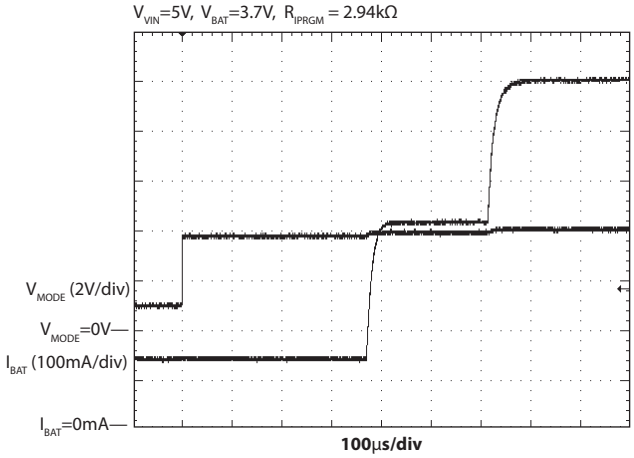


USB Low-Power Re-Charge Cycle

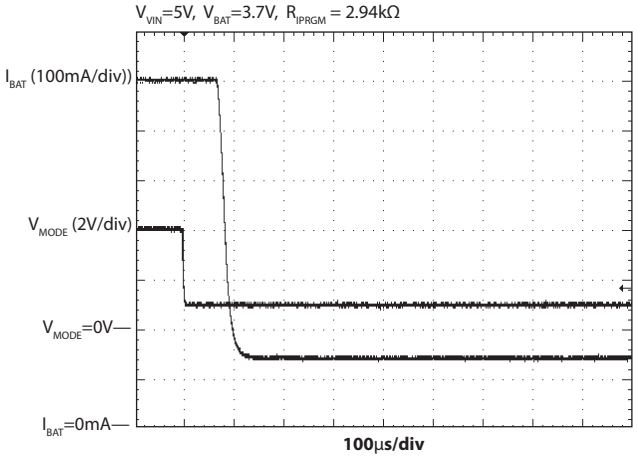


Typical Characteristics (continued)

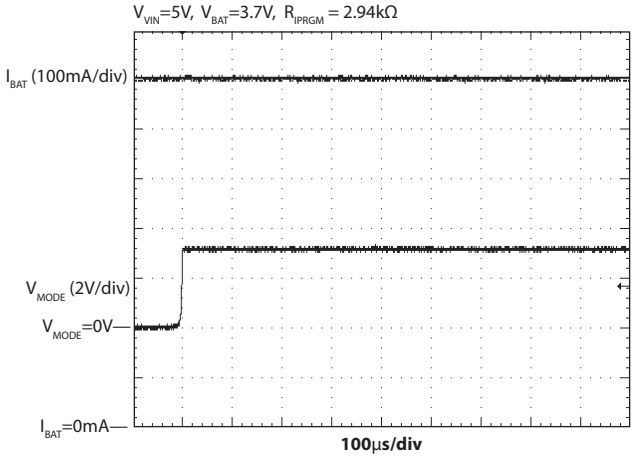
Mode Reselection — USB Low to USB High



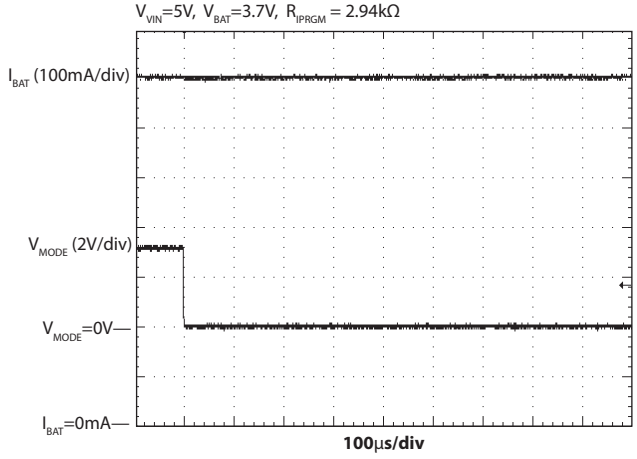
Mode Reselection — USB High to USB Low



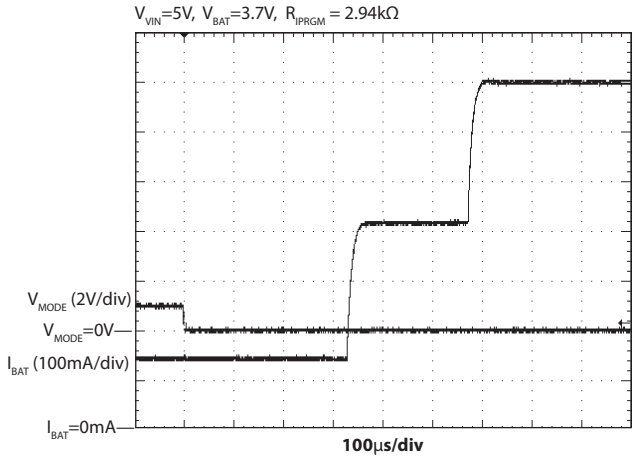
Mode Reselection — AD to USB High



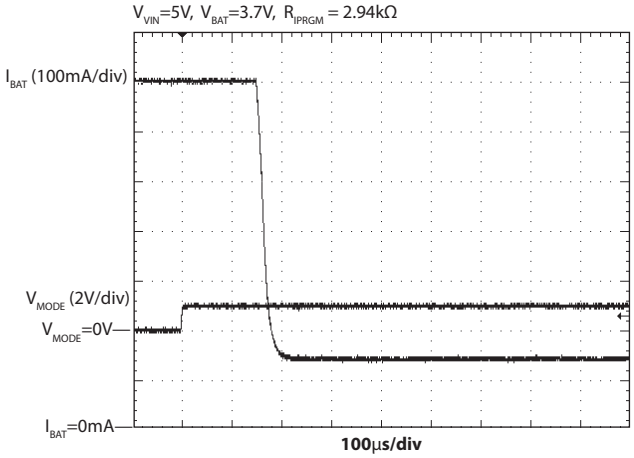
Mode Reselection — USB High to AD



Mode Reselection — USB Low to AD



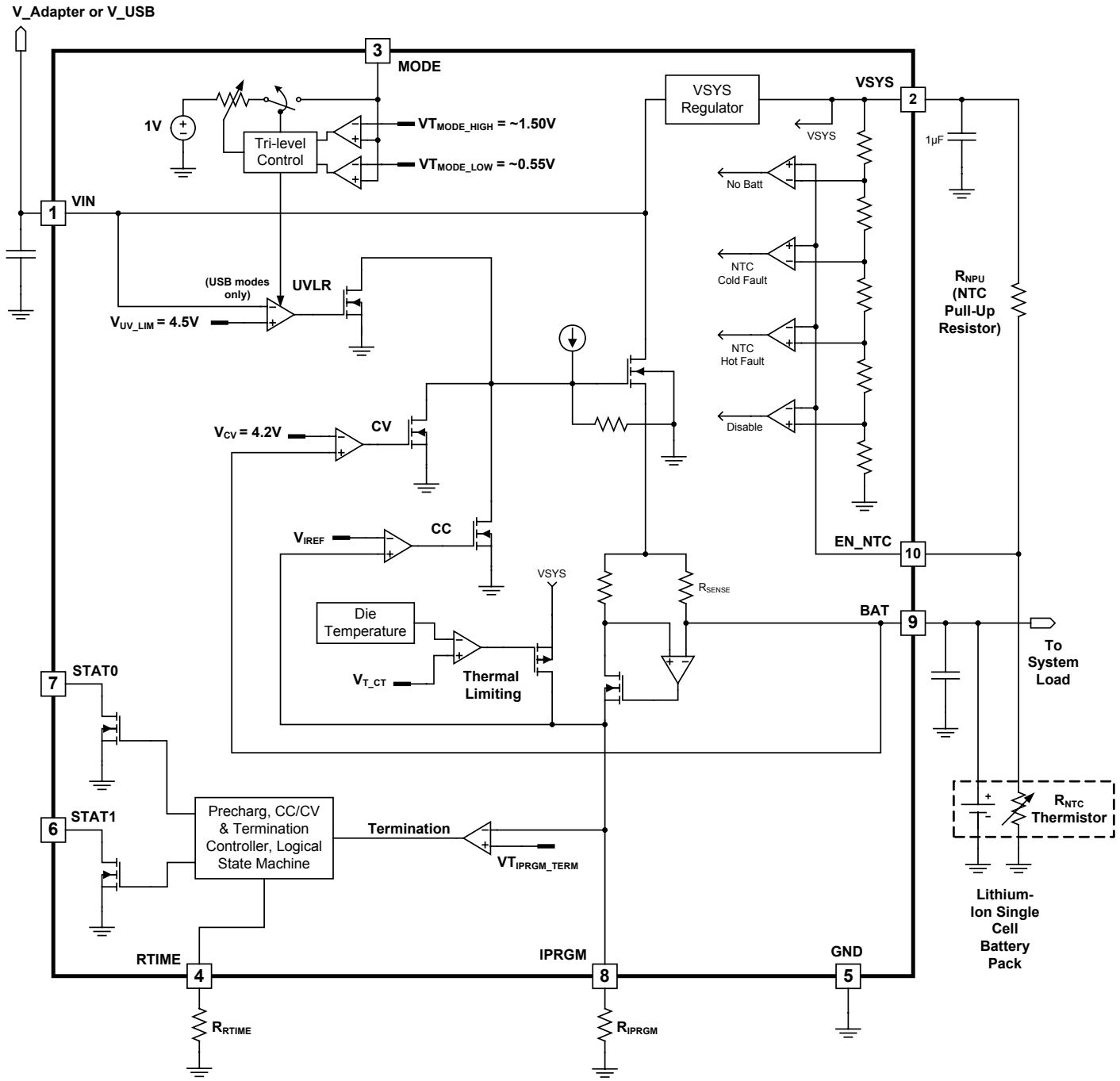
Mode Reselection — AD to USB Low



Pin Descriptions

Pin #	Pin Name	Pin Function
1	VIN	Supply pin — Connect to charging adapter (wall adapter or USB). This pin is protected against damage due to high voltage up to 30V.
2	VSYS	System reference voltage supply — 4.6V reference used internally and externally by the NTC circuit. Must have a 1µF capacitor connected between VSYS and GND.
3	MODE	Charging mode selection (tri-level logical) input — Logical high selects USB high power mode, floating selects USB low power mode, ground selects adapter mode.
4	RTIME	Timer setting pin — Connect a resistor between this pin and ground to set the time-out value of the CC mode timer. Connect to ground to disable the timer. Tie to VSYS to select the 3 hour CC timer using the internal oscillator.
5	GND	Ground
6	STAT1	Status open drain output pin that is active low when charging is in progress, with or without a charging fault. When charging is complete, pin is released. See STATx Pin Truth Table.
7	STAT0	Status open drain output pin that is pulled low when a valid charging adapter is connected and the voltage is greater than the UVLO level and less than the OVP level, and no charging fault is detected. Pin is released when the input is disconnected from a power supply, or to indicate a charging fault. See STATx Pin Truth Table.
8	IPRGM	Charging current programming pin — Connect a resistor from this pin to ground to program charge current. Pre-charge current (also USB low power mode fast-charge current) is 20% of IPRGM-programmed fast-charge current in all modes. The charging termination current threshold for all modes is 10% of the IPRGM programmed fast-charge current. If this pin is grounded, pin-short detection holds the SC824 in logical reset, with charging disabled.
9	BAT	Charger output — Connect to battery positive terminal.
10	EN_NTC	Battery NTC thermistor connection pin — EN_NTC pin input voltage ranges are ratiometric with respect to the VSYS pin output voltage. The safe-to-charge battery temperature range is programmed with a resistor from the EN_NTC pin to the VSYS pin, and a battery pack NTC thermistor to ground; charging is suspended when the EN_NTC pin voltage is less than 30%, or greater than 75%, of V_{VSYS}. When pulled down below 10% of V_{VSYS}, charging is unconditionally disabled. When the level exceeds 95% of V_{VSYS}, the battery is assumed to be disconnected and the device operates in No-Battery mode.
T	Thermal Pad	Pad is for heatsinking purposes — The thermal pad is not connected internally. Connect exposed pad to ground plane using multiple vias.

Block Diagram



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Applications Information

Charger Operation

The SC824 is a single input, tri-mode, stand-alone Li-Ion battery charger. It has a tri-state MODE input pin that allows the device to be put in USB high power, USB low power, or adapter mode. Fast-charge current is programmed with a resistor from the IPRGM pin to ground. USB high power mode is equal to adapter mode current. USB low power current is 20% of fast-charge current.

When a valid input supply is detected, the STAT0 output goes low. A charge cycle is initiated and the STAT1 output goes low. When the battery voltage is less than the pre-charge threshold voltage, the pre-charge current is output to the battery. Pre-charge current is fixed at 20% of the programmed adapter mode or USB high power mode fast-charge current, and is equal to the USB low power mode fast-charge current.

Fast-charge Constant Current (CC) regulation begins when the battery voltage exceeds the pre-charge threshold. The charge current soft-starts in three steps (20%, 60%, and 100% of programmed fast charge current) to reduce adapter load transients. In USB low power mode, the CC current is held at the 20% step.

The charger begins Constant Voltage (CV) regulation when the battery voltage rises to the fully-charged single-cell Li-Ion regulation voltage (V_{CV}), nominally 4.2V. When regulating the output voltage, the charge current gradually decreases as the battery charges. The STAT1 output goes high, after a 20 second delay, when the output current I_{BAT} drops below the termination current threshold. This is known as charge termination. The termination current threshold is 10% of the IPRGM-programmed fast-charge current regardless of the mode selected.

Each step of the charge cycle is separately timed using the optional programmable charge timer. Time-out of the fixed 45 minute pre-charge stage timer or the fixed or programmable CC stage timer is indicated as a fault, which is encoded in the STAT0 and STAT1 outputs. Time-out during the CV timer stage has the same result as normal charge termination. When the timer is used, the output remains on for 45 minutes following termination to ensure that the battery is fully topped-off, then turns off. If the timer is not used, the charger turns off immediately upon reaching the termination current.

Optional Top-off Charging, and Monitoring

Depending on the state of the RTIME pin, upon termination the SC824 either tops-off the battery by operating as a voltage regulator (known as float charging) for 45 minutes or it immediately turns off its output. Once the output is turned off, the device enters the monitor state. In this state, the output remains off until the BAT pin voltage decreases by the re-charge threshold (VT_{ReQ} = 100mV typically). A re-charge cycle then begins automatically and the process repeats. If the timer is enabled, then the multistage timer also protects the re-charge cycle. Re-charge cycles are not indicated by the STAT1 pin.

A forced re-charge cycle can also be periodically commanded by the processor to maintain the battery in a fully charged state without discharging to the re-charge threshold, and without top-off charging. See the Monitor State section for details.

Charging Input Mode Dependencies

In adapter mode, a programmed charging current greater than the adapter's current limit will pull down the VIN pin voltage to the battery voltage plus charger dropout voltage. This is referred to as Current-Limited-Adapter (CLA) operation. The UVLO falling threshold is set close to the battery voltage pre-charge threshold to permit low-dissipation charging from a current limited adapter.

Both USB modes provide Under-Voltage Load Regulation (UVLR) in which the charging current is reduced if needed to prevent overloading of the USB Vbus supply. UVLR ensures the integrity of the USB Vbus supply for all devices sharing a host or hub supply. UVLR can also serve as a low-cost alternative to commanding USB low power charge current where there is no signal available to indicate whether USB low or high power mode should be selected.

CC Fast-charge Current Programming

CC regulation is active when the battery voltage is above VT_{PreQ} and less than V_{CV}. When either adapter mode or USB high power mode is selected, the programmed CC regulation fast-charge (FQ) current is inversely proportional to the IPRGM pin resistance to GND according to the following equation:

Applications Information (continued)

$$I_{FQ} = \frac{V_{IPRGM\_Typ}}{R_{IPRGM}} \times 1000$$

The nominal fast charge current can be programmed to any value between 70mA and 1000mA.

Current regulation accuracy is dominated by gain error at high current settings, and offset error at low current settings. The range of expected fast-charge output current versus programming resistance R_{IPRGM} is shown in Figures 1a and 1b. Each figure shows the nominal fast-charge current versus nominal R_{IPRGM} resistance as the center plot, and two theoretical limit plots indicating maximum and minimum current versus nominal programming resistance. These plots are derived from models of the expected worst-case contribution of error sources depending on programmed current. The current range includes the uncertainty due to 1% tolerance resistors. The dots on each plot indicate the currents obtained with the Electronic Industries Association (EIA) E96 standard value 1% tolerance resistors. Figures 1a and 1b show low and high resistance ranges, respectively. The USB low power mode fast-charge current accuracy is exactly like that of pre-charge in high power mode. USB low power mode current regulation accuracy is described in the next section.

Pre-charge and USB Low Power Mode Fast-charge Current Regulation

Pre-charging is automatically selected when the battery voltage is below the pre-charge threshold voltage (VT_{PreQ}). Pre-charge current conditions the battery for fast charging. The pre-charge current value is fixed at 20% of the programmed fast-charge current. Note that USB low power mode pre-charge current is equal to USB low power mode fast-charge current.

Pre-charge current regulation accuracy is dominated by offset error. The range of expected pre-charge output current versus programming resistance R_{IPRGM} is shown in Figures 2a and 2b. Each figure shows the nominal pre-charge current versus nominal R_{IPRGM} resistance as the center plot and two theoretical limit plots indicating maximum and minimum current versus nominal programming resistance. These plots are derived from models of the expected worst-case contribution of error sources depending on programmed current. The current range includes the uncertainty due to 1% tolerance resistors. The dots on each plot indicate the currents obtained with EIA E96 standard value 1% tolerance resistors. Figures 2a and 2b show low and high resistance ranges, respectively.

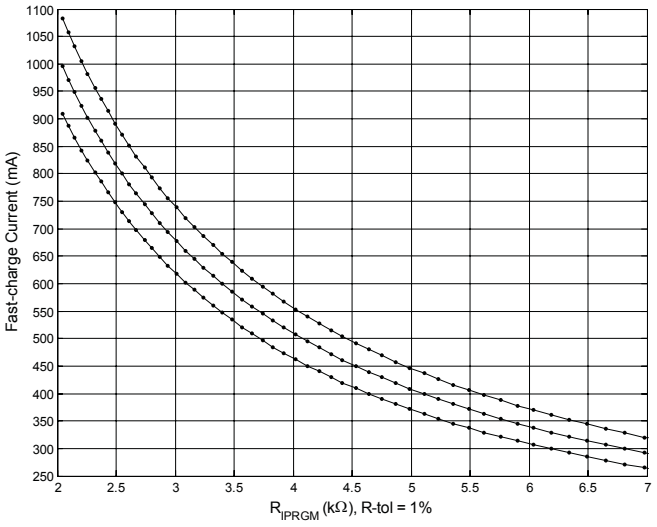


Figure 1a — Fast-charge Current Tolerance versus Programming Resistance, Low Resistance Range

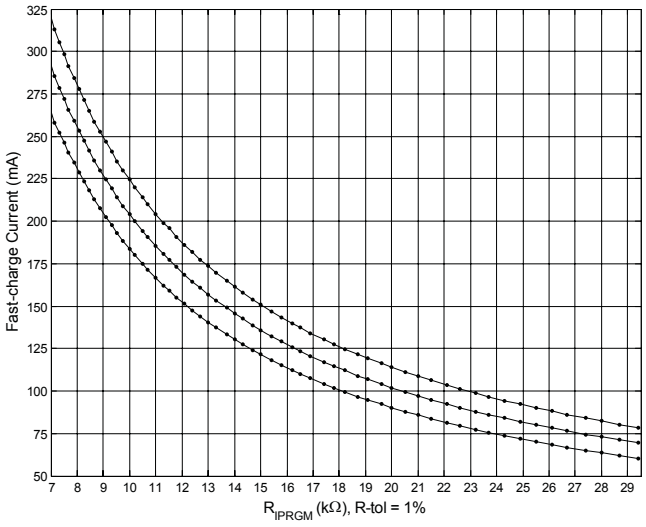


Figure 1b — Fast-charge Current Tolerance versus Programming Resistance, High Resistance Range

Applications Information (continued)

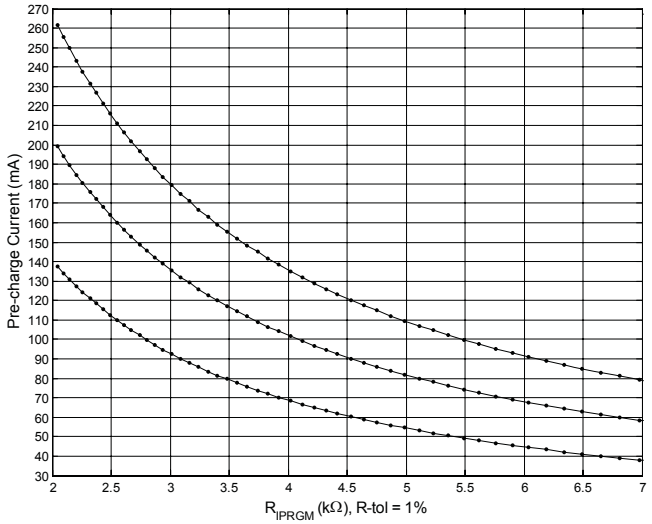


Figure 2a — Pre-charge Current and USB Low Power Mode Fast-charge Current Tolerance vs. Programming Resistance, Low Resistance Range

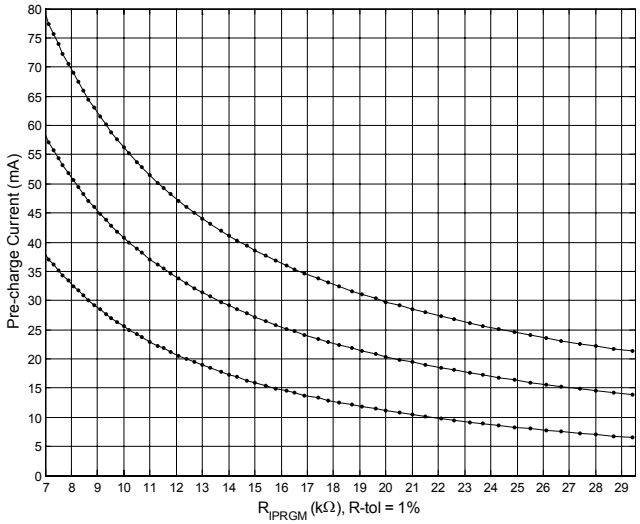


Figure 2b — Pre-charge Current and USB Low Power Mode Fast-charge Current Tolerance vs. Programming Resistance, High Resistance Range

Termination

When the battery voltage reaches V_{CV}, the SC824 transitions from constant current regulation to constant voltage regulation. The current into the battery decreases while the BAT voltage is regulated to V_{CV} as the battery becomes fully charged. When the output current drops below the termination current threshold, charging terminates. Upon termination, the charger either enters monitor state or float charges the battery for the top-off timer duration, depending on the configuration of the charge timer. After a 20 second delay following termination, the STAT1 pin open drain output turns off.

The termination current threshold is fixed at 10% of the fast-charge current, as programmed by the IPRGM pin resistance to ground, for all charging modes.

Charger output current is the sum of the battery charge current and the system load current. Battery charge current changes gradually and establishes a slowly diminishing lower bound on the output current while charging in CV regulation. The load current into a typical digital system is highly transient in nature. Charge cycle termination is detected when the sum of the battery charging current and the greatest load current occurring within the immediate 300µs to 550µs past interval is less than the programmed termination current. This timing behavior permits charge cycle termination to occur during a brief low-load-current interval, and does not require that the longer interval average load current be small.

Termination current threshold accuracy is dominated by offset error. The range of expected termination current versus programming resistance R_{IPRGM} (for any charging mode) is shown in Figures 3a and 3b. Each figure shows the nominal termination current versus nominal R_{IPRGM} resistance as the center plot and two theoretical limit plots indicating maximum and minimum current vs. nominal programming resistance. These plots are derived from models of the expected worst-case contribution of error sources depending on programmed current. The current range includes the uncertainty due to a 1% tolerance resistor. The dots on each plot indicate the currents obtained with EIA E96 standard value 1% tolerance resistors. Figures 3a and 3b show low and high resistance ranges, respectively.

Monitoring Output Current

The output current I_{BAT} is indicated by the voltage at the IPRGM pin according to the following equation.

$$I_{BAT} = \frac{V_{IPRGM}}{R_{IPRGM}} \times 1000$$

Ensure that the IPRGM pin is not loaded or corrupted by the processor Analog to Digital Converter (ADC). An RC

Applications Information (continued)

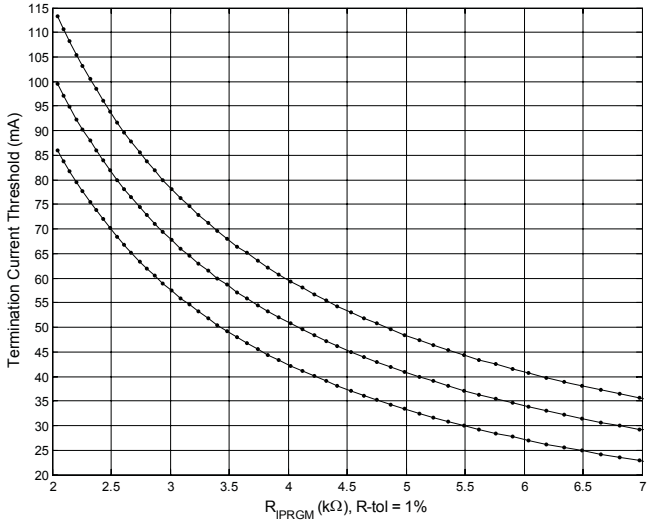


Figure 3a — Termination Current Tolerance vs. Programming Resistance, Low Resistance Range

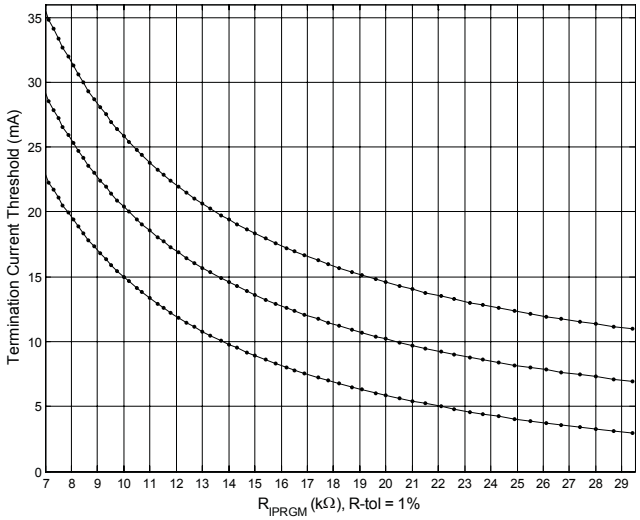


Figure 3b — Termination Current Tolerance vs. Programming Resistance, High Resistance Range

filter (R at least 100×R_{IPRGM}, C large compared to the Sample-and-Hold capacitance of the ADC) can prevent corruption of the IPRGM pin voltage by the ADC. Any noise introduced onto the IPRGM pin will be seen as current noise at the SC824 output during CC regulation, and can introduce errors in the termination current.

The IPRGM pin will see a brief (<1ms) pulse whenever the charger turns on, just prior to enabling the output. This pulse is part of the startup IPRGM pin-short (to ground) test. When the charger first turns on, the processor should allow time for this pulse prior to reading the IPRGM voltage. See the section Short Circuit Protection.

MODE Pin Tri-level Logical Input

The MODE pin is designed to interface to a processor GPIO port that is powered from a peripheral supply voltage as low as 1.8V or as high as a fully charged battery. The processor writes 0 to select MODE low-range, and 1 to select high-range. The GPIO port is configured as an input to select mid-range.

While driven high (V_{MODE} > Min V_{IH}), the SC824 will operate in USB High Power mode. While the MODE input voltage is within its specified mid range (Min V_{IM} < V_{ENB} < Max V_{IM}), either by floating (by reconfiguring its GPIO as an input) or by being externally forced, the SC824 will operate in USB Low Power mode. While driven low (V_{MODE} < Max V_{IL}), the SC824 will operate in adapter mode.

When no charging source is present, while the charger is disabled, or while operating in the monitor state (described in a later section), the MODE pin enters a high impedance state, suspending the tri-level functionality. Upon recharge or re-enabling the charger, the MODE pin tri-level interface is reactivated.

While the tri-level interface is active, the equivalent circuit looking into the MODE pin is a variable resistance, minimum 15kΩ, to an approximately 1V source. The input will float to mid range whenever the external driver sinks or sources less than 5µA. This is a common worst-case characteristic of a high impedance GPIO, or a weak pull-up or pull-down GPIO, configured as an input. The driving GPIO must be able to sink or source at least 75µA to ensure a low or high state, respectively, although the drive current required is typically far less. (See the electrical characteristics table.) Typically a processor GPIO port direction defaults to input upon processor reset, or is high impedance when unpowered. This is the ideal initial condition for driving the MODE pin, since this will select USB Low Power mode, which is the safest default mode with the lowest fast charge current.

For fixed mode operation, this pin can be permanently grounded to select low-range, left unconnected to select mid-range, or permanently connected to a logical high voltage source, such as BAT or a regulated peripheral supply voltage, to select high-range.

Applications Information (continued)

Monitor State

Upon termination (charge timer disabled) or time-out of the top-off timer (charge timer enabled), the charger will enter the monitor state. If the battery voltage falls below the recharge threshold (V_{CV} - V_{ReQ}) while in the monitor state, the charger will automatically initiate a re-charge cycle. This operation will turn on the charger output, but will not assert the STAT1 output. A recharge cycle is subject to normal timer operation if the timer is enabled. The battery leakage current during monitor state is no more than 1µA over temperature and typically less than 0.1µA at room temperature.

The SC824 can be forced out of the monitor state by disabling and re-enabling the charger using the EN_NTC pin. This operation will initiate a new charge cycle. This forced re-charge behavior can be used for periodically testing the battery state-of-charge and topping off the battery without requiring the battery to discharge to the automatic re-charge voltage. A single CPU instruction cycle is a sufficient disable hold-time to initiate a re-charge cycle.

Following termination, the host processor can schedule a forced re-charge at any desired interval. Forced re-charge will assert the STAT1 output, which will remain on for 20 seconds following termination, regardless of whether the charge timer is enabled.

VSYS pin

The voltage of the VSYS pin is regulated from the VIN input and is present only when VIN is powered. A capacitor of at least 1µF should be connected from VSYS to ground near the pin. Capacitance must be rated at the expected bias voltage of 4.6V.

The internal CC timer is selected when the RTIME pin is connected to VSYS. VSYS provides an external voltage reference and supply for the NTC network. The total external load on the VSYS pin should not exceed 1mA.

EN_NTC Interface

The EN_NTC pin is the interface to a battery pack temperature sensing Negative Temperature Coefficient (NTC) thermistor, which can be used to suspend charging if the battery pack temperature is outside of a safe-to-charge range. The EN_NTC interface also often serves as a charger disable input and as a battery removal detector.

The recommended EN_NTC network is a fixed-value pull-up resistor (designated R_{NPU}) from the EN_NTC pin to the VSYS pin, and the battery pack NTC thermistor (designated R_{NTC}) from the EN_NTC pin to ground. In this configuration, an increasing battery temperature produces a decreasing NTC pin voltage.

When V_{EN_NTC} is greater than the high (cold) threshold (but below the No-Battery detector threshold) or less than the low (hot) threshold (but above the disable threshold), the charge cycle is suspended by turning off the output. This suspends but does not reset the charge timer, in any timer stage, and a charging fault is indicated by asserting (pulling low) STAT1 and releasing STAT0. Hysteresis is included for both high and low NTC thresholds to avoid chatter at the NTC temperature fault thresholds. When V_{EN_NTC} returns to the Temperature-OK-to-Charge range, the charge timer resumes, STAT0 and STAT1 are asserted, and the charge cycle continues. The charge timer will expire when the output on-time exceeds the timer setting, regardless of how long it has been disabled due to an NTC fault.

All EN_NTC input thresholds are proportional to the VSYS pin voltage (V_{VSYS}). See the Block Diagram. When the recommended external NTC circuit shown in the Block Diagram is used, the external EN_NTC pin voltage is also proportional to V_{VSYS}, with the proportionality varying with the thermistor resistance. This ensures that all EN_NTC thresholds are insensitive to V_{VSYS}. The ratiometric hot and cold thresholds are given by the parameters RT_{NTC_HF} and RT_{NTC_CR}. EN_NTC pin voltage V_{EN_NTC} between $RT_{NTC\_HF} \times V_{VSYS}$ and $RT_{NTC\_CR} \times V_{VSYS}$ enables charging. See Table 1.

Table 1 — EN_NTC Pin Ratiometric Thresholds

	% of V_{VSYS}	Range
V_{EN_NTC} Ratiometric Thresholds		No-Battery
	RT_{NTC_NBR} = 95%	NTC Cold Fault
	RT_{NTC_CR} = 75%	NTC Temperature-OK-to-Charge
	RT_{NTC_HF} = 30%	NTC Hot Fault
	RT_{NTC_DIS} = 10%	Charger Disabled

Applications Information (continued)

When $V_{EN\_NTC} < RT_{NTC\_DIS} \times V_{VSYS}$ (nominally 10% of V_{VSYS}), the SC824 charger is disabled. This threshold allows the EN_NTC pin to be used as a disable pin, allowing the system controller to asynchronously disable or reset the device by pulling EN_NTC to ground. When $V_{EN\_NTC} < RT_{NTC\_DIS} \times V_{VSYS}$, the charger is turned off, the charge timer is reset, and the STAT1 status output is turned off. While disabled, the VIN input UVLO and OVP threshold detectors remain active, and the STAT0 pin continues to indicate whether the VIN input voltage is valid for charging.

No-Battery operation is selected when the battery (along with the thermistor) is removed, determined by the NTC pin exceeding $RT_{NTC\_NBR} \times V_{VSYS}$, which is 95% of the VSYS pin voltage. In No-Battery operation, the charge timer is disabled and the output is regulated to V_{CV}, subject to the output current limit determined by the selected mode and IPRGM pin resistance to GND. The STAT0 output remains asserted to indicate that the charging source is present and STAT1 is released. When returning to normal charging (by reinstalling the battery and thermistor), the timer is reset.

The response of the SC824 to an EN_NTC pin voltage above the NTC Cold Fault threshold (but below RT_{NTC_NBR}) or below the low NTC Hot Fault threshold (but above VT_{NTC_DIS}) is the same. Therefore the EN_NTC network can be configured with the battery pack thermistor between EN_NTC and VSYS, and a fixed resistor between EN_NTC and ground, reversing the designation of the hot and cold thresholds. This configuration may be used to disable the charger when the battery pack is removed.

For detailed design guidance for ratiometric NTC interfaces, including thermistor selection guidelines, see the Semtech Application Note AN–PM–0801, *NTC Thermistor Network Design for Ratiometric Thresholds*.

Charge Timer

The SC824 provides a multi-stage charge timer. Each stage of the charge cycle is timed separately, in compliance with IEEE Std. 1725-2006, Section 7.3.5.

The pre-charge stage timer indicates a fault and halts charging if the battery voltage has not exceeded the pre-charge threshold within 45 minutes after the start of the charge cycle. The pre-charge stage timer is active even if the timer function has been disabled.

When the battery voltage exceeds the pre-charge threshold, the timer is reset and begins timing the CC stage. The CC stage timer indicates a fault and halts charging if the battery voltage has not reached V_{CV} within the CC stage fault timer duration (t_{CCF}). The CC stage timer is not active if the timer function has been disabled.

An internally programmed CC stage duration of three hours can be selected by connecting RTIME directly to VSYS. Or it can be programmed from two hours to 16 hours by selection of the resistance from the RTIME pin to ground, as shown in the Block Diagram. The broad CC stage timer programming range permits timer-protected charging of large batteries with small charging currents, such as in USB low power mode charging.

The value of t_{CCF} is programmed according to Figures 4a and 4b. Each figure shows the nominal t_{CCF} duration versus nominal R_{RTIME} resistance as the center plot and two theoretical limit plots indicating maximum and minimum t_{CCF} duration versus nominal programming resistance. These plots are derived from models of the expected worst-case contribution of error sources that depend on programmed current. The t_{CCF} tolerance range includes the uncertainty due to 1% tolerance resistors. The dots on each plot indicate the currents obtained with EIA E96 standard value 1% tolerance resistors. Figures 4a and 4b show low and high resistance ranges, respectively.

When the battery voltage has risen to V_{CV}, the CC timer stage ends, the timer is reset, and the CV timer stage begins. The CV stage timer is set to expire in three hours using a fixed-duration internal timer. Upon termination by current (10% of fast charge current) or expiration of the CV stage timer (whichever occurs first), end-of-charge is indicated by releasing STAT1 and the timer is reset. Note that CV stage time-out is not a fault, but rather is regarded as termination by another means. This alternative termination-by-time behavior ensures termination in the case that the minimum load current exceeds the programmed termination current.

Following termination, by current or by timer CV stage time-out, the post-termination top-off timer stage begins.

Applications Information (continued)

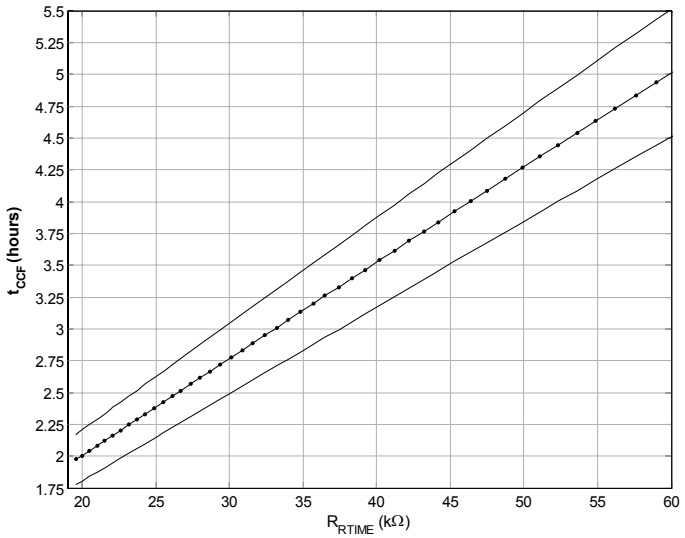


Figure 4a — CC Stage Fault Timeout vs. Programming Resistance, Low Resistance Range

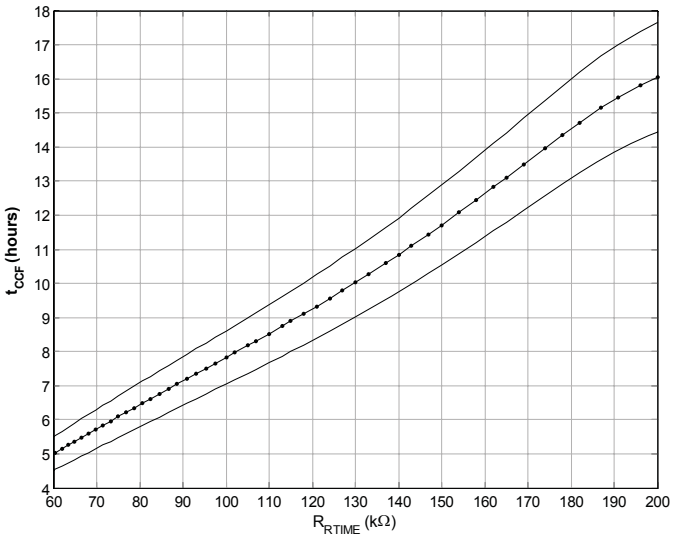


Figure 4b — CC Stage Fault Timeout vs. Programming Resistance, High Resistance Range

Top-off charging maintains the BAT pin voltage at V_{CV} by acting as a voltage regulator until the time-out of the top-off timer. The top-off timer times-out in 45 minutes, at which time the charger is turned off and enters the monitor state.

The charge timer is disabled when the RTIME pin is grounded. In this case, the output is turned off immediately upon current termination and the charger enters the monitor state. Note that the pre-charge stage timer will be active regardless of whether the RTIME pin is grounded, to detect a grossly defective battery or output short to ground. A pre-charge timeout will signal a fault and turn off the charging output.

During the CC timer interval, momentarily grounding (at least 300µs) and releasing the RTIME pin will reset the CC mode timer. This feature allows the CC mode timer to be used as a watchdog timer, enabling the host processor to extend the CC interval as long as needed for charging a large battery with a low fast-charge current.

While the charger is in the top-off interval and the timer is enabled, the RTIME pin can be grounded momentarily (at least 300µs) to immediately end the charging cycle and place the charger in the monitor state. In this condition, the charge timer remains enabled for operation in a subsequent recharge cycle.

An NTC temperature fault will suspend but will not reset the charge timer, in any timer stage. The timer resumes from its current state when the battery temperature returns to the safe-to-charge range.

See the section Logical State Machine for details of timer stage transitions and sequencing.

Status Outputs

The STAT0 and STAT1 pins are open-drain status indicating outputs. STAT0 is asserted (driven low) whenever a valid charging source is present at the VIN input pin. A valid charging source has a voltage greater than the UVLO threshold and less than the OVP threshold.

STAT1 is asserted as charging begins and is subsequently released upon charge termination (by CV stage timeout or by charge current) to indicate end-of-charge. It is also released when the charger is disabled and in No-Battery mode. If the battery is already fully charged when a charge cycle is initiated, STAT1 is asserted and will remain asserted for approximately 22 seconds before being released. The STAT1 pin is not asserted for automatic recharge cycles.

The STAT0 and STAT1 pins may be connected to processor GPIO ports to notify a host controller of the charging status, or they can be used as LED drivers. Both are high voltage inputs, so they can be safely pulled up to the input

Applications Information (continued)

supply to power LEDs. The conditions indicated by STAT0 and STAT1 are summarized in Table 2.

Table 2 — STATx Pin Truth Table

Condition	STAT0	STAT1
Power applied ($VT_{UVLO} < V_{VIN} < VT_{OVP}$), prior to charging	0 (asserted)	1 (released)
Charging	0 (asserted)	0 (asserted)
Charging Done, any stage of a recharge cycle, or No-Battery Mode	0 (asserted)	1 (released)
Charging Fault (Pre-charge or CC time-out, NTC temperature fault, IPRGM pin short to ground)	1 (released)	0 (asserted)
No valid input supply	1 (released)	1 (released)

The STAT0 and STAT1 outputs indicate charging faults by asserting STAT1 while releasing STAT0. Charging faults include pre-charge or CC-stage timeout, a battery NTC temperature fault (hot or cold), and the shorting of the IPRGM pin to ground.

Charging status is indicated during precharge, CC charging, and CV charging until termination. Top-off charging is not indicated. Upon termination, whether the timer is enabled or disabled, charging status will be indicated for an additional 22 seconds, either while top-off charging with the timer enabled, or while in monitor state with the output off if the timer is disabled. This feature ensures that "charging" will be indicated long enough to be seen, even if the adapter voltage is applied when the battery is already fully charged. It informs the user that a charge cycle was begun and completed normally. Note that the SC824 can terminate charging of a fully charged battery in as little as a millisecond; without this feature the "charging" indication would not be visible.

Logical CC-to-CV Transition

The SC824 differs from monolithic linear single cell Li-Ion chargers that implement a linear transition from CC to CV regulation. The linear transition method uses two simultaneous feedback signals — output voltage and output current — to the closed-loop controller. When the output voltage is sufficiently below the CV regulation voltage, the influence of the voltage feedback is negligible and the output current is regulated to the desired current. As the battery voltage approaches V_{CV} (nominally 4.2V), the voltage feedback signal begins to influence the control loop, which causes the output current to decrease even though the output voltage has not yet reached V_{CV}. The output voltage limit dominates the controller when the battery reaches V_{CV}, and eventually the controller is entirely in CV regulation. The soft transition effectively reduces the charge current below that which is permitted for a portion of the charge cycle, which increases charge time.

The SC824 uses a logical transition from CC to CV to recover the charge current lost due to a soft transition. The controller regulates only current until the output voltage exceeds the transition threshold voltage. It then switches to CV regulation. The transition voltage from CC to CV regulation is typically 7mV higher than the CV regulation voltage, which provides a sharp and clean transition free of chatter between regulation modes. The difference between the transition voltage and the regulation voltage is referred to as the CC/CV overshoot. While in CV regulation, the output current sense remains active. If the output current exceeds the mode-dependent programmed fast-charge current by approximately 5%, the controller reverts to current regulation.

The logical transition from CC to CV results in a faster charging cycle that is compliant with the specified current and voltage limits of the Li-Ion cell. The output current is constant at the CC limit, then decreases abruptly when the output voltage steps from the overshoot voltage to the regulation voltage at the transition to CV control.

Thermal Limiting

Device Thermal Limiting (TL) is the third output constraint of the CC/CV/TL control. This feature permits a higher input OVP threshold in the SC824, and thus the use of higher regulation voltage or poorly regulated adapters. If high input voltage results in excessive power dissipation, the output current is reduced to prevent overheating of the SC824. The thermal limiting controller reduces the output current at the rate of $i_T \approx -50mA/^oC$ for any junction temperature $T_J > T_{TL}$.

Applications Information (continued)

When thermal limiting is inactive,

$$T_J = T_A + V_\Delta I_{FQ} \theta_{JA},$$

where T_A is the ambient temperature, V_Δ is the voltage difference between the VIN pin and the BAT pin, I_{FQ} is the programmed fast charge current, and θ_{JA} is the thermal resistance from junction to ambient. However, if T_J computed this way exceeds T_{TL}, then thermal limiting will become active and the thermal limiting junction temperature will be

$$T_{JTL} = T_A + V_\Delta I(T_{JTL}) \theta_{JA},$$

where

$$I(T_{JTL}) = I_{FQ} + i_T (T_{JTL} - T_{TL}).$$

(Note that i_T is a negative quantity.) Combining these two equations and solving for T_{JTL}, the steady state junction temperature during active thermal limiting is

$$T_{JTL} = \frac{T_A + V_\Delta (I_{FQ} - i_T T_{TL}) \theta_{JA}}{1 - V_\Delta i_T \theta_{JA}}.$$

The thermal limiting controller is able to reduce output current to zero. However, this does not happen in practice. Output current is reduced to $I(T_{JTL})$, reducing power dissipation such that die temperature equilibrium T_{JTL} is reached.

While thermal limiting is active, all charger functions remain active and the charger logical state is preserved.

See the section Input Over-Voltage Protection for an example of thermal limiting operation.

Operating a Charging Adapter in Current Limit

In high charging current applications, charger power dissipation can be greatly reduced by operating the charging adapter in current limit. The SC824 supports adapter-current-limited charging with a low UVLO falling threshold and with internal circuitry designed for low input voltage operation. To operate an adapter in current limit, R_{IPRGM} is chosen such that the programmed fast-charge current I_{FQ} exceeds the current limit of the charging adapter I_{AD-LIM}. The charging load will pull the adapter output voltage (the VIN pin input voltage) down to the battery voltage plus the charger dropout voltage. Power dissipation in the SC824 will be reduced to the charger dropout voltage multiplied by I_{AD-LIM}.

If I_{AD-LIM} is less than 20% of I_{FQ}, then the adapter voltage can be pulled down to the battery voltage while the battery voltage is still below the precharge threshold. In this case, ensure that the adapter will maintain its current limit below 20% of I_{FQ} at least until the battery voltage exceeds the precharge threshold. Failure to do so could permit charge current to exceed the precharge current while the battery voltage is below the precharge threshold. This is because the low input voltage can also compress the precharge threshold internal reference voltage to below the battery voltage. This will prematurely advance the charger logic from precharge current regulation to fast-charge regulation, and the charge current will be permitted, by the charger, to exceed the safe level recommended for pre-charge conditioning.

The low UVLO falling threshold (VT_{UVLO-F}) permits the adapter voltage to be pulled down to just above the battery voltage only in adapter mode (MODE pin grounded). In either USB mode, Under-Voltage Load Regulation (UVLR) prevents the input being pulled down by the charging current to below the UVLR limit of V_{UVLR} = 4.51V typically.

The SC824 should be operated with the adapter voltage below the rising selection threshold (VT_{UVLO-R}) only if the low input voltage is the result of adapter current limiting. This implies that the VIN pin voltage first exceeds VT_{UVLO-R} to begin charging and is subsequently pulled down by the charging current to just above the battery voltage.

Interaction of Thermal Limiting and CLA Charging

To permit the charge current to be limited by the adapter, it is necessary that the adapter mode fast-charge current be programmed greater than the maximum adapter current, (I_{AD-LIM}). In this configuration, the CC regulator will operate with its pass device fully on (in saturation, also called "dropout"). The voltage drop from VIN to BAT is determined by the R_{DS-ON} of the internal pass device multiplied by the adapter current.

Applications Information (continued)

In dropout, the power dissipation in the SC824 is $P_{ILIM} = (R_{DS-ON}) \times (I_{AD-LIM})^2$. Since R_{DS-ON} does not vary with battery voltage, dropout power dissipation is constant throughout the CC portion of the charge cycle while the adapter remains in current limit. The SC824 junction temperature will rise above ambient by $P_{ILIM} \times \theta_{JA}$. If the device temperature rises to the temperature at which the TL control loop limits charging current (rather than the current being limited by the adapter), the input voltage will rise to the adapter regulation voltage. The power dissipation will increase so that the TL regulation will further limit charge current. This will keep the adapter in voltage regulation for the remainder of the charge cycle. In this case, the SC824 will continue to charge with thermal limiting until charge current decreases while in CV regulation (reducing power dissipation sufficiently), resulting in a slow charge cycle, but with no other negative effect.

To ensure that the adapter remains in current limit, the internal device temperature must never rise to T_{TL}. This implies that θ_{JA} must be kept small enough, through careful layout, to ensure that $T_J = T_A + (P_{ILIM} \times \theta_{JA}) < T_{TL}$.

Under-Voltage Load Regulation in USB Modes

The VIN pin UVLR feature, enabled in either USB mode, prevents the battery charging current from overloading the USB Vbus network, regardless of the programmed fast charge value (I_{FQ_USB}). When either USB High Power or USB Low Power mode is selected, the SC824 monitors the input voltage (V_{VIN}) and reduces the charge current by the amount necessary to keep V_{VIN} no lower than the UVLR limit (V_{UVLR}). UVLR is active only when one of the USB modes is selected. UVLR ensures the integrity of the USB Vbus supply for all devices sharing a host or hub supply.

In either USB mode, the UVLR feature will reduce the charging current to zero if V_{VIN} is externally pulled below V_{UVLR}. This condition will not be interpreted as termination and will not result in an end-of-charge indication. The STAT1 pin will remain asserted as if charging is continuing. This behavior prevents repetitive indications of end-of-charge alternating with start-of-charge in the case that the external VIN load is removed or is intermittent. STAT0 remains asserted until the input voltage is less than VT_{UVLO-F}.

USB High Power and Low Power Support

The USB specification restricts the load on the USB Vbus power network to 100mA for low power devices and for high power devices prior to granting permission for high power operation. The USB specification restricts the Vbus load to 500mA for high power devices after granting permission to operate as a high power device. A fixed 1:5 ratio of low power to high power charging current is desirable for charging batteries with maximum fast charge current of at least 500mA. For this application, the SC824 provides fixed 1:5 current ratio low-to-high power mode support via the tri-level MODE input pin.

For batteries with maximum fast charge current less than 500mA, a fixed 1:5 low/high power charge current ratio will result in suboptimal charging in USB low power mode. For example, a 300mAh battery will typically require a fast-charge current of 300mA or less. A fixed 1:5 ratio for USB low-to-high power charging current will unnecessarily reduce charging current to 60mA, well below the 100mA permitted. In this case, it may be preferable to program USB low-power fast-charge current by switching an external programming resistor. See the section Design Considerations — Small Battery.

Input Over-Voltage Protection

The VIN pin is protected from over-voltage to at least 30V above GND. When the input voltage exceeds the Over-Voltage Protection rising threshold (VT_{OVP-R}), charging is halted. Charging resumes when the input voltage falls below the OVP falling threshold. OVP turns off the STAT0 and STAT1 outputs.

All modes use the same input OVP threshold, which has been set relatively high to permit the use of poorly regulated adapters. Such adapters may output a high voltage until loaded by the charger. A too-low OVP threshold could prevent the charger from ever turning on and loading the adapter to a lower voltage. If the adapter voltage remains high despite the charging load, the fast thermal limiting feature will immediately reduce the charging current to prevent overheating of the charger. This behavior is illustrated in Figure 5, in which $V_{BAT} = 3.0V$, $I_{FQ} = 700mA$, and V_{VIN} is stepped from 0V to 8.1V. Initially, power dissipation in the SC824 is 3.6W.

Applications Information (continued)

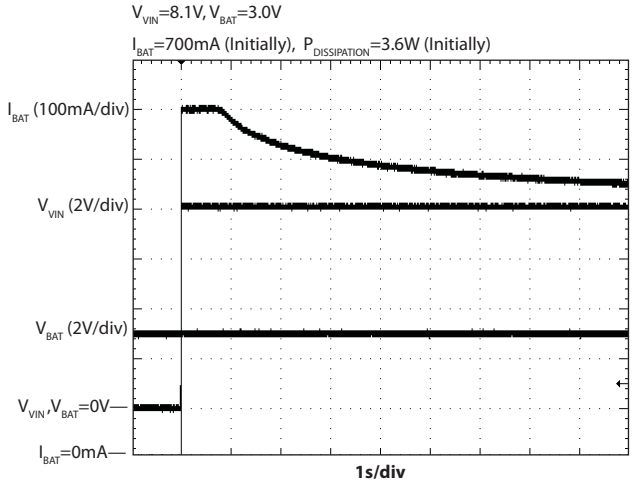


Figure 5 — Thermal Limiting Example

Note that the BAT output current is rapidly reduced to limit the internal die temperature. It then continues to decline as the circuit board temperature gradually rises, further reducing the conduction of heat from the die to the ambient environment. The fast thermal limiting feature ensures compliance with CCSA YD/T 1591-2006, *Telecommunication Industrial Standard of the People's Republic of China — Technical Requirements and Test Method of Charger and Interface for Mobile Telecommunication Terminal*, Section 4.2.3.1.

Short Circuit Protection

The SC824 can tolerate a BAT pin short circuit to ground indefinitely. The current into a ground short (while V_{BAT} < 1.8V) is approximately 10mA. For V_{BAT} > 1.8V, normal pre-charge current regulation is active.

A short circuit or too little programming resistance to ground on the IPRGM pin (<< 2kΩ) will prevent proper regulation of the BAT pin output current. Prior to enabling the output a check of the IPRGM pin is performed to ensure that there is sufficient resistance to ground. A test current is output on the IPRGM pin. If the test current produces a voltage of sufficient amplitude, then the output is enabled. An example with R_{IPRGM} = 2.94kΩ is illustrated in Figure 6, in which the test current is applied for approximately 250µs to determine that there is no pin short. If a short is detected, the test current persists until the short to ground is removed, and then the charging startup sequence will continue.

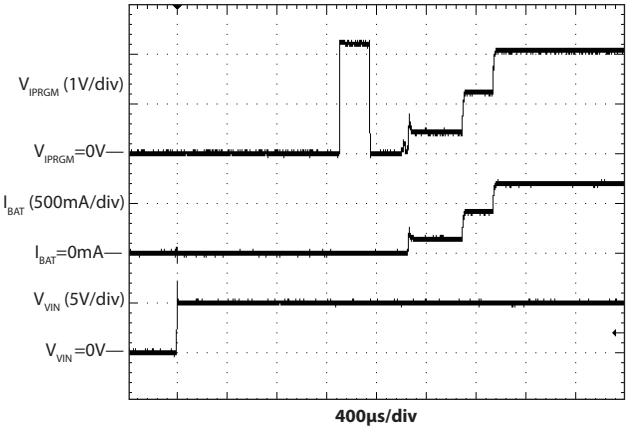


Figure 6 — IPRGM Pin Short-to-Ground Test During Startup

A short to ground applied to the IPRGM pin while charging will also be detected, by a different mechanism. IPRGM pin short-to-ground detection on the IPRGM pin forces the SC824 into reset, turning off the output and clearing the logical state, including the timer.

A short-to-ground on the IPRGM pin will halt charging and prevent startup regardless of the mode selected. It is indicated as a fault condition on the STATx pins. When the IPRGM ground short is removed, the charger begins normal operation automatically without input power cycling.

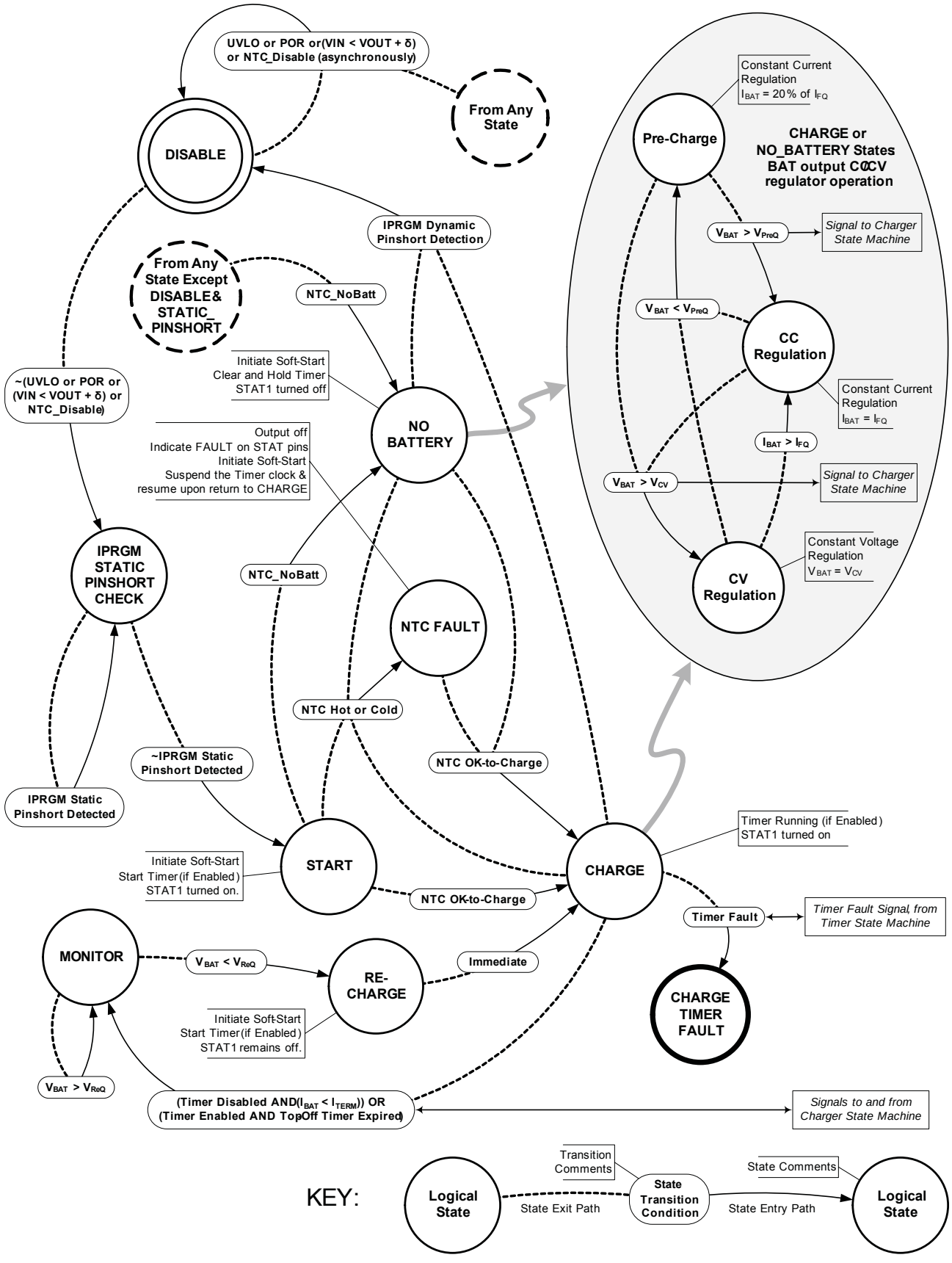
Over-Current Protection

Over-current protection is provided in all modes of operation, including CV regulation. The output current is limited to the programmed pre-charge current limit value when the battery voltage is below the pre-charge threshold and the fast-charge current limit value otherwise.

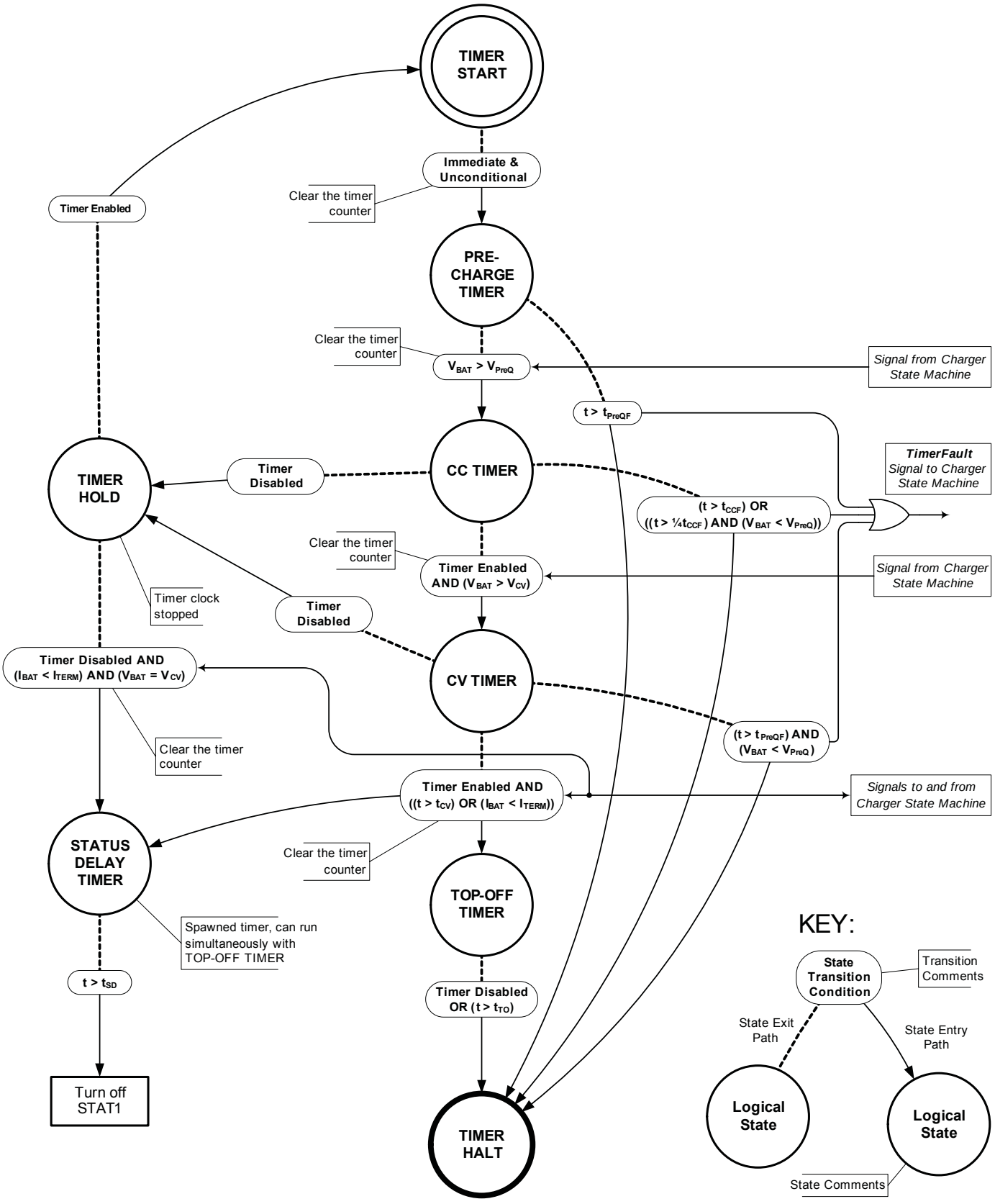
Logical State Machine

The SC824 logical behavior described in the preceding sections is derived from two distinct state machines, as illustrated in the following diagrams. The charger state machine permits transitions to most states from most other states, as shown. The multi-stage timer state machine enforces a unidirectional flow. Once the timer has advanced from one stage to the next, there is no return to the previous stage except by a re-charge cycle, a reset (by disabling and re-enabling the SC824), or by cycling the input power off and on.

Applications Information (continued) — Charger Logical State Machine



Applications Information (continued) — Multi-stage Timer Logical State Machine



Applications Information (continued)

Operation Without a Battery

The SC824 can be operated as a 4.2V LDO regulator without the battery present, for example, for factory testing. If this use is required, the total output capacitance, C_{BAT} plus any other capacitors tied directly to BAT pin network, should be at least 2.2µF but less than 22µF to ensure stability in CV regulation. To operate the charger without a battery, the NTC pin should be pulled up to the VSYS voltage to select No-Battery mode. This can be accomplished automatically when a battery is absent if the recommended NTC network is used. See the section EN_NTC Interface for details.

Capacitor Selection

Low cost, low ESR ceramic capacitors such as the X5R and X7R dielectric material types are recommended. The BAT pin capacitor should be at least 1µF, but can be as large as desired to accommodate the required input capacitors of regulators connected directly to the battery terminal. BAT pin total capacitance must be limited if the SC824 is to be operated without the battery present. See the section Operation Without a Battery. The VIN pin capacitor is typically between 0.1µF and 2.2µF, although larger values will not degrade performance. The VSYS pin capacitor must be at least 1µF. Capacitance must be rated at the expected bias voltage (4.2V for the BAT pin capacitor, 4.6V for the VSYS pin capacitor, the expected V_{VIN} supply regulation voltage for the VIN pin capacitor), rather than the zero-volt capacitance rating.

PCB Layout Considerations

Layout for linear devices is not as critical as for a switching regulator. However, careful attention to detail will ensure reliable operation.

- Place input and output capacitors close to the device for optimal transient response and device behavior.
- Connect all ground connections directly to the ground plane. If there is no ground plane, connect to a common local ground point before connecting to board ground near the GND pin.
- Attaching the device to a larger copper footprint will enable better heat transfer from the device on PCBs with internal ground and power planes.

Design Considerations — Large Battery

A battery with a desired fast-charge current exceeding 500mA is most compatible with the USB fixed 1:5 current ratio low-to-high power model of operation. For example, consider an 800mAhr battery, with maximum fast-charge current of 800mA. The adapter input fast-charge should be configured for 800mA max (R_{IPRGM} = 2.78kΩ equivalent is required). Select R_{IPRGM} = 4.53kΩ to set USB high power fast-charge to 450mA, and the USB low power fast-charge set to 450/5 = 90mA. The MODE pin tri-level logical input can be used to select between USB high power and USB low power modes whenever a fixed 5:1 current ratio is desired. For adapter mode charging, set the MODE pin high for USB high power mode if UVLR is desired, or low for adapter mode if current limited adapter capability is desired. Then switch in a parallel 7.15kΩ IPRGM resistor, as shown in Figure 7, for an equivalent 2.77kΩ IPRGM resistance. This will program the desired 800mA max adapter mode fast charge current.

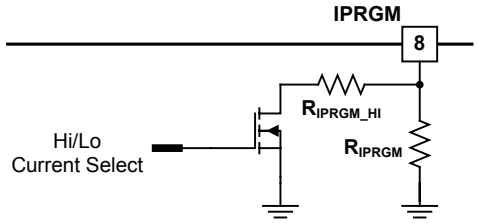


Figure 7 — External Programming of Arbitrary USB High Power and Low Power Charge Currents

Design Considerations — Small Battery

A battery with a desired fast-charge current less than 500mA will not be charged in the minimum charge time when in USB low power mode with a 1:5 low-to-high power mode current ratio. A 300mAhr battery can be used as an example with maximum fast-charge current of 300mA. In this example, the adapter input and USB input high power fast-charge currents should both be set to 300mA. In this case, the fixed USB low-to-high power charging current ratio of 1:5 would provide a USB low power mode fast charge current of 60mA.

For this example, setting the USB low power fast-charge current to 90mA would provide a shorter charge time without violating USB Vbus current requirements. An arbitrary ratio of USB low-to-high power charging currents can be obtained using an external n-channel FET operated with a processor GPIO signal to engage a second

Applications Information (continued)

parallel IPRGM resistor, while selecting high power mode (MODE pin driven high) for both low or high power USB charging. The external circuit is similar to that illustrated in Figure 7.

For USB low power mode charging, the external transistor is turned off. For adapter mode or USB high power mode, the external transistor is turned on. The effect of the switched parallel IPRGM resistor is to reduce the effective programming resistance and thus raise the fast-charge current.

A 300mAhr battery with maximum fast-charge current of 300mA is an example. The adapter mode and USB high power mode fast-charge currents should both be set to 300mA max. The USB input low power fast-charge current is 100mA max. Refer to the circuit in Figure 7 and the data of Figures 1a and 1b. For I_{FQ} = 300mA max, R_{IPRGM} = 7.50kΩ is desired. A fixed IPRGM resistor of R_{IPRGM} = 23.2kΩ programs I_{FQ} = 100mA max for USB low power charging. When parallel resistor R_{IPRGM_HI} = 11.0kΩ is switched in, the equivalent IPRGM resistor is 7.50kΩ, for I_{FQ} = 300mA max.

USB Low Power Mode Alternative

Where a USB mode selection signal is not available, or for a low capacity battery where system cost or board space make USB low power mode external current programming impractical, USB low power charging can be supported indirectly. The IPRGM pin resistance can be selected to obtain the desired USB high power charge current. Then, with the MODE pin always configured for USB high power mode, the UVLR feature will ensure that the charging load on the VIN pin will never pull the USB Vbus supply voltage below V_{UVLR} regardless of the host or hub supply limit. The UVLR limit voltage guarantees that the voltage of the USB Vbus supply will not be loaded below the low power voltage specification limit, as seen by any other low power devices connected to the same USB host or hub.

Under-voltage load regulation can also be beneficial for charging small batteries. Instead of switching the programming resistor depending on the USB mode, UVLR (while selecting USB high power mode) can permit charging at whatever charge current a USB hub low-power supply can provide without compromising the integrity of the hub power supply for other devices.

USB Dedicated Charger Compatibility

The SC824 is especially well suited to the USB Charging Specification, Revision 1.0, Dedicated Charger, Sections 3.5 and 4.1. Important features that support compliance include low quiescent current when disabled (less than 1.5mA), and selectable current limited supply charging behavior.

The USB Dedicated Charger is required to limit its output current to more than 0.5A and less than 1.5A. A dedicated charger identifies itself by shorting together the USB D+ and D- lines. Once the dedicated charger is detected, the SC824, with its 1A max programmed fast charge current in any mode, permits the fast-charge current to be set higher than the 500mA USB High Power Mode limit to permit faster charging of a large battery. (See the section Design Considerations — Large Battery.)

Regardless of the SC824 programmed current, any specification compliant USB Dedicated Charger will either supply more than the programmed fast charge current (and so will regulate to its specified output voltage), or will limit its output current such that its output voltage will be pulled down. The USB Dedicated Charger is required to maintain its current limit down to 2V. By selecting Adapter Mode, the SC824 input will be pulled down to the battery voltage plus charging path dropout. This behavior is recognized in the USB Battery Charging Specification, Section 3.5, as an accepted means to reduce power dissipation in the device while charging at high current.

If there are additional system circuits requiring that the USB Vbus node voltage be maintained above the USB Low Power Mode minimum voltage specification (4.4V), the SC824 USB High Power Mode should be selected. This mode enables Under-Voltage Load Regulation, which will regulate the charging output current, if necessary, to match the Dedicated Charger current limit while maintaining V_{UVLR} (nominally 4.51V) at the VIN pin.

Either of these SC824 charging modes will ensure reliable charging at any programmed charge current, using any USB Battery Charging Specification compliant Dedicated Charger, regardless of its current limit.

Applications Information (continued)

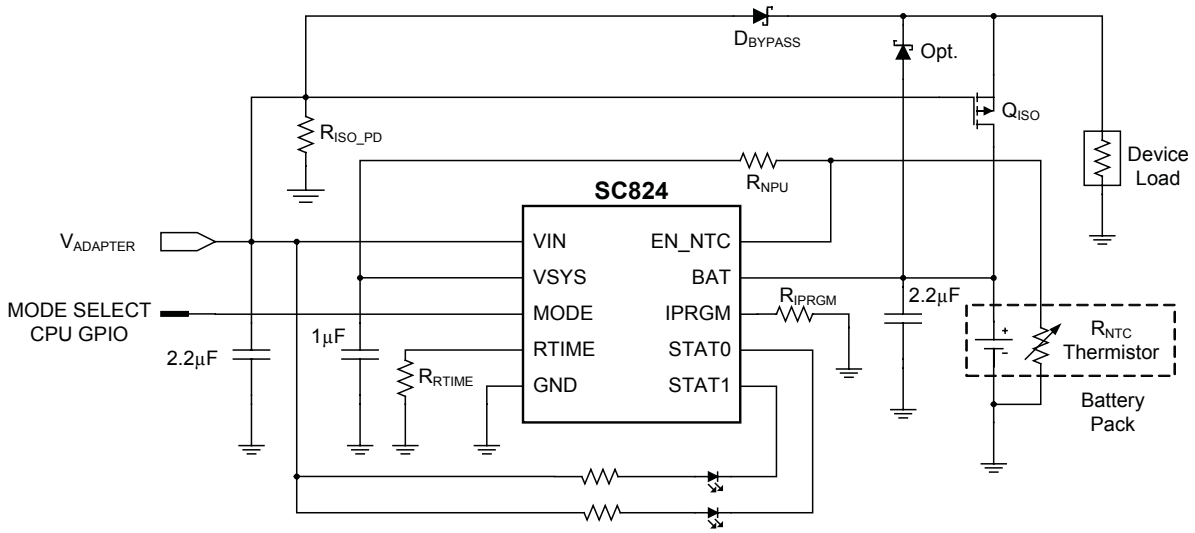


Figure 8 — Battery Isolation and Power Path Bypass – Powering the Load Directly From the Charging Adapter

External Power Path Management

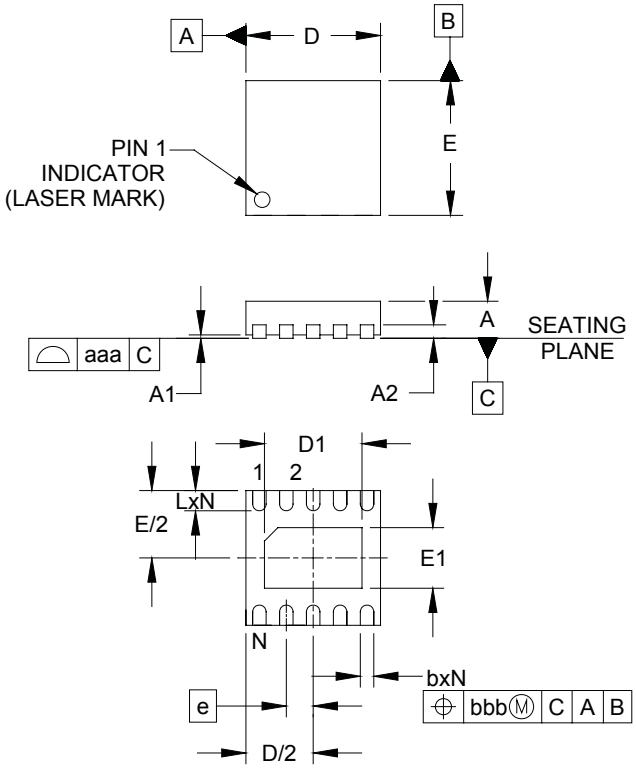
Some applications require that the battery be isolated from the load while charging. Figure 8 illustrates a typical charger bypass circuit. This circuit powers the load directly from the charging source via the Schottky diode D_{BYPASS}. When the charging source is present, the p-channel MOSFET battery isolation switch Q_{ISO} source-to-gate voltage V_{SG} is equal to minus the D_{BYPASS} forward-biased voltage drop, ensuring that the switch Q_{ISO} is off (open). When the charging source is removed, the MOSFET gate is pulled down to ground by R_{ISO_PD}, closing the battery isolation switch and connecting the battery to the load.

When the charging source is removed, the turn-on of Q_{ISO} could be delayed due to its gate capacitance. If so, the substrate PN diode of Q_{ISO} will become forward biased, holding the load voltage to within 0.7V of the battery voltage until $V_{SG} > V_{TH}$, turning on Q_{ISO}. This momentary voltage drop can be mitigated by the use of an optional Schottky diode in parallel with Q_{ISO}, as shown.

With the load isolated from the battery, the charging adapter must supply both the load current and the charging current. If the sum of these should ever exceed the current capacity of the adapter, $V_{ADAPTER}$ will be pulled down. Selection of either of the SC824 USB modes will enable Under-Voltage Load Regulation. UVLR will reduce the charge current if needed to ensure that $V_{ADAPTER}$ will remain at or above V_{UVLR}, maintaining the load supply voltage

To better understand the trade-offs between charger bypass and direct connection of the load to the battery, see the Semtech Application Note AN–PM–0802, *Tradeoffs Between Direct Battery Connection vs. Bypassing the Charger*.

Outline Drawing — MLPD-UT10 2x2

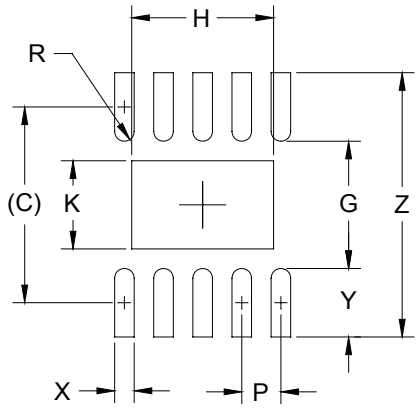


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.152)	
b	.006	.008	.010	0.15	0.20	0.25
D	.075	.079	.083	1.90	2.00	2.10
D1	.053	.057	.061	1.35	1.45	1.55
E	.075	.079	.083	1.90	2.00	2.10
E1	.031	.035	.039	0.80	0.90	1.00
e		.016 BSC			0.40 BSC	
L	.010	.012	.014	0.25	0.30	0.35
N		10			10	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPD-UT10 2x2



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.079)	(2.00)
G	.051	1.30
H	.057	1.45
K	.035	0.90
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.028	0.70
Z	.106	2.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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