10A EcoSpeed® Integrated FET Regulator with 5V LDO and Hiccup Restart

POWER MANAGEMENT

Features

- Power system
  - Input voltage — 3V to 28V
  - Bias Voltage — 5V LDO or 3V to 5.5V external
  - Up to 96% peak efficiency
  - Integrated bootstrap switch
  - LDO output current — up to 200mA
  - Reference tolerance — 1% T_J= -40 to +125 °C
  - EcoSpeed® architecture with pseudo-fixed frequency adaptive on-time control
  - Pre-bias start-up
- Logic input and output control
  - Independent enable control for LDO and switcher
  - Programmable V_{IN} UVLO threshold
  - Power good output
  - Programmable soft-start time
- All protection: automatic restart on fault
  - Over-voltage and under-voltage
  - TC compensated $R_{DS(ON)}$ sensed current limit
  - Thermal shutdown
- Smart gate drive reduces EMI
- Capacitor types: SP, POSCAP, OSCON, and ceramic
- Package — 5 x 5(mm), 32-pin MLPQ
- Lead-free and halogen-free
- RoHS and WEEE compliant

Applications

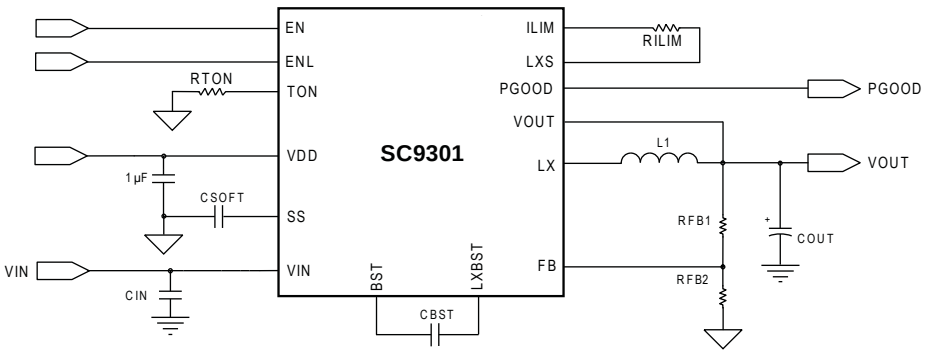
- Networking and telecommunication equipment
- Printers, DSL, and STB applications
- Point-of-load power supplies and module replacement

Description

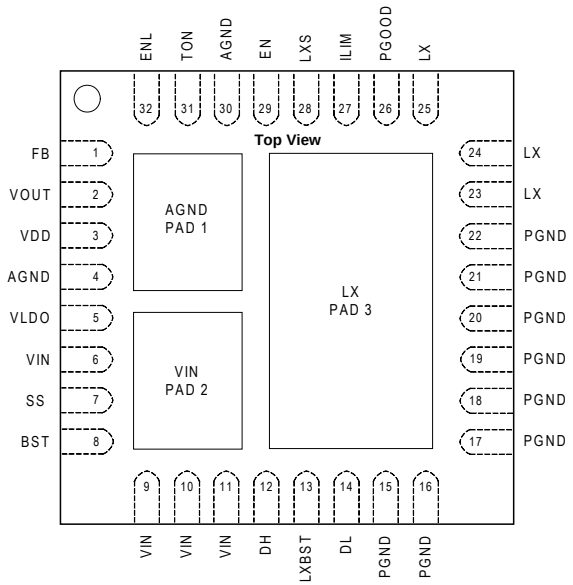
The SC9301 is a stand-alone synchronous EcoSpeed® buck regulator with adaptive on-time control architecture. It features integrated power MOSFETs, a bootstrap switch, and a fixed 5V LDO in a 5x5mm package. The device is highly efficient and uses minimal PCB area. The SC9301 supports using standard capacitor types such as electrolytic or specialty polymer, in addition to ceramic, at switching frequencies up to 1MHz.

Additional features include programmable cycle-by-cycle current limit protection, programmable soft-start, under and over-voltage protection, automatic fault recovery (hiccup restart), and soft shutdown. The device also provides separate enable inputs for the PWM controller and LDO as well as a power good output for the PWM controller.

Typical Application Circuit

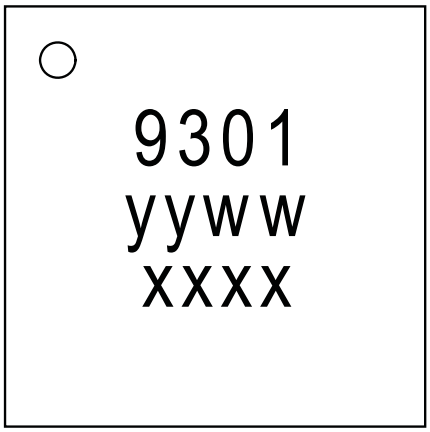


Pin Configuration



MLPQ-UT32

Marking Information



yyww = Date Code
xxxx = Semtech Lot Number

Ordering Information

Device	Package
SC9301MLTRT[1][2]	MLPQ-32, 5 x 5(mm)
SC9301EVB	Evaluation Board

Notes:
1) Available in tape and reel only. A reel contains 3000 devices.
2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Absolute Maximum Ratings[1]

LX to PGND (V) ..... -0.3 to +30
LX to PGND (V) (transient — 100ns max.) ..... -2 to +30
DH, BST to PGND (V) ..... -0.3 to +35
DH, BST to LX (V) ..... -0.3 to +6
DL to PGND (V) ..... -0.3 to +6
VIN to PGND (V) ..... -0.3 to +30
EN, FB, ILIM, PGOOD to AGND (V) ..... -0.3 to +(VDD + 0.3)
SS, VLDO, VOUT to AGND (V) ..... -0.3 to +(VDD + 0.3)
TON to AGND (V) ..... -0.3 to +(VDD -1.5)
ENL to AGND (V) ..... -0.3 to VIN
VDD to PGND (V) ..... 0.3 to +6
AGND to PGND (V) ..... -0.3 to +0.3
ESD Protection Level (HBM)[1] (kV) 2
ESD Protection Level (CDM)[1] (kV) 1

Recommended Operating Conditions

Input Voltage (V) ..... 3 to 28
VDD to PGND (V) ..... 3.0 to 5.5
VOUT to PGND (V) ..... 0.6 to 5.5

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal resistance, junction to ambient [2] (°C/W)
High-side MOSFET 25
Low-side MOSFET 20
PWM controller and LDO thermal resistance 50
Peak IR Reflow Temperature (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, VDD = 5V, T_A = +25°C for Typ, -40 to +85 °C for Min and Max, T_J < 125°C, Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
Input Supply Voltage	$V_{IN} \geq$ VDD	3		28	V
VDD Voltage		3		5.5	V
VIN UVLO Threshold[1]	Sensed at ENL pin, rising edge	1.47	1.57	1.77	V
	Sensed at ENL pin, falling edge	1.15		1.35	
VIN UVLO Hysteresis	Sensed at ENL pin; EN = 5V		0.3		V
VDD UVLO Threshold	Measured at VDD pin, rising edge	2.5		3.0	V
	Measured at VDD pin, falling edge	2.4		2.9	
VDD UVLO Hysteresis			0.18		V
VIN Supply Current	Shutdown mode; ENL , EN = 0V		8.5	20	µA
	Standby mode; ENL = VDD, EN = 0V		130		

Electrical Characteristics (continued)

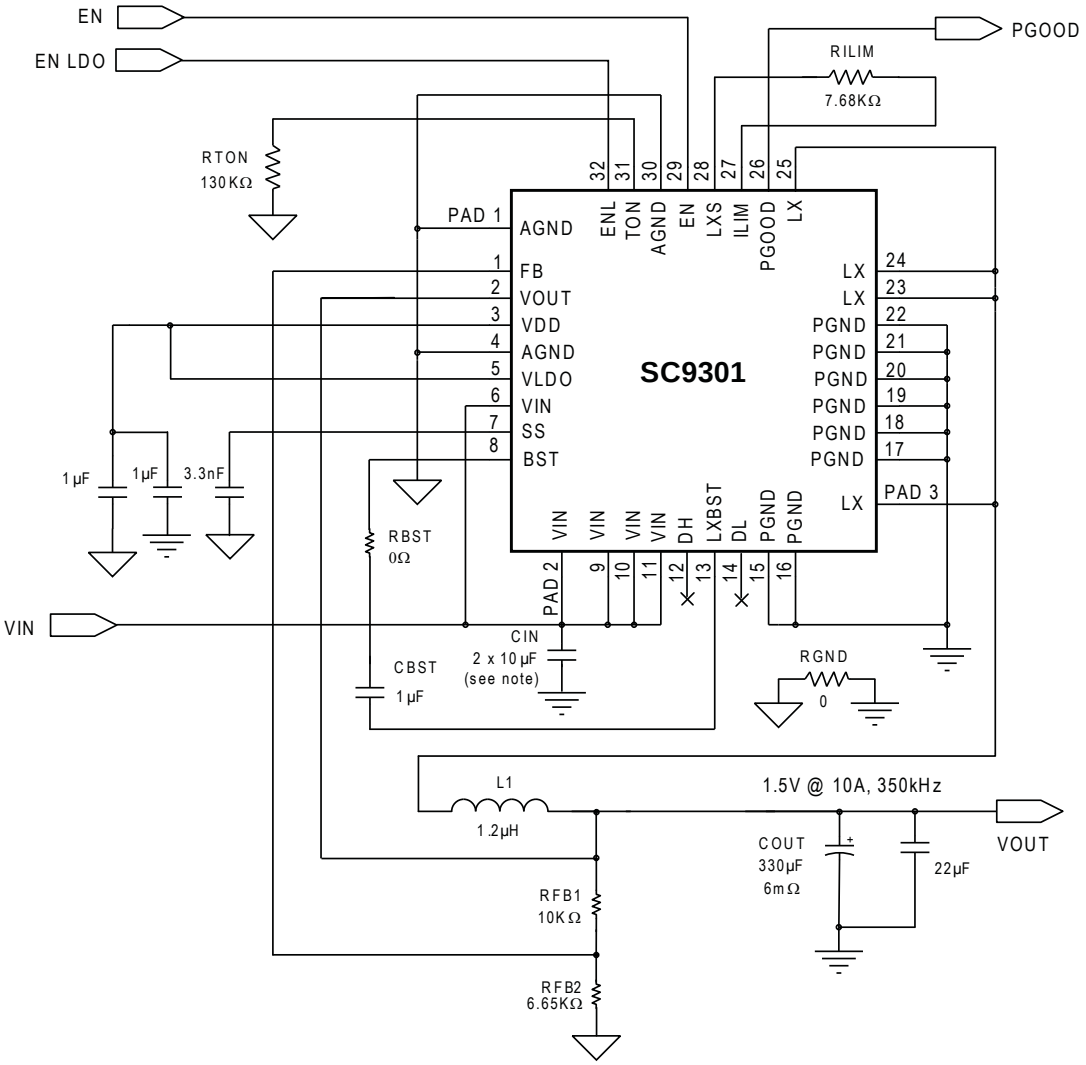
Parameter	Conditions	Min	Typ	Max	Units
Input Supplies (continued)					
VDD Supply Current	ENL , EN = 0V		3	7	μA
	VDD =5V, f_{SW} = 270kHz, EN = VDD, no load[2]		7.7		mA
	VDD =3.3V, f_{SW} = 280kHz, EN = VDD, no load[2]		5.1		mA
FB Comparator Threshold	Static V_{IN} and load, T_J= 0 to +125 °C	0.595	0.600	0.605	V
	Static V_{IN} and load, T_J= -40 to +125 °C	0.594	0.600	0.606	V
Frequency Range				1000	kHz
Bootstrap Switch Resistance			17		Ω
Timing					
On-Time	V_{IN} = 15V, V_{OUT} = 3V, R_{TON} = 300kΩ, VDD = 5V	1395	1600	1805	ns
Minimum On-Time [2]			80		ns
Minimum Off-Time[2]	VDD =5V		250		ns
	VDD =3.3V		370		ns
Soft-Start					
Soft-Start Charge Current			3.0		μA
Soft-Start Voltage[2]	When V_{OUT} reaches regulation		1.5		V
Analog Inputs/Outputs					
VOUT Input Resistance			500		kΩ
Power Good					
Power Good Threshold	Upper limit, V_{FB} > internal 600mV reference		+20		%
	Lower limit, V_{FB} < internal 600mV reference		-10		%
Power Good Hysteresis			1.2		%
Start-Up Delay Time[2] (between PWM enable and PGOOD high)	VDD = 5V, C_{SS} = 3.3nF		3.8		ms
	VDD = 3.3V, C_{SS} = 3.3nF		2.6		ms
Fault (noise immunity) Delay Time[2]			5		μs
Leakage	PGOOD = high impedance (open)			1	μA
Power Good On Resistance			10		Ω

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Fault Protection					
Valley Current Limit(3)	VDD = 5V, R_{ILIM} = 7320, T_J = 0 to +125 °C	8.5	10	11.5	A
	VDD = 3.3V, R_{ILIM} = 7320, T_J = 0 to +125 °C		9		A
I_{LIM} Source Current	Trimmed to match lower FET Rdson		9		µA
I_{LIM} Comparator Offset	With respect to AGND	-8	0	+8	mV
Output Under-Voltage Threshold	V_{FB} with respect to internal 600mV reference, 8 consecutive cycles		-25		%
Smart Power-Save Protection Threshold(2)	V_{FB} with respect to internal 600mV reference		+10		%
Over-Voltage Protection Threshold	V_{FB} with respect to internal 600mV reference		+20		%
Over-Voltage Fault Delay(2)			5		µs
Over-Temperature Shutdown(2)	10°C hysteresis		150		°C
Logic Inputs/Outputs					
Logic Input High Voltage	EN, ENL	1.0			V
Logic Input Low Voltage	EN, ENL			0.4	V
EN Input Bias Current	EN = VDD or AGND	-10		+10	µA
ENL Input Bias Current	ENL = V_{IN} = 28V	-1	11	+18	µA
FB Input Bias Current	FB = VDD or AGND	-1		+1	µA
Linear Regulator (LDO)					
VLDO Accuracy	VLDO load = 10mA	4.90	5.0	5.10	V
Current Limit	Short-circuit protection, V_{IN} = 12V, VLDO < 1V		20		mA
	V_{IN} = 12V, 1V < VLDO < 4.5V		115		
	Operating, VLDO > 4.5V		200		
VLDO Drop Out Voltage(4)	V_{IN} to VLDO, VLDO load = 100mA		1.9		V

Notes:
(1) VIN UVLO is programmable using a resistor divider from VIN to ENL to AGND. The ENL voltage is compared to an internal reference.
(2) Typical value measured on standard evaluation board.
(3) The device has first order temperature compensation for over current. Results vary based upon the PCB thermal layout.
(4) The LDO drop out voltage is the voltage at which the LDO output drops 2% below the nominal regulation point.

Detailed Application Circuit



Key Components

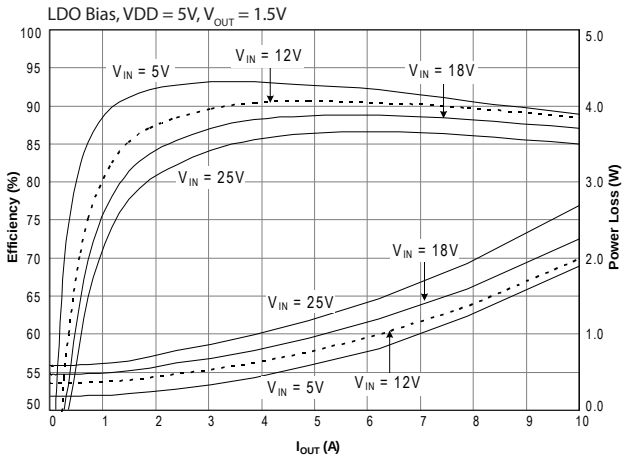
Component	Value	Manufacturer	Part Number	Web
CIN (see note)	2 x 10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT	330µF/6mΩ	Sanyo	2TPF330M6	www.sanyo.com
L1	1.2µH/1.8mΩ	Wurth Elektronik	744 325 120	www.we-online.com

NOTE: The quantity of 10µF input capacitors required varies with the application requirements.

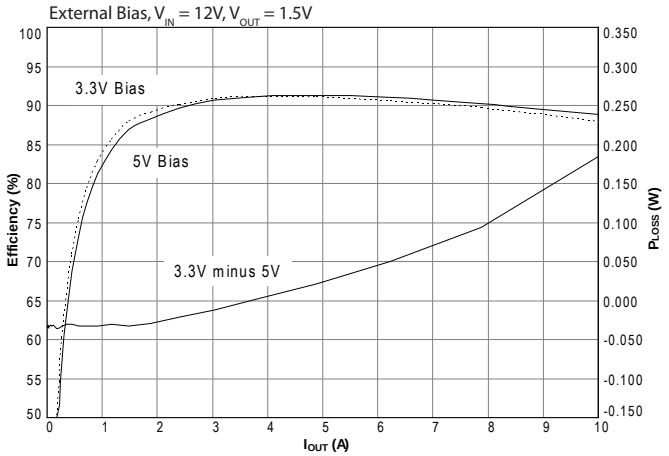
Typical Characteristics

Characteristics in this section are based upon using the Typical Application Circuit on page 6.

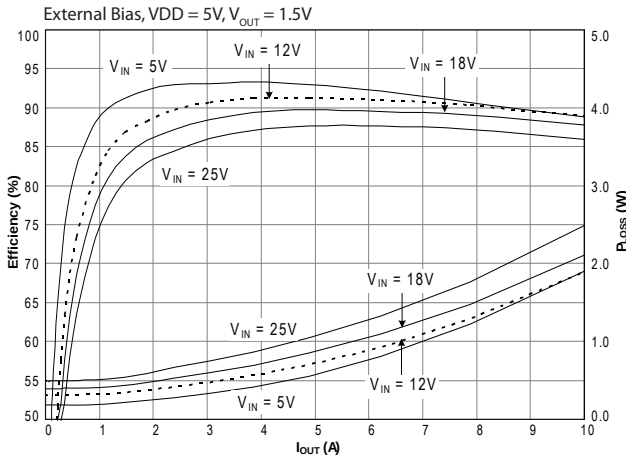
Efficiency/Power Loss vs. Load



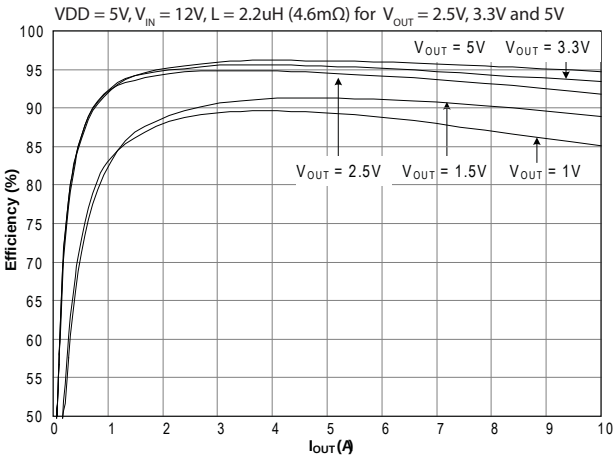
Efficiency/Power Loss Comparison



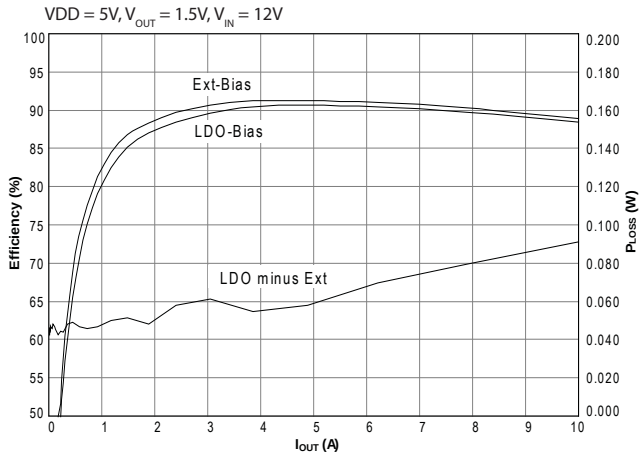
Efficiency/Power Loss vs. Load



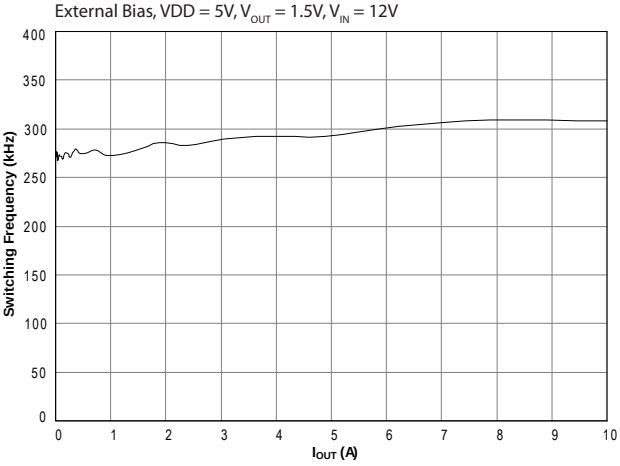
Efficiency/Power Loss Comparison



Efficiency/Power Loss Comparison



Switching Frequency vs. Load

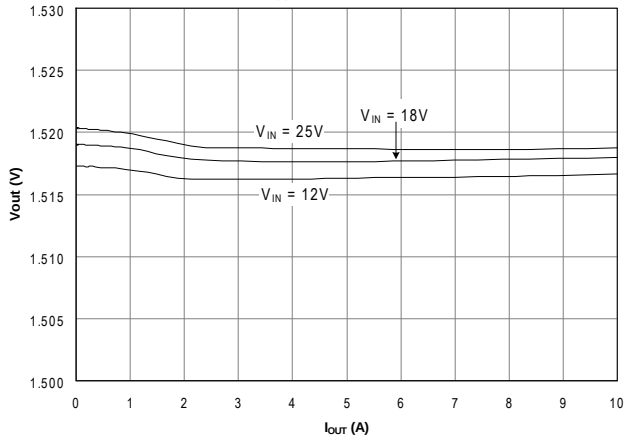


Typical Characteristics

Characteristics in this section are based upon using the Typical Application Circuit on page 6.

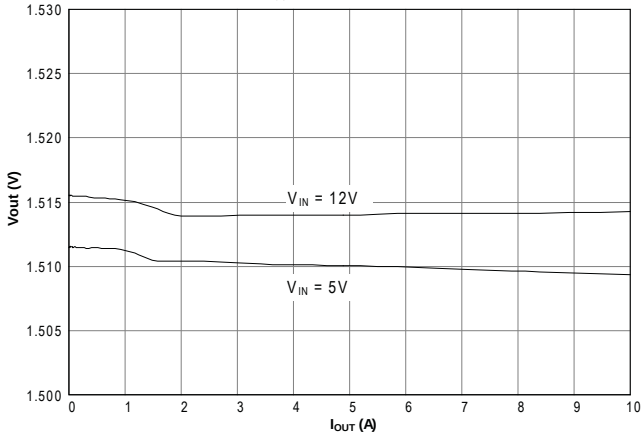
Load Regulation

External Bias, VDD = 5V, V_{OUT} = 1.5V



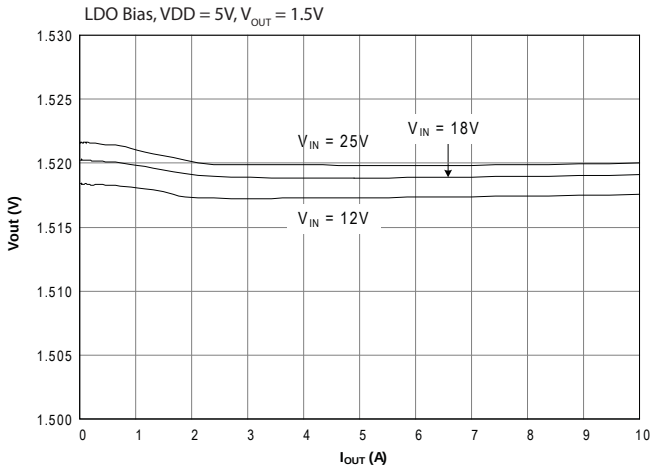
Load Regulation

External Bias, VDD = 3.3V, V_{OUT} = 1.5V



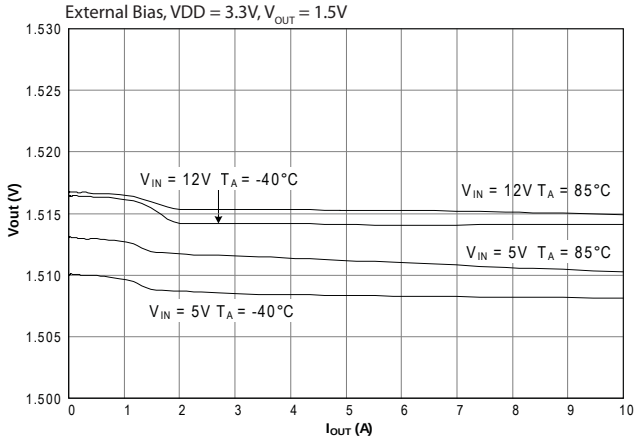
Load Regulation

LDO Bias, VDD = 5V, V_{OUT} = 1.5V



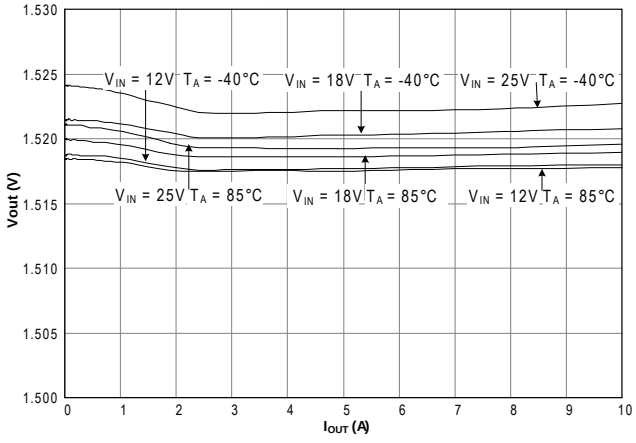
Load Regulation vs. Temperature

External Bias, VDD = 3.3V, V_{OUT} = 1.5V



Load Regulation vs. Temperature

External Bias, VDD = 5V, V_{OUT} = 1.5V

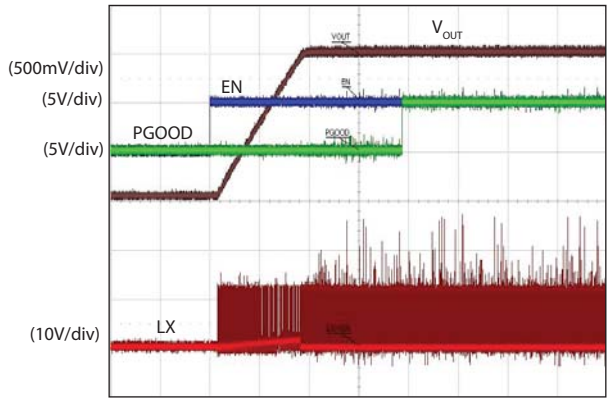


Typical Characteristics (continued)

Characteristics in this section are based upon using the Typical Application Circuit on page 6.

Start-up — Full Load

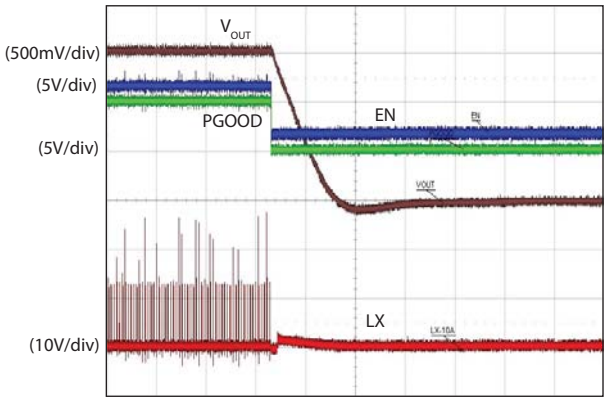
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A



Time (1ms/div)

Shutdown — EN

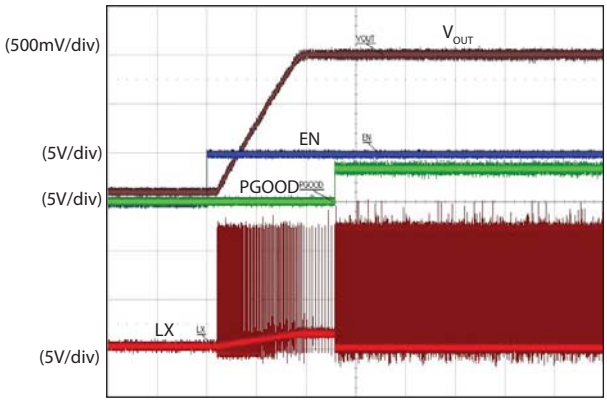
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A



Time (50µs/div)

Start-up — No Load

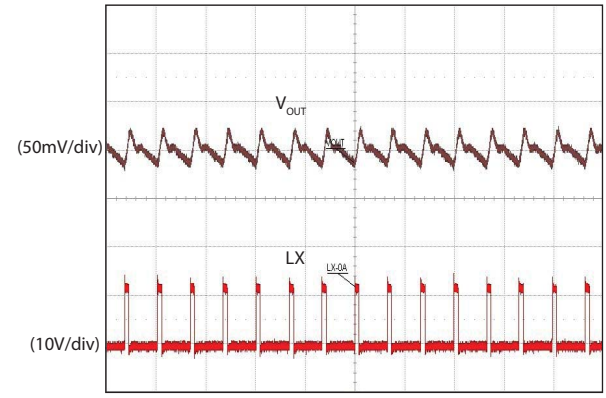
VDD = 3.3V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (1 ms/div)

Steady State — No Load

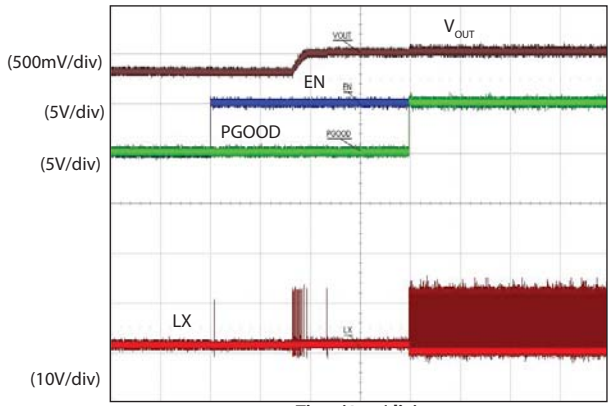
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (5µs/div)

Start-up — Prebias

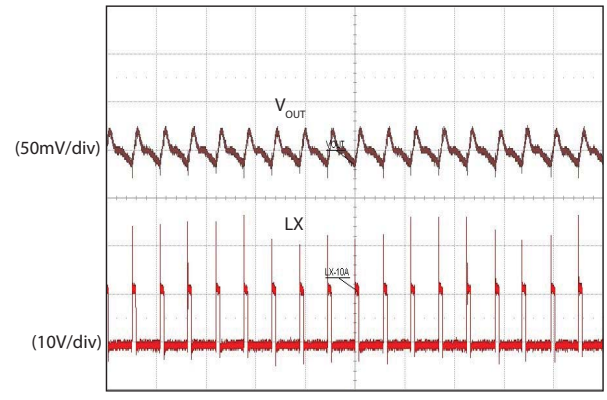
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (1ms/div)

Steady State — Full Load

VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A



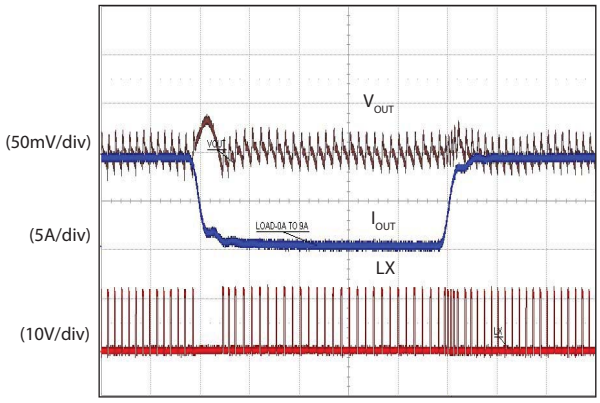
Time (5µs/div)

Typical Characteristics (continued)

Characteristics in this section are based upon using the Typical Application Circuit on page 6.

Transient Response

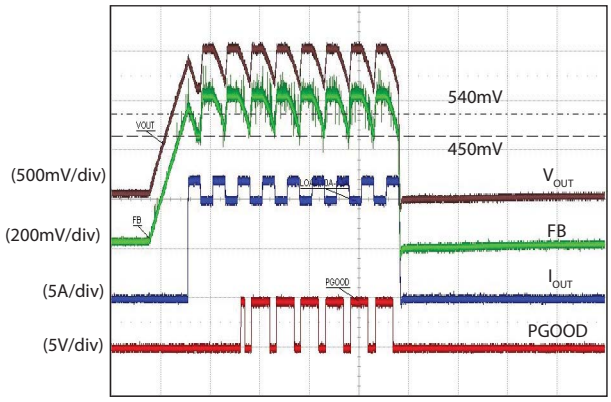
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 9A to 0A to 9A



Time (20µs/div)

Protection — OCP then UV

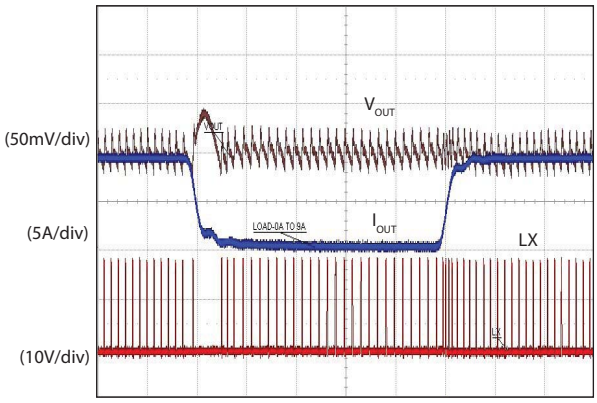
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 10A to 12A



Time (2ms/div)

Transient Response

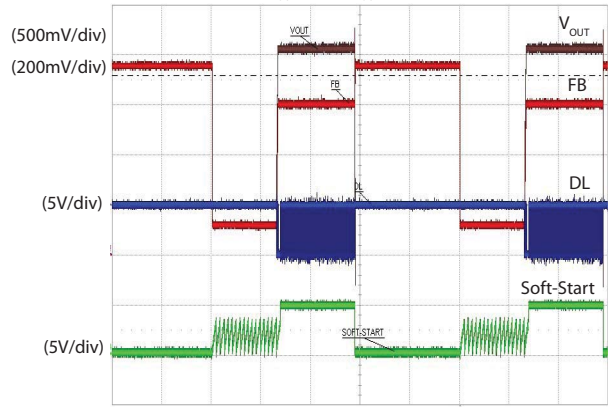
VDD = 5V, V_{IN} = 18V, V_{OUT} = 1.5V, I_{OUT} = 9A to 0A to 9A



Time (20µs/div)

Protection — OVP

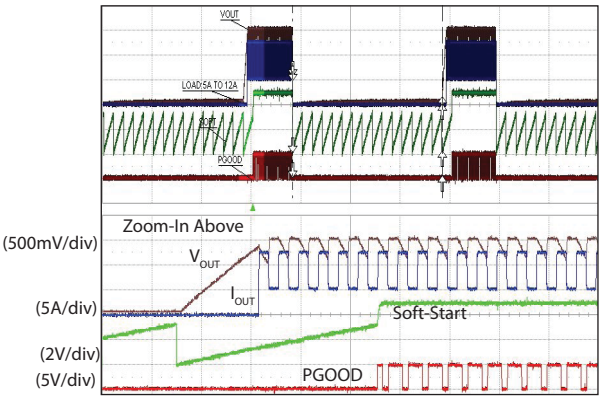
VDD = 5V, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A



Time (50ms/div)

Protection: OCP, UVP then Hiccup

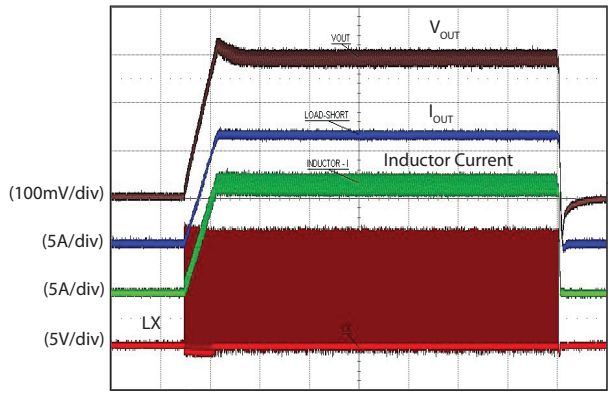
V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 5A to 12A



Time: Above (20ms/div), Bottom (1ms/div)

Start-up—Short & Over Current Protection

V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = OC regulated at valley 10.2A

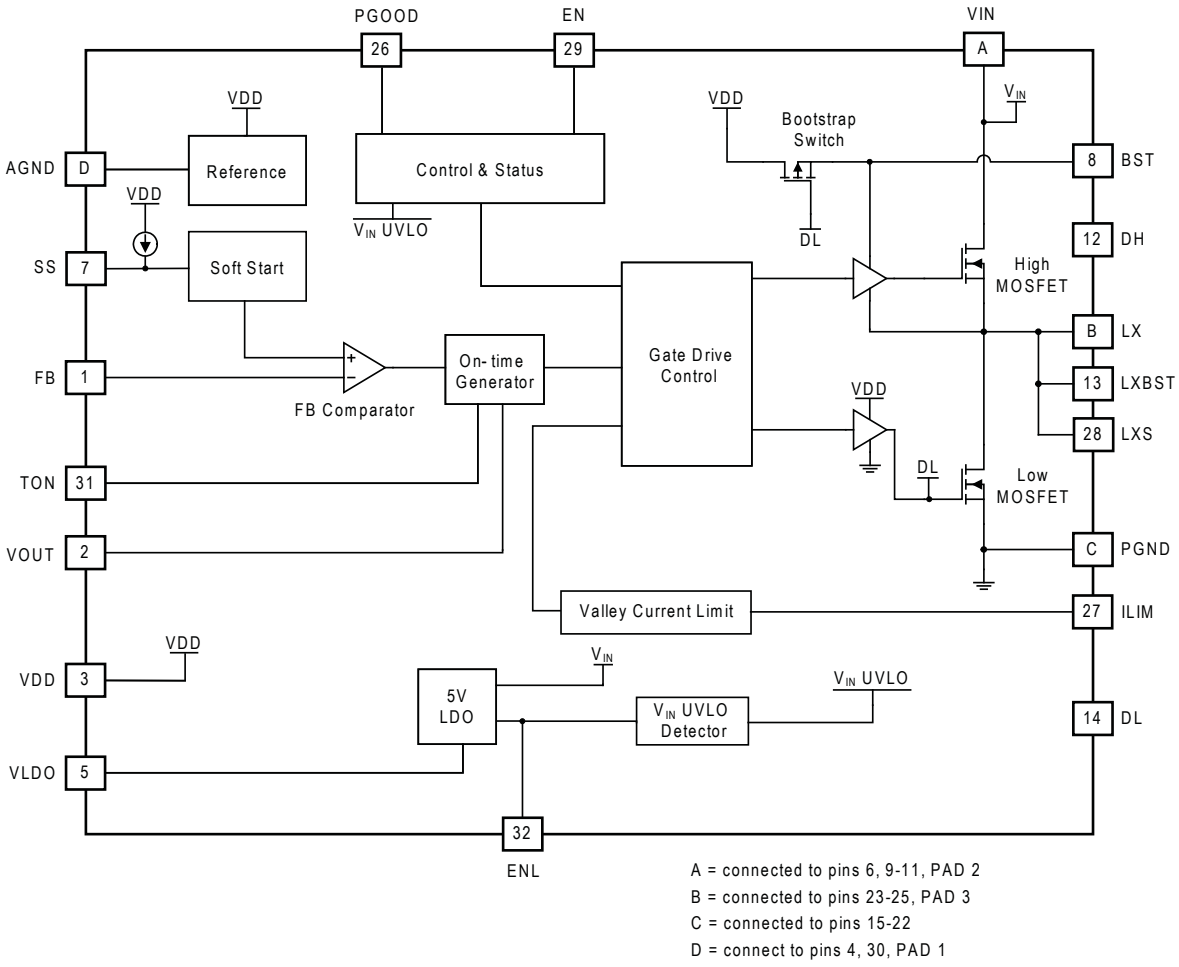


Time (500µs/div)

Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback input for switching regulator used to program the output voltage — connect to an external resistor divider from VOUT to AGND.
2	VOUT	Switcher output voltage sense pin.
3	VDD	Bias supply for the IC.
4, 30, PAD 1	AGND	Analog ground
5	VLDO	LDO output. Connect to VDD when using the internal LDO as a bias power supply.
6, 9-11, PAD 2	VIN	Input supply voltage
7	SS	The soft-start ramp will be programmed by an internal current source charging a capacitor on this pin.
8	BST	Bootstrap pin — connect a capacitor of at least 100nF from BST to LXBST to develop the floating supply for the high-side gate drive.
12	DH	High-side gate drive
13	LXBST	LX Boost — connect to the BST capacitor.
23-25, PAD 3	LX	Switching (phase) node
14	DL	Low-side gate drive
15-22	PGND	Power ground
26	PGOOD	Open-drain power good indicator — high impedance indicates power is good. An external pull-up resistor is required.
27	ILIM	Current limit sense pin — used to program the current limit by connecting a resistor from ILIM to LXS.
28	LXS	LX sense — connects to R_{ILIM}
29	EN	Enable input for the switching regulator — connect to AGND to disable the switching regulator, connect to VDD or float to operate in forced continuous mode.
31	TON	On-time programming input — set the on-time by connecting through a resistor to AGND
32	ENL	Enable input for the LDO — connect ENL to AGND to disable the LDO. Drive with logic signal for logic control, or program the VIN UVLO with a resistor divider between VIN, ENL, and AGND.

Block Diagram



Applications Information

Synchronous Buck Converter

The SC9301 is a step down synchronous DC-DC buck converter with integrated power MOSFETs and a 200mA capable 5V LDO. The device is capable of 10A operation at very high efficiency. A space saving 5x5 (mm) 32-pin package is used. The programmable operating frequency of up to 1MHz enables optimizing the configuration for PCB area and efficiency.

The buck controller uses a pseudo-fixed frequency adaptive on-time control. This allows fast transient response which permits the use of smaller output capacitors.

Input Voltage Requirements

The SC9301 requires two input supplies for normal operation: V_{IN} and VDD. V_{IN} operates over the wide range of 3V to 28V. VDD requires a 3V to 5.5V supply which can be from an external source or from the internal fixed 5V LDO.

Power Up Sequence

When the SC9301 uses an external power source at the VDD pin, the switching regulator initiates the start up when V_{IN}, VDD and EN are above their respective thresholds. When EN is at a logic high, VDD can be applied after V_{IN} rises. It is also recommended to use a10Ω resistor between an external power source and the VDD pin. To start up using the EN pin when both VDD and V_{IN} are above their respective thresholds, apply EN to enable the start-up process. For SC9301 in self-biased mode, refer to the LDO section for a full description.

Shutdown

The SC9301 can be shutdown by pulling either VDD or EN below its threshold. When VDD is active and EN at low logic, the output voltage discharges through an internal FET.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC9301 is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

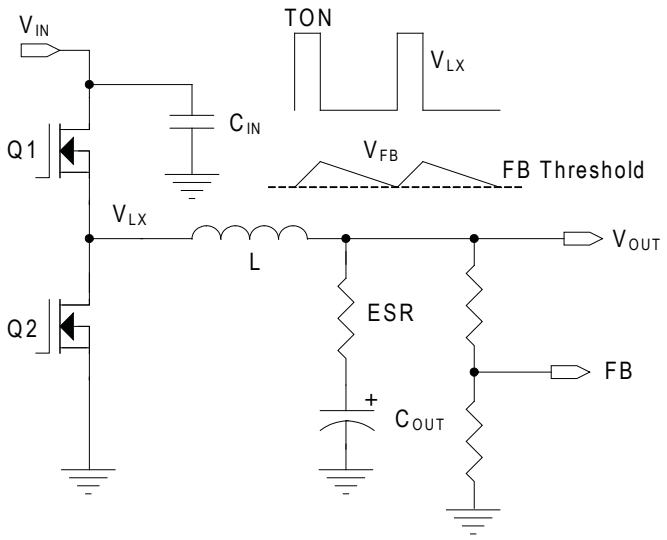


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}. The period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time configuration, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response.

One-Shot Timer and Operating Frequency

One-shot timer operation is shown in Figure 2. The FB comparator output goes high when V_{FB} is less than the internal 600mV reference. This feeds into the DH gate drive and turns on the high-side MOSFET, and also starts the one-shot

Applications Information (continued)

timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

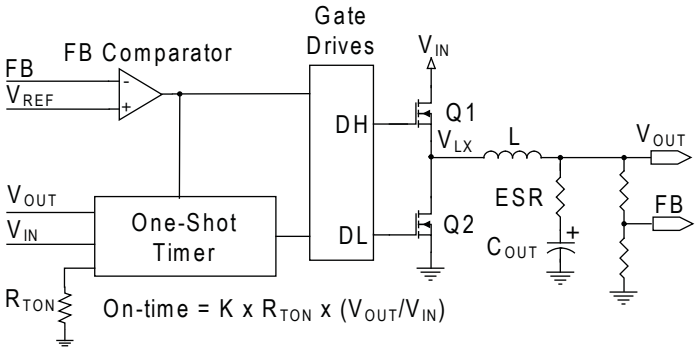


Figure 2 — On-Time Generation

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

The SC9301 uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide an operating frequency from 200kHz to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{k}{26.75pF \times f_{SW}}$$

The constant, k, equals 1 when VDD is greater than 4.5V. If VDD is less than 4.5V and V_{IN} is greater than (VDD -1.8) x 10, k is shown by the following equation.

$$k = \frac{(VDD - 1.8) \times 10}{V_{IN}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{TON\_MAX} = \frac{V_{IN\_MIN}}{10 \times 1.5\mu A}$$

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 600mV reference voltage (see Figure 3).

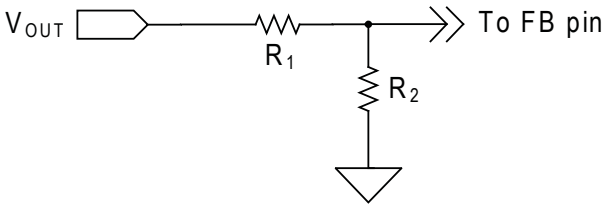


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC value of V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

When a large capacitor is placed in parallel with R1 (CTOP) VOUT is shown by the following equation.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right) \times \sqrt{\frac{1 + (R_1 \omega C_{TOP})^2}{1 + \left(\frac{R_2 \times R_1}{R_2 + R_1} \omega C_{TOP}\right)^2}}$$

The switcher output voltage can be programmed higher than 5V with careful design. In this case the VOUT pin cannot connect directly to the switcher output due to its the maximum voltage rating. An additional resistor divider network is required to connect from the switcher output to the VOUT pin. When the SC9301 operates from an external 5V supply and the LDO is disabled by grounding the ENL pin, the voltage at the VOUT pin can be as high as shown in the Recommended Operating Conditions. Note that RTON must be adjusted higher by the same divider ratio to maintain the desired on-time; on-time is calculated according to the voltage at the VOUT pin.

Applications Information (continued)

Forced Continuous Mode Operation

The SC9301 operates the switcher in FCM (Forced Continuous Mode) as shown in Figure 4. In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This feature results in uniform frequency across the full load range. DH is the gate signal to drive upper MOSFET. DL is the lower gate signal to drive lower MOSFET.

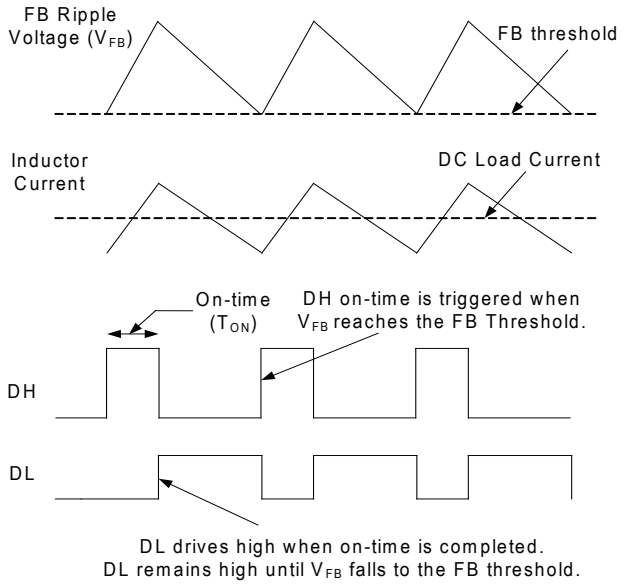


Figure 4 — Forced Continuous Mode Operation

SmartDrive™

For each DH pulse, the DH driver initially turns on the high-side MOSFET at a slower speed, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off and the LX voltage has risen 0.5V above PGND, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching noise while maintaining high efficiency, reducing the need for snubbers or series resistors in the gate drive.

Enable Input

The EN pin is used to enable or disable the switching regulator. When EN is low, the switching regulator is off and in its lowest power state. When off, the output of the switching regulator soft-discharges the output into a 15Ω internal resistor via the VOUT pin.

Current Limit Protection

The device features programmable current limiting, which is accomplished by using the RDS_{ON} of the lower MOSFET for current sensing. The current limit is set by R_{ILIM} resistor. The R_{ILIM} resistor connects from the ILIM pin to the LXS pin which is also the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal ~9µA current flows from the ILIM pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the RDS_{ON}. The voltage across the MOSFET is negative with respect to ground. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and will not allow another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM voltage back up to zero. This method regulates the inductor valley current at the level shown by I_{OC} in Figure 5.

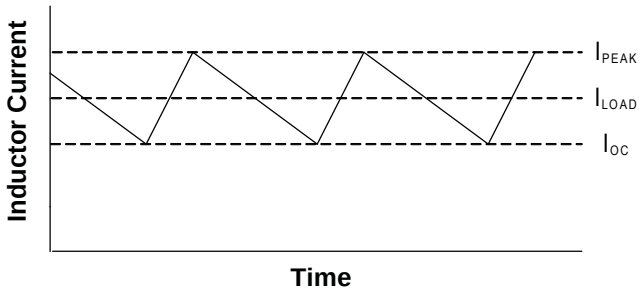


Figure 5 — Valley Current Limit

Setting the valley current limit to 10A results in a peak inductor current of 10A plus the peak-to-peak ripple current. In this situation, the average (load) current through the inductor is 10A plus one-half the peak-to-peak ripple current.

The internal 9µA current source is temperature compensated at 4100ppm in order to provide tracking with the RDS_{ON}.

The R_{ILIM} value is calculated by the following equations.

For VDD>4V; $R_{ILIM} = 732 \times I_{OC}$

For VDD<4V; $R_{ILIM} = 834 \times I_{OC}$

Applications Information (continued)

When selecting a value for R_{ILIM} be sure not to exceed the absolute maximum voltage value for the ILIM pin. Note that because the low-side MOSFET with low RDS_{ON} is used for current sensing, the PCB layout, solder connections, and PCB connection to the LX node must be done carefully to obtain good results. R_{ILIM} should be connected directly to LXS (pin 28).

Soft-Start of PWM Regulator

SC9301 has a programmable soft-start time that is controlled by an external capacitor at the SS pin. After the controller meets both UVLO and EN thresholds, the controller has an internal current source of 3µA flowing through the SS pin to charge the capacitor. During the start up process (Figure 6), 40% of the voltage at the SS pin is used as the reference for the FB comparator. The PWM comparator issues an on-time pulse when the voltage at the FB pin is less than 40% of the SS pin. As result, the output voltage follows the SS start voltage. The output voltage reaches and maintains regulation when the SS pin voltage is > 1.5V. The time between the first LX pulse and when VOUT meets regulation is the soft-start time (t_{SS}). The calculation for the soft-start time is shown by the following equation.

$$t_{SS} = \frac{C_{SS} \times 1.5V}{3\mu A}$$

The voltage at the SS pin continues to ramp up and eventually is equal to 67% of VDD. After soft-start completes, the FB pin voltage is compared to an internal reference of 600mV. The delay time between the VOUT regulation point and PGOOD going high is shown by the following equation.

$$t_{PGOOD} = \frac{C_{SS}}{3\mu A} \times \left(\frac{2 \times V_{IN}}{3} - 1.5V \right)$$

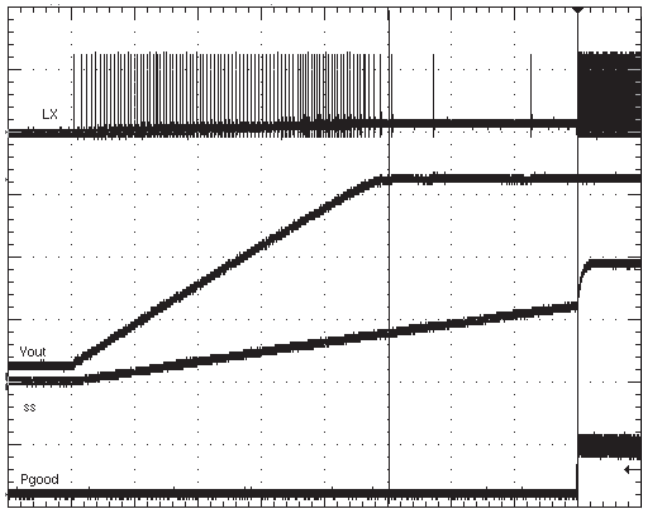


Figure 6 — Soft-start Timing Diagram

Pre-Bias Startup

SC9301 can start up as if in a soft-start condition with an existing output voltage level. The soft-start time is still the same as normal start up (when the output voltage starts from zero). The output voltage starts to ramp up when 40% of the voltage at SS pin meets the pre-charge FB voltage level. Pre-bias startup is achieved by turning off the lower gate when the inductor current falls below zero. This method prevents the output voltage from decreasing.

Power Good Output

The PGOOD (power good) output is an open-drain output which requires a pull-up resistor. When the voltage at the FB pin is 10% below the nominal voltage, PGOOD is pulled low. It remains low until the FB voltage returns above -8% of nominal. During start-up PGOOD is held low and will not be allowed to transition high until the PGOOD start-up delay time has passed and soft-start is completed (when V_{FB} reaches 600mV).

PGOOD will transition low if the FB voltage exceeds +20% of nominal (720mV), which is also the over-voltage shutdown threshold. PGOOD also pulls low if the EN pin is low when VDD is present.

Applications Information (continued)

Output Over-Voltage Protection

OVP (Over-voltage protection) becomes active as soon as the device is enabled. The OVP threshold is set at 600mV + 20% (720mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off until the over-voltage condition is removed. At this point a hiccup delay cycle initiates and the part will re-start. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25% below its nominal voltage (falls to 450mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to tri-state the MOSFETs and enters hiccup mode.

Hiccup Cycling and Automatic Fault Recovery

The SC9301 includes an automatic recovery feature (hiccup mode upon fault). If the switcher output is shut down due to a fault condition, the device will use the SS capacitor as a timer. Upon fault shutdown the SS pin is pulled low, and then will begin charging through the internal 3µA current source. When the SS capacitor reaches 67% of VDD, the SS pin is again pulled low, after which the SS capacitor begins another charging cycle. The SS capacitor will be used for 15 cycles of charging from 0 to 67% of VDD. During this time, the switcher is off and there is no MOSFET switching.

During the 16th SS cycle, a normal soft-start cycle is implemented and the MOSFETs will start a switching cycle. Switching continues until the soft-start delay time is reached. If the switcher output is still in a fault condition, the switcher will shut down again and wait another fifteen soft-start cycles before attempting the next soft-start. The long delay between soft-start cycles reduce average power loss in the power components.

VDD UVLO and POR

The VDD Under-Voltage Lock-Out (UVLO) circuitry inhibits switching and tri-states the DH/DL drivers until VDD rises above 2.5V. When VDD exceeds 2.5V, an internal POR (Power-On Reset) resets the fault latch and the soft-start circuitry and then the SC9301 begins the soft-start cycle. The switcher will shut off if VDD falls below 2.4V.

LDO Regulator

When the LDO is providing bias power to the device, a minimum 0.1µF capacitor referenced to AGND is required, along with a minimum 1µF capacitor referenced to PGND to filter the gate drive pulses. Refer to the PCB Layout Guidelines section.

ENL Pin and VIN UVLO

The ENL pin also acts as the V_{IN} under-voltage lockout for the switcher. The V_{IN} UVLO voltage is programmable via a resistor divider at the VIN, ENL and AGND pins.

Timing is important when driving ENL with logic and not implementing V_{IN} UVLO. The ENL pin must transition from high to low within 2 switching cycles to avoid the PWM output turning off. If ENL goes below the V_{IN} UVLO threshold and stays above 1V, then the switcher will turn off but the LDO will remain on.

The next table summarizes the function of the ENL and EN pins, with respect to the rising edge of ENL.

EN	ENL	LDO status	Switcher status
low	low, < 0.4V	off	off
high	low, < 0.4V	off	on
low	high, < 1.57V	on	off
high	high, < 1.57V	on	off
low	high, > 1.57V	on	off
high	high, > 1.57V	on	on

Figure 7 shows the ENL voltage thresholds and their effect on LDO and Switcher operation.

Applications Information (continued)

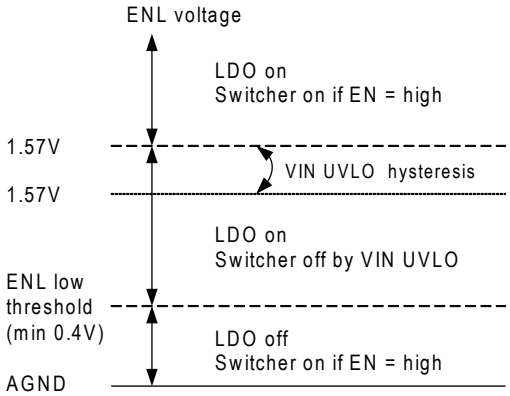


Figure 7 — ENL Thresholds

ENL Logic Control of PWM Operation

When the ENL input exceeds the VIN UVLO threshold of 1.57V, internal logic checks the PGOOD signal. If PGOOD is high, the switcher is already running and the LDO will start without affecting the switcher. If PGOOD is low, the device disables PWM switching until the LDO output has reached 90% of its final value. This delay prevents the additional current needed by the DH and DL gate drives from overloading the LDO at start-up.

LDO Start-up

Before LDO start-up, the device checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. VLDO output
3. V_{IN} input voltage

When the ENL pin is high and V_{IN} is available, the LDO will begin start-up. During the initial phase, when VLDO is below 1V, the LDO initiates a current-limited start-up (typically 20mA). This protects the LDO from thermal damage if the V_{LDO} is shorted to ground. As V_{LDO} exceeds 1V, the start-up current gradually increases to 115mA. When V_{LDO} reaches 4.5V, the LDO current limit is increased to 200mA and the LDO output rises quickly to 5.0V. The LDO start-up is shown in Figure 8.

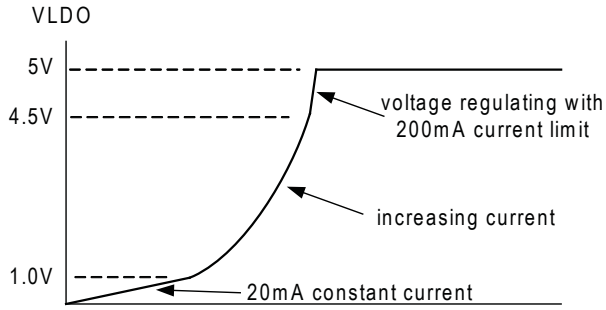


Figure 8 — LDO Start-Up

Using the Internal LDO to Bias the SC9301

The following steps must be followed when using the internal LDO to bias the device.

- Connect VDD to VLDO before enabling the LDO.
- During the initial start-up the LDO, when the LDO output is less than 1V, the external load should not exceed 20mA. Above 1V, any external load on VLDO should not exceed 115mA until the LDO voltage has reached 90% of final value.

Applications Information (continued)

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage including the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- V_{IN} = 12V ± 10% and LDO bias
- V_{OUT} = 1.5V ± 3%
- f_{SW} = 300kHz
- Load = 10A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 300kHz which results from using components selected for optimum size and cost.

A resistor, R_{TON} is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{k}{26.75pF \times f_{SW}}$$

Substituting for R_{TON} results in the following solution.

$$R_{TON} = 124.6k\Omega$$

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4A then Power-save operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then power-save will start for loads less than 20% of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25% to 50% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The following equation for determining inductance is shown.

$$\Delta = \frac{\square_{IN} - \square_{OUT} \times T_{ON}}{\square_{\square\square\square}}$$

Example

In this example, the inductor ripple current is set equal to 35% of the maximum load current. Therefore ripple current will be 35% x 10A or 3.5A. To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

Applications Information (continued)

$$T_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

T_{ON} = 379 ns at 13.2V_{IN}, 1.5V_{OUT}, 300kHz

$$\square = \frac{\square 13.2 - 1.5 \square \times 379ns}{3.5 \square} = 1.27\mu H$$

A slightly smaller value of 1.2µH is selected. This will increase the maximum I_{RIPPLE} to 3.7A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON \square VIN \square IN} = \frac{25 \square \square \times \square_{TON} \times V_{OUT}}{V_{IN \square IN}} = \square 51ns$$

$$I_{\square I \square \square \square} = \frac{\square V_{IN} - V_{OUT} \square \times T_{ON}}{\square}$$

$$I_{\square I \square \square \square \square VIN \square IN} = \frac{\square 10. \square - 1.5 \square \times \square 51ns}{1.2\mu H} = 3.5 \square$$

Capacitor Selection

The output capacitors are chosen based upon required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. A change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal for output voltage ripple is 2% of 1.5V or 30mV. The maximum ESR value allowed is shown by the following equations.

$$\square \square \square_{\square \square} = \frac{V_{\square I \square \square \square}}{I_{\square I \square \square \square \square \square \square}} = \frac{30 \square V}{3.7 \square}$$

ESR_{MAX} = 8.1 mΩ

The output capacitance is usually chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$\square OUT_{MIN} = \frac{\square \left(I_{OUT} + \frac{1}{2} \times I_{RI \square \square \square EMAX} \right)^2}{(V_{\square EA \square})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.65V (150mV rise upon load release), and a 10A load release, the required capacitance is shown by the next equation.

$$\square OUT_{MIN} = \frac{1.2\mu H \left(10 + \frac{1}{2} \times 3.7 \right)^2}{(1. \square 5)^2 - (1.5)^2} = 357\mu \square$$

During the load release time, the voltage cross the inductor is approximately -V_{OUT}. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not much faster than the di/dt of the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt.

Peak inductor current is shown by the next equation.

I_{LPK} = I_{MAX} + 1/2 x $I_{RIPPLEMAX}$

I_{LPK} = 10 + 1/2 x 3.7 = 11.85A

$$Rat \square \ \square \square \square an \square \square \ L \square a \square \ \square \square \square \square nt = \frac{\square \square_{LOA \square}}{\square t}$$

I_{MAX} = maximum load release = 10A

$$\square_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOA \square}} \times dt}{2(V_{PK} - V_{OUT})}$$

Applications Information (continued)

Example

$$\frac{dI_{LOAD}}{dt} = \frac{2.5A}{1\mu s}$$

This would cause the output current to move from 10A to 0A in 4µs, giving the minimum output capacitance requirement shown in the following equation.

$$C_{OUT} = 11.85 \times \frac{1.2\mu H \times \frac{11.85}{1.5} - \frac{10}{2.5} \times 1\mu s}{2(1.65 - 1.5)}$$

$$C_{OUT} = 216\ \mu F$$

Note that C_{OUT} is much smaller in this example, 216µF compared to 357µF based on a worst-case load release. To meet the two design criteria of minimum 357µF and maximum 8.1mΩ ESR, select one capacitor of 330µF and 6mΩ ESR.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small capacitor across the upper feedback resistor, as shown in Figure 9. This capacitor should be left unpopulated unless it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

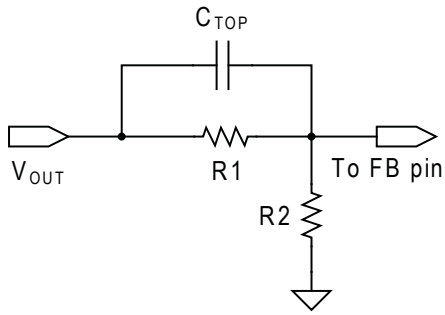


Figure 9 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is decreased load regulation.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications the minimum ESR ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

Applications Information (continued)

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

Using Ceramic Output Capacitors

When the system is using high ESR value capacitors, the feedback voltage ripple lags the phase node voltage by 90 degrees. Therefore, the converter is easily stabilized. When the system is using ceramic output capacitors, the ESR value is normally too small to meet the above ESR criteria. As a result, the feedback voltage ripple is 180 degrees from the phase node and behaves in an unstable manner. In this application it is necessary to add a small virtual ESR network that is composed of two capacitors and one resistor, as shown in Figure 10.

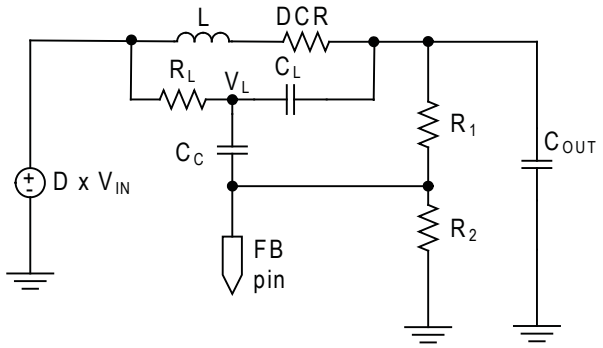


Figure 10 — Virtual ESR Ramp Circuit

The ripple voltage at FB is a superposition of two voltage sources: the voltage across C_L and output ripple voltage. They are defined in the following equations.

$$Vc_L = \frac{I_L \times DCR(s \times L / DCR + 1)}{S \times R_L C_L + 1}$$

$$\Delta V_{OUT} = \frac{\Delta I_L}{8C \times f_{SW}}$$

Figure 11 shows the magnitude of the ripple contribution due to C_L at the FB pin.

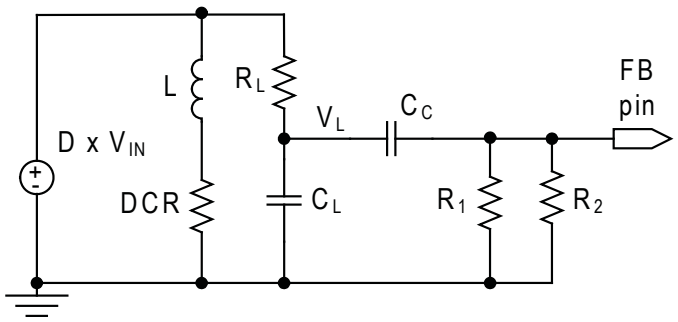


Figure 11 — FB Voltage by CL Voltage

It is shown by the following equation.

$$VFBc_L = Vc_L \times \frac{(R_1 // R_2) \times S \times C_C}{(R_1 // R_2) \times S \times C_C + 1}$$

Figure 12 shows the magnitude of the ripple contribution due to the output voltage ripple at the FB pin.

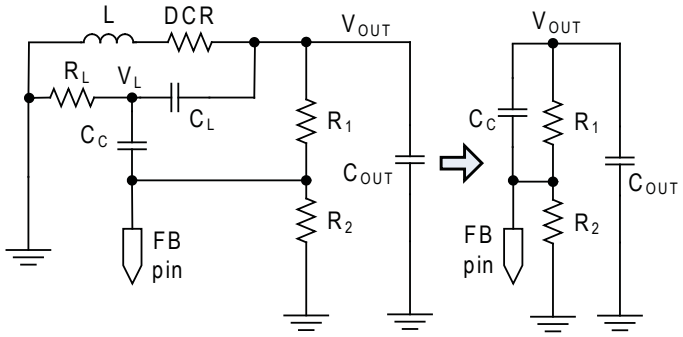


Figure 12 — FB Voltage by Output Voltage

It is shown by the following equation.

$$VFB\Delta V_{OUT} = \Delta V_{OUT} \times \frac{R_2}{R_1 // \frac{1}{S \times C_C} + R_2}$$

The purpose of this network is to couple the inductor current ripple information into the feedback voltage such that the feedback voltage has 90 degrees phase lag to the switching node similar to the case of using standard high ESR capacitors. This is illustrated in Figure 13.

Applications Information (continued)

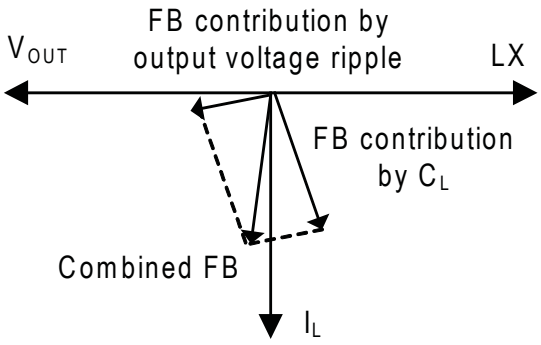


Figure 13 — FB voltage in Phasor Diagram

The magnitude of the feedback ripple voltage, which is dominated by the contribution from C_L, is controlled by the value of R_1, R_2 and C_C. If the corner frequency of (R_1// R_2) x C_C is too high, the ripple magnitude at the FB pin will be smaller, which can lead to double-pulsing. Conversely, if the corner frequency of (R_1// R_2) x C_C is too low, the ripple magnitude at FB pin will be higher. Since the SC9301 regulates to the valley of the ripple voltage at the FB pin, a high ripple magnitude is undesirable as it significantly impacts the output voltage regulation. As a result, it is desirable to select a corner frequency for (R_1// R_2) x C_C to achieve enough, but not excessive, ripple magnitude and phase margin. The component values for R_1, R_2, and C_C should be calculated using the following procedure.

Select C_L (typical 10nF) and R_L to match with L and DCR time constant using the following equation.

$$R_L = \frac{L}{DCR \times C_L}$$

Select C_C by using the following equation.

$$C_C \approx \frac{1}{R_1 // R_2} \times \frac{3}{2 \times \pi \times f_{sw}}$$

The resistor values (R_1 and R_2) in the voltage divider circuit set the V_{OUT} for the switcher. The typical value for C_C is from 10pF to 1nF.

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 250ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the following equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 600mV, $\pm$1%.

The on-time pulse from the SC9301 in the design example is calculated to give a pseudo-fixed frequency of 250kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because adaptive on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with V_{IN} = 25V, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1% feedback resistors contributes up to 1% error. If tighter DC accuracy is required, 0.1% resistors should be used.

Applications Information (continued)

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variations

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage.

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A adaptive on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). Because the on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the off-time will reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

PCB Layout Guidelines

The optimum layout for the SC9301 is shown in Figure 16. This layout shows an integrated FET buck regulator with a maximum current of 10A. The total PCB area is approximately 25 x 29 mm with single side components.

Critical Layout Guidelines

The following critical layout guidelines must be followed to ensure proper performance of the device.

- IC Decoupling capacitors
- PGND plane
- AGND island
- FB, VOUT, and other analog control signals
- C_{SS}
- BST, ILIM, and LX
- C_{IN} and C_{OUT} placement and Current Loops

IC Decoupling Capacitors

- A 1 µF capacitor must be located as close as possible to the IC and directly connected to pins 3 (VDD) and 4 (AGND).
- Another 1 µF capacitor must be located as close as possible to the IC and directly connected to pins 3 (VDD) and PGND plane.

PGND Plane

- PGND requires its own copper plane with no other signal traces routed on it.
- Copper planes, multiple vias and wide traces are needed to connect PGND to input capacitors, output capacitors, and the PGND pins on the IC.
- The PGND copper area between the input capacitors, output capacitors and PGND pins must be as tight and compact as possible to reduce the area of the PCB that is exposed to noise due to current flow on this node.

AGND Island

- AGND should have its own island of copper with no other signal traces routed on this layer that connects the AGND pins and pad of the IC to the analog control components.
- All of the components for the analog control circuitry should be located so that the connections to AGND are done by wide copper traces or vias down to AGND.

Applications Information (continued)

- Connect PGND to AGND with a short trace or 0Ω resistor. This connection should be as close to the IC as possible.

FB, VOUT, and Other Analog Control Signals

- The connection from the V_{OUT} power to the analog control circuitry must be routed from the output capacitors and located on a quiet layer.
- The traces between Vout and the analog control circuitry (VOUT, and FB pins) must be wide, short and routed away from noise sources, such as BST, LX, VIN, and PGND between the input capacitors, output capacitors, and the IC.
- The feedback components for the switcher and the LDO need to be as close to the FB and FBL pins of the IC as possible to reduce the possibility of noise corrupting these analog signals.

BST, ILIM,TON,SS and LX

- The connections for the boost capacitor between the BST and LXBST must be short, wide and directly connected.
- ILIM and TON nodes must be as short as possible to ensure the best accuracy in current limit and on time.
- R_{ILIM} should be close to the IC and connected between LXS (pin 28) and ILIM (pin 27) only.
- R_{TON} should be close to the IC and connected between TON (pin 31) and AGND (pin 30).
- C_{SOFT} should be close to the IC and kept away from the boost capacitor. Connect the AGND end of C_{SOFT} to the AGND plane at pin 4.
- The LX node between the IC and the inductor should be wide enough to handle the inductor current and short enough to eliminate the possibility of LX noise corrupting other signals.
- Multiple vias should be used on the LX PAD to provide good thermals and connection to an internal or bottom layer LX plane.

Capacitors and Current Loops

- Figure 14 shows the placement of input/output capacitors and inductor. This placement shows the smallest current loops between the input/output capacitors, the SC9301 and the inductor to reduce the IR drop across the copper.

Applications Information (continued)

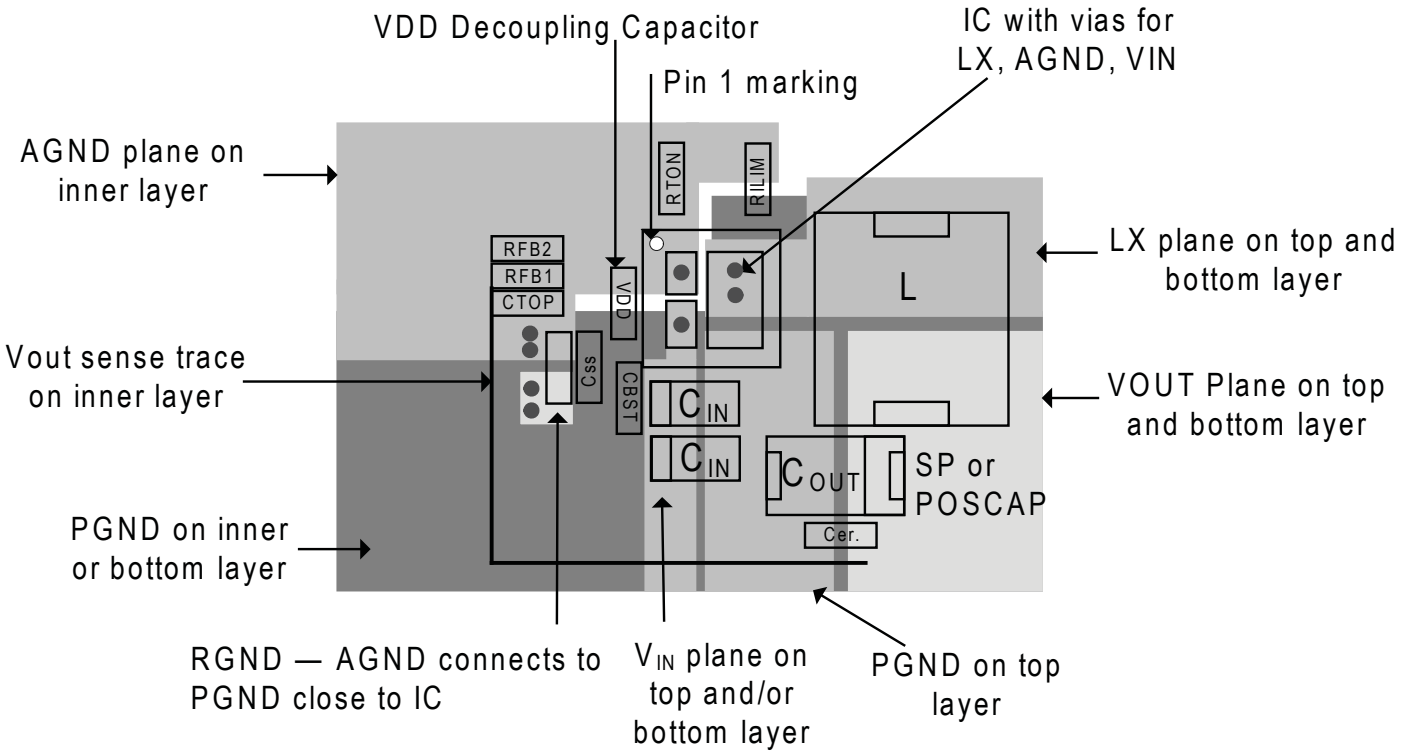
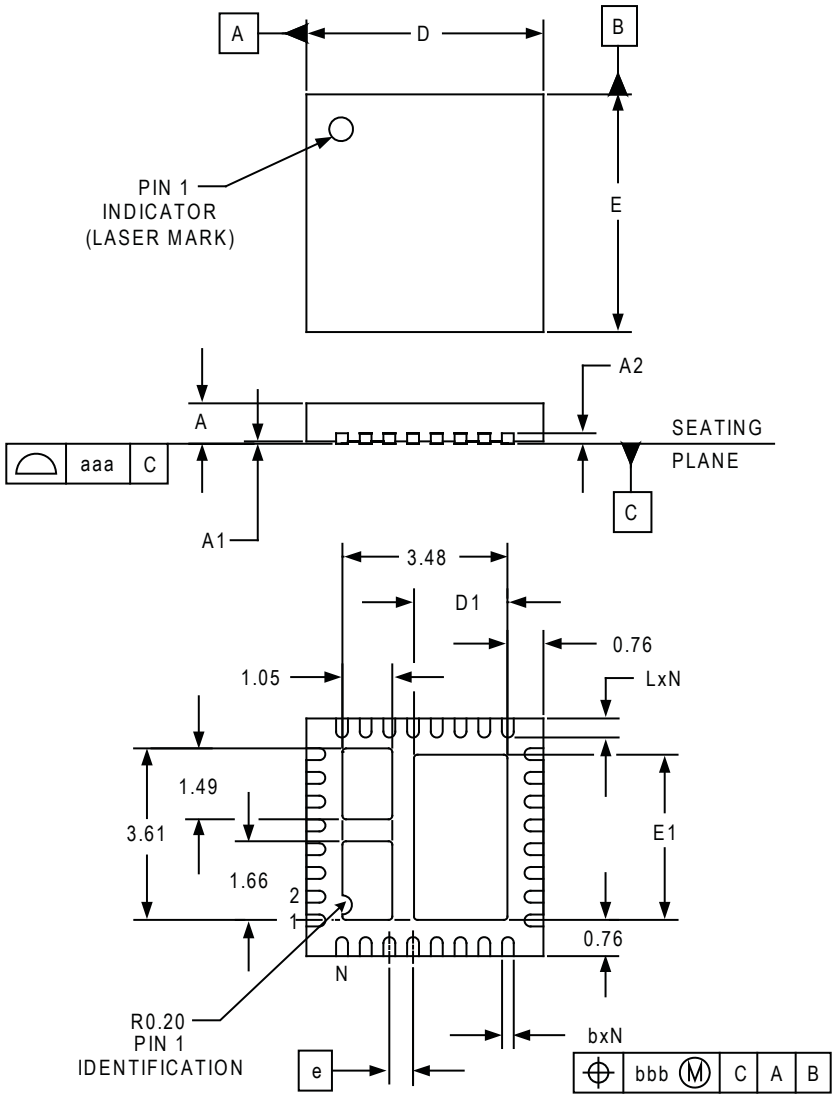


Figure 14 — PCB Layout

Outline Drawing — MLPQ-UT32 5x5

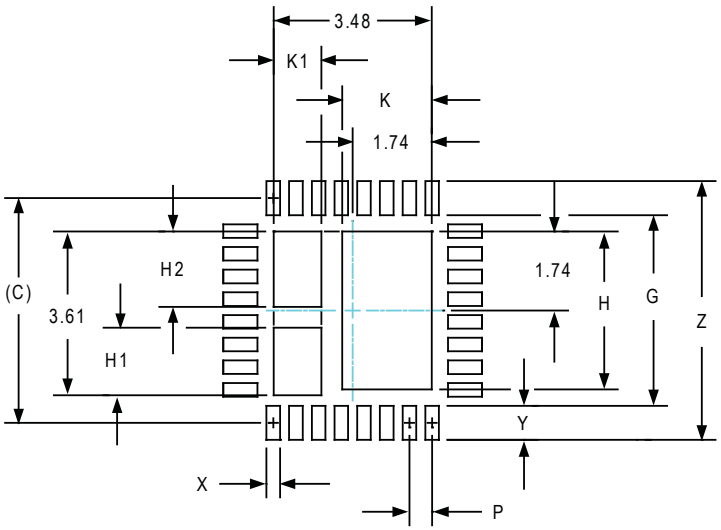


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.076	.078	.080	1.92	1.97	2.02
E	.193	.197	.201	4.90	5.00	5.10
E1	.135	.137	.139	3.43	3.48	3.53
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern — MLPQ-UT32 5x5



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.195)	(4.95)
G	.165	4.20
H	.137	3.48
H1	.059	1.49
H2	.065	1.66
K	.078	1.97
K1	.041	1.05
P	.020	0.50
X	.012	0.30
Y	.030	0.75
Z	.224	5.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

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