

PROTECTION PRODUCTS

Description

The SMF series TVS arrays are designed to protect sensitive electronics from damage or latch-up due to ESD and other voltage-induced transient events. They are designed for use in applications where board space is at a premium. Each device will protect up to four lines. They are unidirectional devices and may be used on lines where the signal polarities are above ground.

TVS diodes are solid-state devices designed specifically for transient suppression. They feature large cross-sectional area junctions for conducting high transient currents. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

The SMF series devices may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SC70 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.

Features

- ◆ Transient protection for data lines to **IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air), $\pm 8\text{kV}$ (contact)**
IEC 61000-4-4 (EFT) 40A (5/50ns)
- ◆ Small package for use in portable electronics
- ◆ Protects four I/O lines
- ◆ Working voltage: 5V and 12V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages
- ◆ Solid-state silicon-avalanche technology

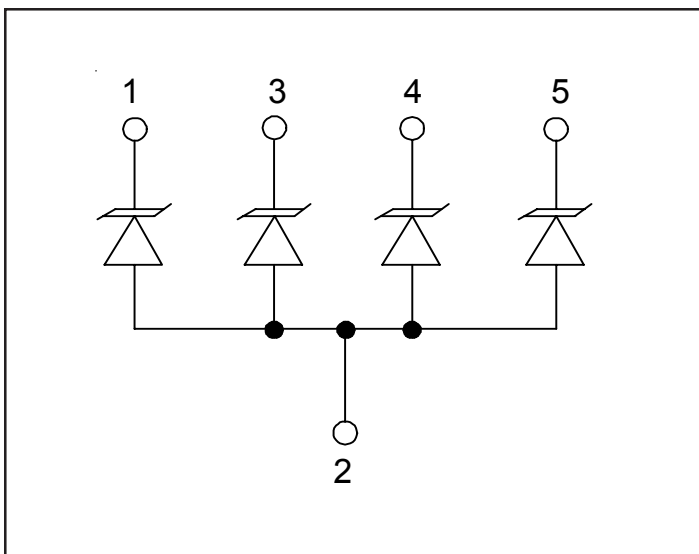
Mechanical Characteristics

- ◆ EIAJ SC70-5L package
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : Marking Code
- ◆ Packaging : Tape and Reel

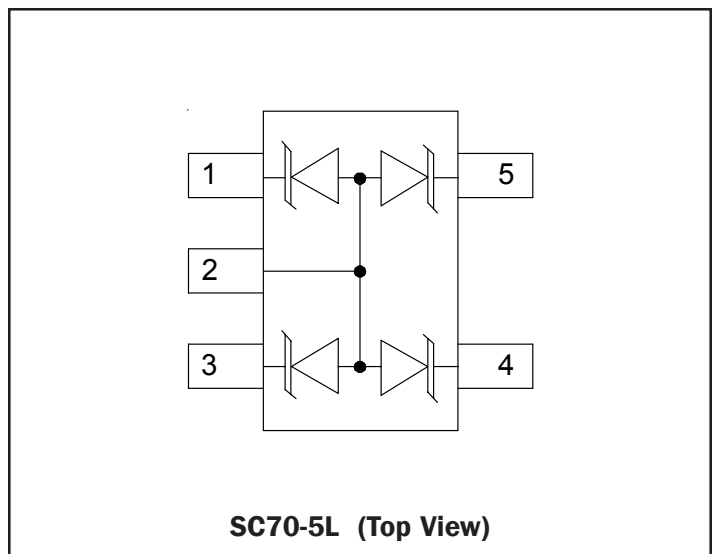
Applications

- ◆ Cellular Handsets and Accessories
- ◆ Cordless Phones
- ◆ Personal Digital Assistants (PDA's)
- ◆ Notebooks & Handhelds
- ◆ Portable Instrumentation
- ◆ Digital Cameras
- ◆ Peripherals
- ◆ MP3 Players

Circuit Diagram



Schematic & PIN Configuration



PROTECTION PRODUCTS
Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{pk}	200	Watts
Peak Forward Voltage ($I_F = 1A, t_p=8/20\mu s$)	V_{FP}	1.5	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	20 15	kV
Lead Soldering Temperature	T_L	260 (10 seconds)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics

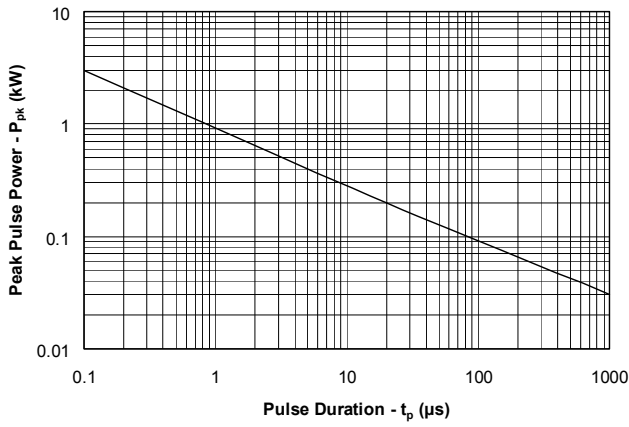
SMF05						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	6			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T=25^\circ C$			10	μA
Clamping Voltage	V_C	$I_{PP} = 1A, t_d = 8/20\mu s$			9.5	V
Clamping Voltage	V_C	$I_{PP} = 12A, t_d = 8/20\mu s$			12.5	V
Peak Pulse Current	I_{PP}	$t_d = 8/20\mu s$			12	A
Junction Capacitance	C_j	Between I/O pins and Ground $V_R = 0V, f = 1MHz$		150	175	pF

SMF12						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	$I_t = 1mA$	13.3			V
Reverse Leakage Current	I_R	$V_{RWM} = 12V, T=25^\circ C$			1	μA
Clamping Voltage	V_C	$I_{PP} = 1A, t_d = 8/20\mu s$			19	V
Clamping Voltage	V_C	$I_{PP} = 8A, t_d = 8/20\mu s$			25	V
Peak Pulse Current	I_{PP}	$t_d = 8/20\mu s$			8	A
Junction Capacitance	C_j	Between I/O pins and Ground $V_R = 0V, f = 1MHz$		60	75	pF

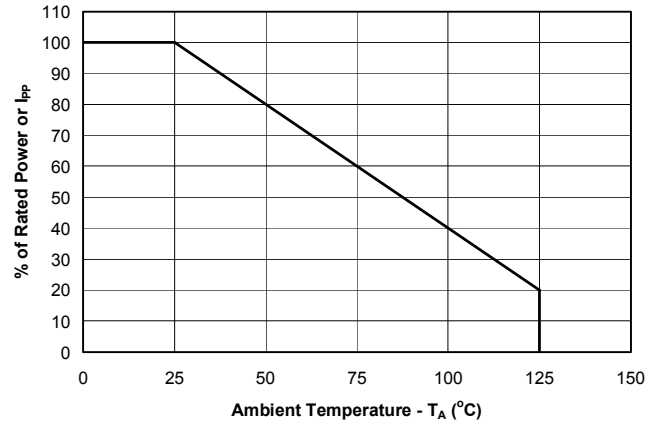
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Typical Characteristics

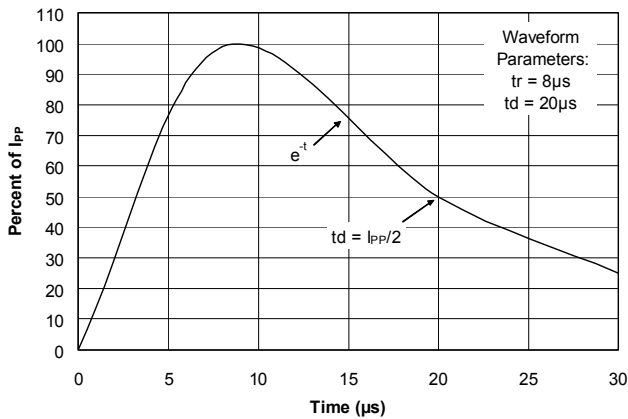
Non-Repetitive Peak Pulse Power vs. Pulse Time



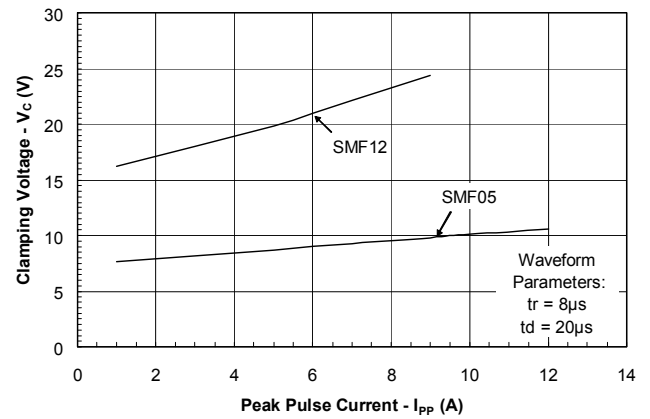
Power Derating Curve



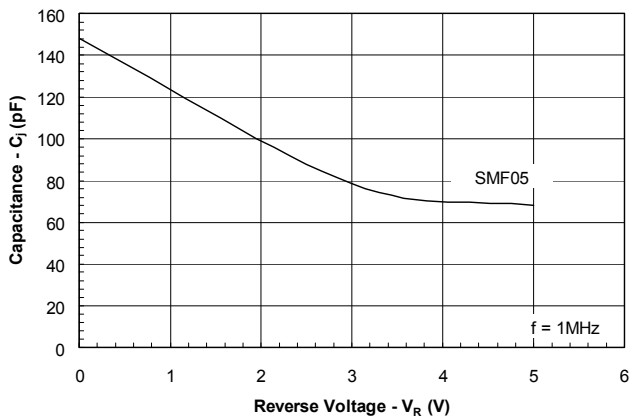
Pulse Waveform



Clamping Voltage vs. Peak Pulse Current



Capacitance vs. Reverse Voltage



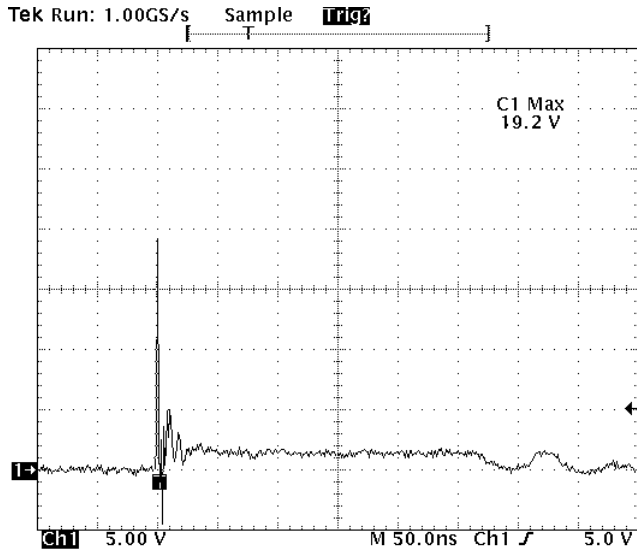
SMF05 Insertion Loss S21



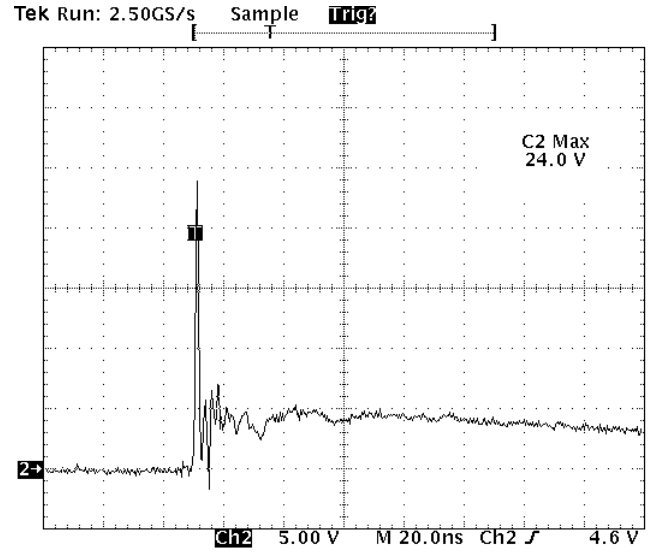
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Typical Characteristics (Continued)

SMF05 ESD Clamping
(8kV Contact per IEC 61000-4-2)



SMF12 ESD Clamping
(8kV Contact per IEC 61000-4-2)



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Applications Information

Device Connection for Protection of Four Data Lines

The SMFxx is designed to protect up to four unidirectional data lines. The device is connected as follows:

1. Unidirectional protection of four I/O lines is achieved by connecting pins 1, 3, 4, and 5 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

Circuit Board Layout Recommendations for Suppression of ESD.

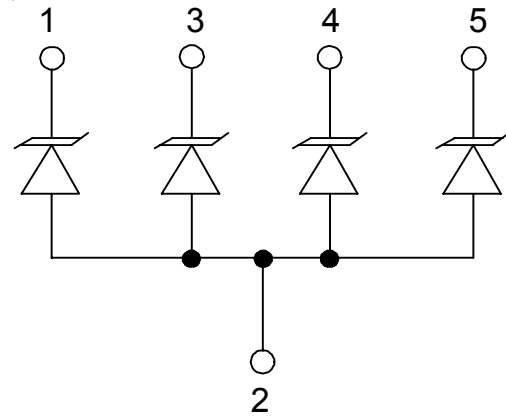
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the SMFxx near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the SMFxx and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

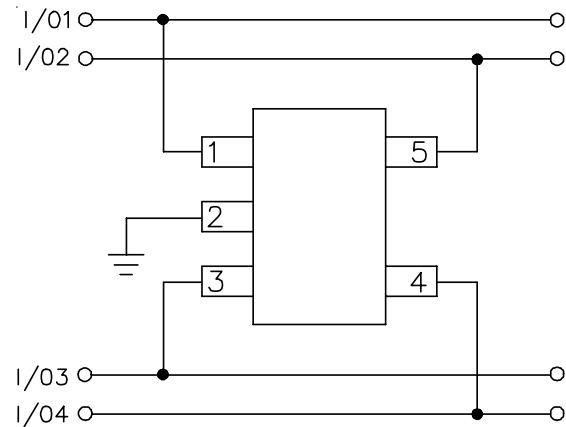
Matte Tin Lead Finish

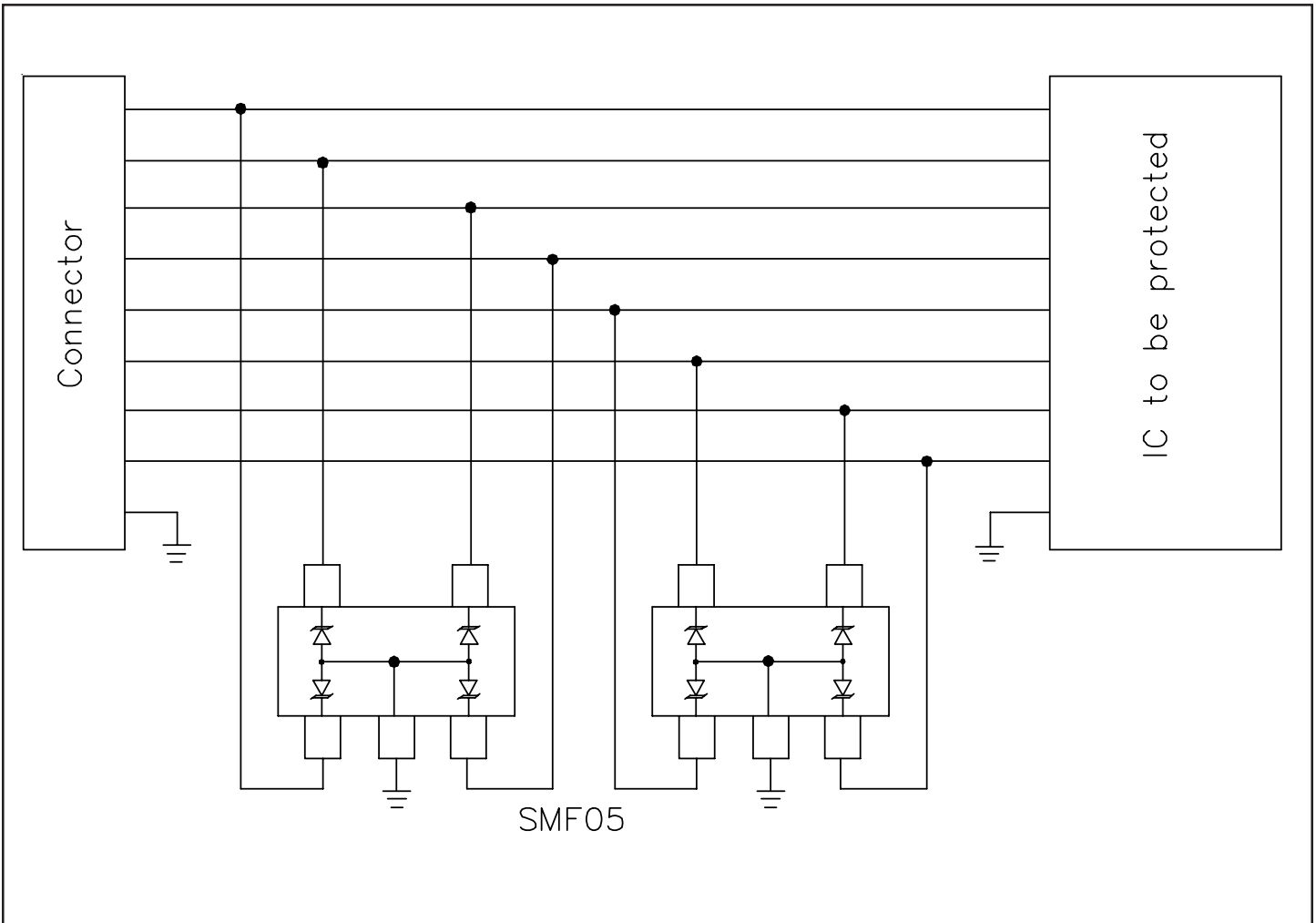
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

SMF Circuit Diagram



Protection of Four Unidirectional Lines



PROTECTION PRODUCTS**Typical Applications**

PROTECTION PRODUCTS**Marking Codes**

Part Number	Marking Code
SMF05	F05
SMF12	F12

Ordering Information

Part Number	Lead Finish	Qty per Reel	Reel Size
SMF05.TC	SnPb	3,000	7 Inch
SMF12.TC	SnPb	3,000	7 Inch
SMF05.TCT	Pb free	3,000	7 Inch
SMF12.TCT	Pb free	3,000	7 Inch

Contact Information

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