## TRIUNE PRODUCTS

## Features

- Ultra-low nA operating current at light load
- Best-in-class quiescent current of 20nA at Iload=0
- Best-in-class quiescent current of 100pA in disable mode
- Output voltage options of $1.2 \mathrm{~V}-4.2 \mathrm{~V}$ in 100 mV steps (programmed at manufacturing)
- Accurate output regulation
- Over-current protection


## Summary Specifications

- Low input operating voltage of 2.5 V to 5.5 V
- Packaged in a 8pin DFN (2x2)
- Product is lead-free, Halogen Free, RoHS / WEEE compliant


## Description

The TS14002 linear regulator is an ultra-low-power circuit which draws low nA level quiescent current at light load, but has the capability to regulate current loads as high as 150 mA .

## Applications

- Portable electronics
- RFID
- Industrial
- Medical
- Energy harvesting systems
- SmartCard


## Typical Applications



## Block Diagram



## Pin Description

| Pin \# | Pin Name | Pin Type ${ }^{(1)}$ | Description |
| :---: | :---: | :---: | :---: |
| 1 | GND | P | Ground |
| 2 | $V_{\text {out }}$ | O | Regulated Output Voltage |
| 3 | NC |  | No Connect (connect to GND or float) |
| 4 | NC | No Connect (connect to GND or float) |  |
| 5 | NC | No Connect (connect to GND or float) |  |
| 6 | FB | Feedback Input |  |
| 7 | $V_{\text {cc }}$ | P | Input Power |
| 8 | EN | I | Enable Input |

(1) I = Input, $0=$ Output, $\mathrm{P}=$ Power

## Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted ${ }^{(2,3,4)}$

| Parameter | Value | Unit |
| :--- | :---: | :---: |
| $\mathrm{V}_{\text {cC }}, \mathrm{V}_{\text {our }}$, EN, FB | -0.3 to 6.0 | V |
| Electrostatic Discharge (Human Body Model) | 2 | kV |
| Operating Junction Temperature Range, $\mathrm{T}_{\mathrm{J}}$ | -40 to 85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature Range, $\mathrm{T}_{\text {sT }}$ | -65 to 150 | ${ }^{\circ} \mathrm{C}$ |
| Reflow Temperature (soldering, 10 seconds) | 260 | ${ }^{\circ} \mathrm{C}$ |

(2) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(3) All voltage values are with respect to network ground terminal.
(4) ESD testing is performed according to the respective JESD22 JEDEC standard.

## Thermal Characteristics

| Package DFN | 日JA $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ <br> $($ See Note 5) | 日JC $\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$ <br> $($ See Note 6) |
| :--- | :---: | :---: |
| 8 pin | 73.1 | 10.7 |

(5) This assumes a FR4 board only.
(6) This assumes a 1 Oz. Copper JEDEC standard board with thermal vias - See Exposed Pad section and application note for more information.

## Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: |
| Unregulated Supply Input Voltage $\left(\mathrm{V}_{\text {cc }}\right)$ | 2.5 |  | 5.5 | V |
| Enable Input (EN) | 0 |  | 5 | V |
| Regulated Supply Output Voltage $\left(\mathrm{V}_{\text {out }}\right.$ ) typical | 1.2 |  | 4.2 | V |
| Operating Ambient Temperature, TA (Note 7) | -40 |  | 55 | ${ }^{\circ} \mathrm{C}$ |
| Operating Junction Temperature, $\mathrm{T}_{\mathrm{J}}$ | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |
| Input Bypass Capacitor $\left(\mathrm{C}_{\text {BY> }}\right)$ |  | 2.2 |  | uF |
| Output Bypass Capacitor $\left(\mathrm{C}_{\text {out }}\right)$ | 1 | 2.2 | 4.7 | uF |

(7) $T_{A}$ Max shown here is a guideline. Higher $T_{A}$ can be tolerated if $T_{\text {, }}$ does not exceed the Absolute Maximum Rating.

## Characteristics

Electrical characteristics, $\mathrm{V}_{\mathrm{CC}}=2.5 \mathrm{~V}$ to $5.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25 \mathrm{C}, \mathrm{C}_{\text {OUT }}=2.2 \mathrm{uF}$ unless otherwise noted

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{cc}}$ | Input Supply Voltage |  | 2.5 |  | 5.5 | V |
| $\mathrm{Vil}_{\text {en }}$ | Input Low Logic Level |  |  |  | $0.3{ }^{*} \mathrm{VCC}$ | v |
| $\mathrm{Vih}_{\text {EN }}$ | Input High Logic Level |  | 0.7*VCC |  |  | v |
| $\mathrm{I}_{\text {q9 }}$ | Quiescent Current (note 9) | $\begin{gathered} \mathrm{V}_{\text {cc }}=2.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V}, \mathrm{I}_{\text {out }}=0 \\ \text { (Note } 9) \end{gathered}$ |  | 20 |  | nA |
| $\mathrm{I}_{\text {qadidisable }}$ | Quiescent Current: Disable Mode | $\mathrm{l}_{\text {OUT }}=0, \mathrm{EN}=0$ |  | 100 |  | pA |
| Op.gnd | Operating Current | $\begin{gathered} \mathrm{V}_{\mathrm{cc}}=\mathrm{V}_{\text {ccanv. }} \mathrm{I}_{\text {out }}=150 \mathrm{~mA} \\ \text { (Note 8) } \end{gathered}$ |  | 200 |  | uA |
| ${ }^{\text {out }}$ | Load Capability | Vout ${ }_{\text {nominal }}$ from 1.2 V to 3.5 V | 0 |  | 150 | mA |
|  |  | $\mathrm{Vout}_{\text {nominal }}>3.5 \mathrm{~V}$ | 0 |  | 100 |  |
| (8) If Vout $\qquad$ $<2.5 \mathrm{~V}$, then $\mathrm{V}_{\text {cc_min }}=2.5 \mathrm{~V}$, otherwise $\mathrm{V}_{\text {cc_MIN }}=$ Vout <br> (9) Not tested in production, but has been evaluated on samples |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |

## Characteristics Continued

Electrical characteristics, $\mathrm{V}_{\mathrm{cc}}=2.5 \mathrm{~V}$ to $5.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{J}}=25 \mathrm{C}$, unless otherwise noted

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {Line }}$ | DC Line Regulation | $\begin{gathered} \mathrm{V}_{\text {cc }}=\mathrm{V}_{\text {cc, MIN }} \text { to } \mathrm{V}_{\text {cC_max }} \\ \mathrm{V}_{\text {out }}=1.8 \mathrm{~V} \text { to } 4.2 \mathrm{~V}, \\ \mathrm{I}_{\text {out }}=50 \mathrm{~mA} \end{gathered}$ |  | 0.5 | 4 | \% |
|  |  | $\begin{gathered} \mathrm{V}_{\text {cC }}=\mathrm{V}_{\text {cC_MIN }} \text { to } \mathrm{V}_{\text {cC_MAX }} \\ \mathrm{V}_{\text {OUT }}<1.8 \mathrm{~V}, \\ \mathrm{I}_{\text {OUT }}=50 \mathrm{~mA} \end{gathered}$ |  |  | 4 | \% |
| $\mathrm{V}_{\text {Load }}$ | DC Load Regulation | $\begin{gathered} V_{\text {cc }}=V_{\text {cC NoM }} \\ \mathrm{I}_{\text {out }}=0.02 \mathrm{~mA} \text { to } 150 \mathrm{~mA}, \end{gathered}$ |  | 1 | 3 | \% |
| $\mathrm{I}_{\text {limit }}$ | Short circuit current limit | Vout forced to GND (Note 9) | 185 | 200 |  | mA |

(9) Not tested in production, but has been evaluated on samples

## Typical Characteristics








Dropout Voltage When $\mathrm{V}_{\text {out }}$ Drops By 3\%


Load Step Response


Load Step Response


Load Regulation Performance


Load Step Response


Line Step Response




## Package Mechanical Drawings (all dimensions in mm)



Marking for the $2.0 \times 2.0 \mathrm{~mm}$ MLPD 8 Lead package:
nnn = Part Number (Example: TS4) - Reference Part No. Code for small MLP yw = Datecode (Reference Package Marking Design Guide lines, Appendix A)

$\oplus|0.10 \otimes| C|A| B$
$0.05(1)$ C
BOTTOM VIEW

|  | UnitsDimension Limits | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX |
| Number of Pins | N |  | 8 |  |
| Pitch | e |  | 0.50 BSC |  |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 |  | 0.20 REF |  |
| Overall Length | D |  | 2.00 BSC |  |
| Exposed Pad Width | E2 | 0.75 | 0.90 | 1.00 |
| Overall Width | E |  | 2.00 BSC |  |
| Exposed Pad Length | D2 | 1.55 | 1.70 | 1.80 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.30 | 0.40 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:
Dimensions and tolerances per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact values shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information only.

## Recommeded PCB Land Pattern



RECOMMENDED
LAND PATTERN

DIMENSIONS IN MILLIMETERS

|  | UnitsDimension Limits | MILLIMETERS |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX |
| Contact Pitch | E |  | . 50 BSC |  |
| Optional Center Pad Width | W2 | - | - | 1.70 |
| Optional Center Pad Length | T2 | - | - | 0.90 |
| Contact Pad Spacing | C1 | - | 2.00 | - |
| Contact Pad Spacing | C2 | - | - | - |
| Contact Pad Width (X8) | X1 | - | - | 0.35 |
| Contact Pad Length (X8) | Y1 | - | - | 0.65 |
| Distance Between Pads | G | 0.15 | - | - |

## Ordering Information

TS14002--CvvvDFNR

| Part Number | Description |
| :---: | :---: |
| vvv | Output Voltage* |
| 012 | 1.2 V |
| 015 | 1.5 V |
| 018 | 1.8 V |
| 020 | 2.0 V |
| 023 | 2.3 V |
| 025 | 2.5 V |
| 028 | 2.8 V |
| 030 | 3.0 V |
| 033 | 3.3 V |
| 042 | 4.2 V |

* Custom values also available (1.2V - 4.2V typical in 100 mV increments)


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