# uClamp6514P

## 65V µClamp®
## 4-Line, Surge & ESD Protection

**PROTECTION PRODUCTS**

## Description

µClamp® TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD. They feature large cross-sectional area junctions for conducting high transient currents. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

µClamp®6514P is in a 10-pin SGP2510P8 package measuring 2.5 x 1.0mm with a nominal height of only 0.60mm. Leads are finished with lead-free NiPdAu. Each line features a minimum breakdown voltage of 65V. This device gives the designer flexibility to replace multiple single line devices in space constrained applications. Flow through package design simplifies PCB layout. uClamp6514P may be used to meet the ESD immunity requirements of IEC 61000-4-2. The combination of high ESD surge capability and innovative package design makes them ideal for use in applications such as LCD Televisions, monitors, and industrial equipment.

## Features

- High ESD Withstand Voltage
  - IEC 61000-4-2 (ESD) +/-8kV (contact)
- Protects up to Four VBus Lines
- Flow-Through Package
- Minimum Breakdown Voltage: 65V
- Low reverse current: <10nA typical (VR=60V)
- Solid-State Silicon-Avalanche Technology

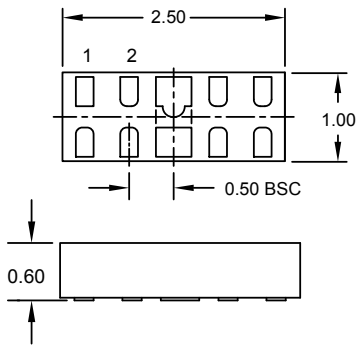
## Mechanical Characteristics

- SGP2510P8 Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 2.5 x 1.0 x 0.60 mm
- Lead Finish: NiPdAu
- Marking : Marking Code + Date Code
- Packaging : Tape and Reel

## Applications

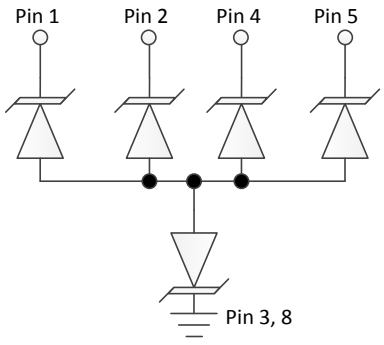
- Chip-On-Glass (COG) Panels
- VBus Protection
- LCD Televisions
- OLED Panels
- Set Top Box
- Industrial Equipment

## Nominal Dimensions




**Nominal Dimensions in mm**

## Schematic




**4-Line, Bidirectional**

## Absolute Maximum Ratings

| Rating | Symbol | Value | Units |
|---|---|---|---|
| Peak Pulse Power | $P_{PK}$ | 240 | W |
| Peak Pulse Current (tp = 8/20µs) | $I_{PP}$ | 2 | A |
| ESD per IEC 61000-4-2 (Contact)(1) | $V_{ESD}$ | ±8 | kV |
| Operating Temperature | $T_J$ | -25 to +85 | $^oC$ |
| Storage Temperature | $T_{STG}$ | -55 to +150 | $^oC$ |

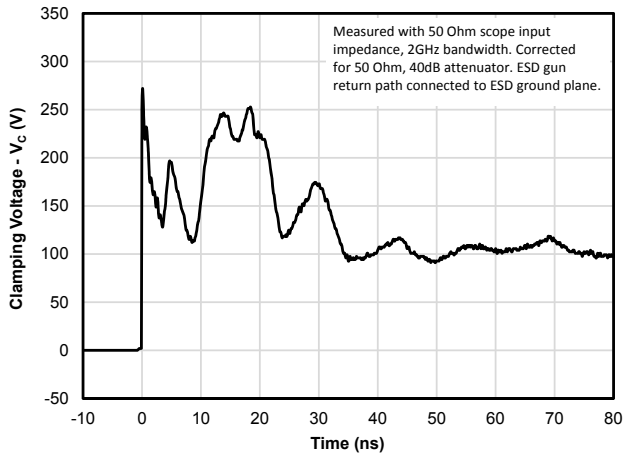
## Electrical Characteristics (T=25$^o$C unless otherwise specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| Reverse Stand-Off Voltage | $V_{RWM}$ | Pins 1, 2, 4, and 5 to Pins 3 & 8 | -25$^o$C to 85$^o$C | | | 60 | V |
| Reverse Breakdown Voltage | $V_{BR}$ | $I_{BR}$ = 1mA Pins 1, 2, 4, and 5 to Pins 3 & 8 | -25$^o$C to 85$^o$C | 65 | 75 | 85 | V |
| Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 60V Pins 1, 2, 4, and 5 to Pins 3 & 8 | T = 25$^o$C | | <10 | 100 | nA |
| | | | T = 85$^o$C | | <10 | 150 | nA |
| Clamping Voltage[2] | $V_C$ | $I_{PP}$ = 2A, tp = 8/20µs Pins 1, 2, 4, and 5 to Pins 3 & 8 | | | 105 | 120 | V |
| Junction Capacitance | $C_J$ | $V_R$ = 0V, f = 1MHz Pins 1, 2, 4, and 5 to Pins 3 & 8 | T = 25$^o$C | | 8.5 | 10.5 | pF |

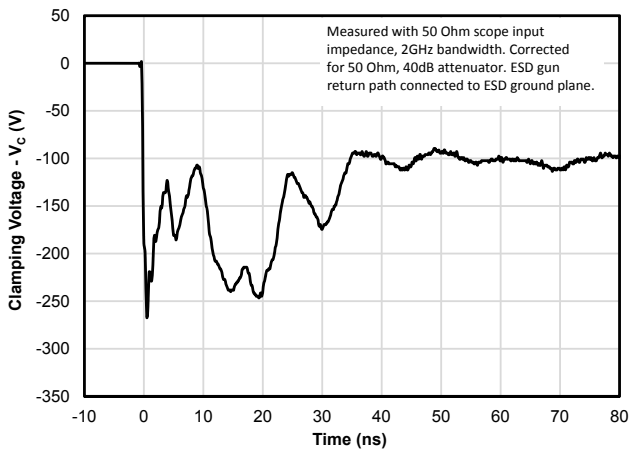
Notes:
(1) Measured with a 40dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to Ground Reference Plane (GRP)
(2) Measured using a 1.2/50us voltage, 8/20us current combination waveform. Clamping is defined as the peak voltage across the device after the device snaps back to a conducting state.
(3) Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, $I_{TLP}$ and $V_{TLP}$ averaging window: $t_1$ = 70ns to $t_2$ = 90ns.
(4) Dynamic resistance calculated from $I_{TLP}$ = 4A to $I_{TLP}$ = 16A

# Typical Characteristics

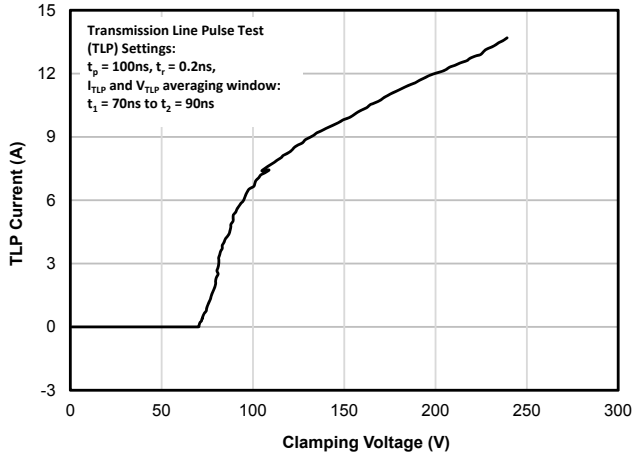
### ESD Clamping (+8kV Contact per IEC 61000-4-2)



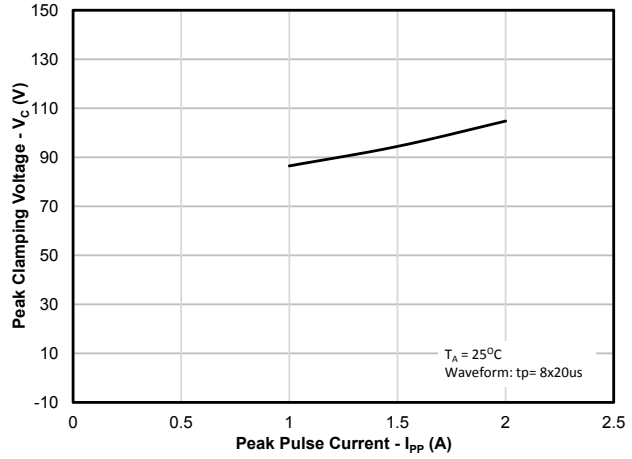

### ESD Clamping (-8kV Contact per IEC 61000-4-2)



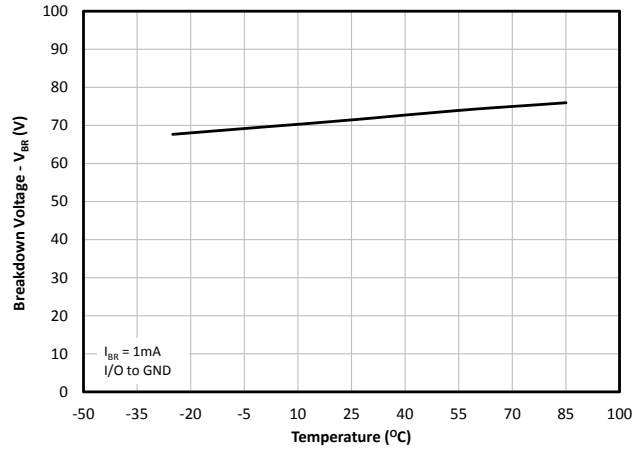

### TLP IV Curve



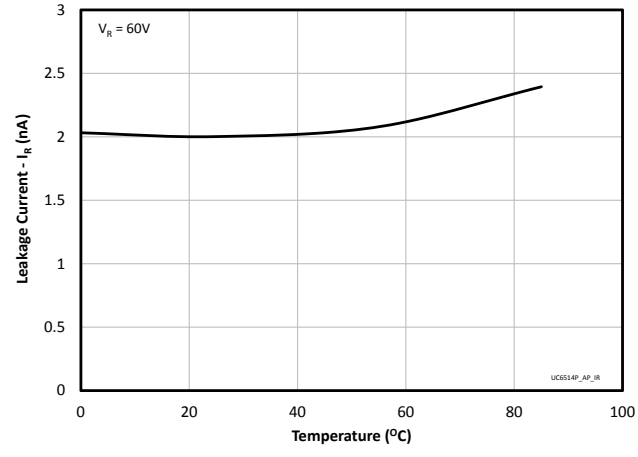

### Clamping Voltage vs. Peak Pulse Current




### Breakdown Voltage vs. Temperature




### Reverse Leakage Current (IR) vs. Temperature



# Application Information

**VBus Protection of Chip-On-Glass (COG) Displays**

LCD displays are often supplied as a module with a built-in driver circuitry mounted on a PCB at the rear of the module. This mechanically strengthens the display module, but it also increases the thickness (of the display module) and raises the manufacturing cost. Chip-On-Glass (COG) modules integrate the circuit driving the display mounts directly on the display glass, thus reducing the overall thickness of the module. The advantages of COG technology make it an attractive option for commercial, automotive, and industrial applications. Power is supplied to the modules from a PMIC on the control. These voltage bus lines are susceptible to ESD/EOS events and require external protection devices.

**Protection Solutions**

Figure 1 below is a simplified block diagram of an LCD panel circuit. The driver ICs are located on the TFT array substrate. This array is connected to a source board which supplies power and data via a flex circuit. The timing controller or T-Con board supplies the VBus power to the source board from an on-board PMIC. uClamp6514P (2 each) are located on the source board near the flex circuit. An example of how to route the traces is shown in Figure 2. VBus lines from the PMIC are routed through each device entering at pins 1, 2, 4, and 5 and exiting at pins 10, 9, 7, and 6 respectively. Each trace should run under the device and connect the pins together. For example, the trace for VBus 1 would enter at pin 1 and exit at pin 10 and so on. Ground connection is made at the center tabs (pins 3, and 8 ).

**Design Verification**

Verification of the ESD design is always recommended. In this case, ESD contact discharges are applied at the source board on the VBus traces. An IEC 61000-4-2 compliant waveform is recommended.

**Figure 1 - COG Protection Solution**

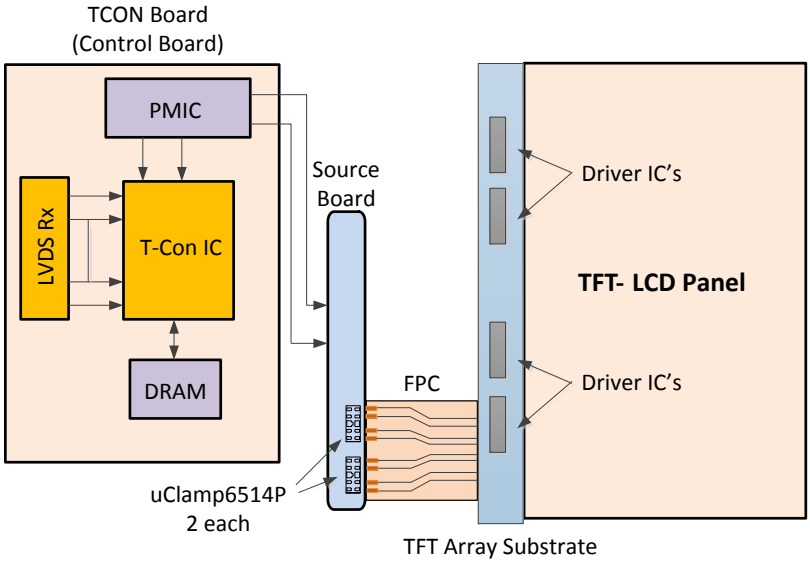
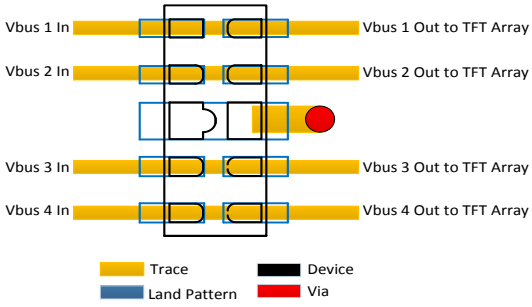
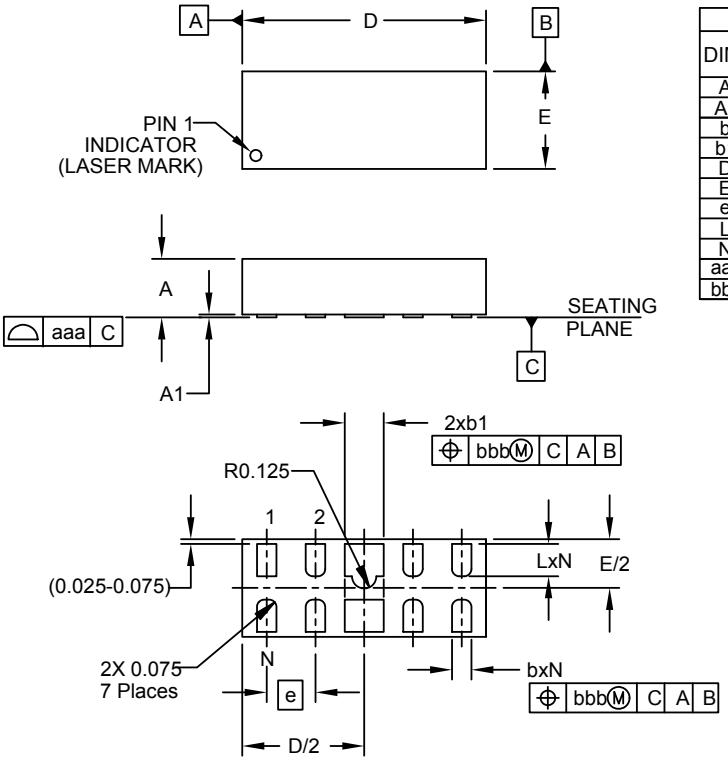



**Figure 2 - uClamp6514P Trace Routing**



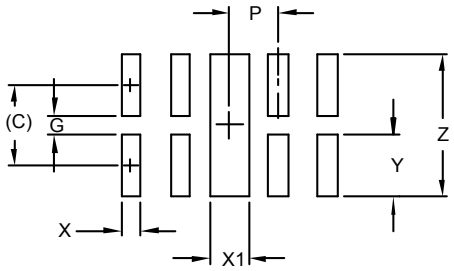
## Outline Drawing - SGP2510P8




| DIMENSIONS | | | |
|---|---|---|---|
| DIM | MILLIMETERS | | |
| | MIN | NOM | MAX |
| A | 0.57 | 0.60 | 0.63 |
| A1 | 0.00 | 0.03 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| b1 | 0.35 | 0.40 | 0.45 |
| D | 2.45 | 2.50 | 2.575 |
| E | 0.95 | 1.00 | 1.075 |
| e | 0.50 BSC | | |
| L | 0.28 | 0.33 | 0.38 |
| N | 8 | | |
| aaa | 0.08 | | |
| bbb | 0.10 | | |

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

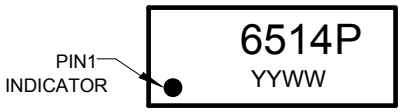
## Land Pattern - SGP2510P8




| DIMENSIONS | |
|---|---|
| DIM | MILLIMETERS |
| C | (0.825) |
| G | 0.20 |
| P | 0.50 |
| X | 0.20 |
| X1 | 0.40 |
| Y | 0.625 |
| Z | 1.45 |

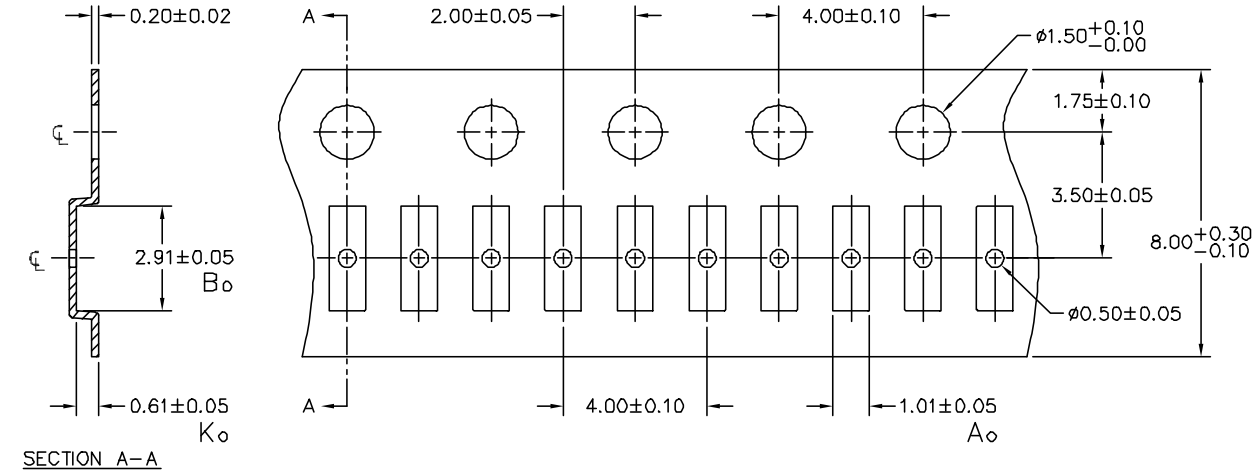
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

## Marking Code

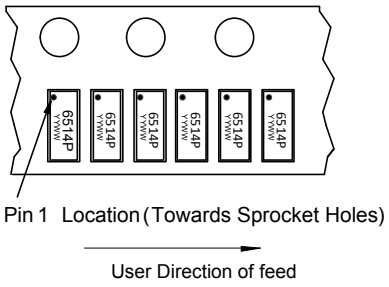



Notes: YYWW = Alphanumeric Date Code

## Tape and Reel Specification




NOTES: 1.) ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.




## Ordering Information

| Part Number | Qty per Reel | Reel Size |
|---|---|---|
| uClamp6514P.TNT | 10000 | 7 Inch |

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## Contact Information

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