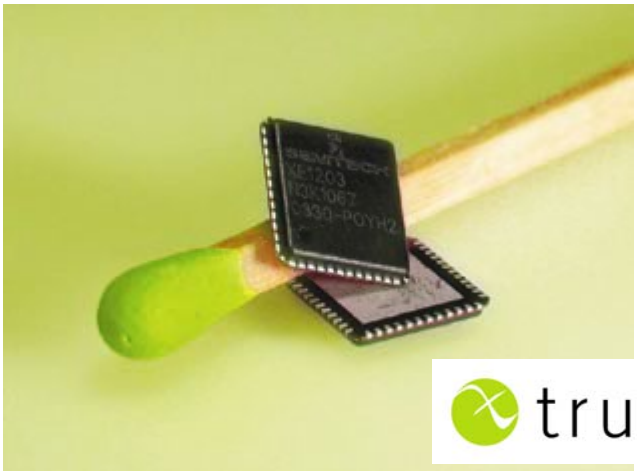


XE1203F

433 MHz / 868 MHz / 915 MHz

Low-Power, Integrated UHF Transceiver

GENERAL DESCRIPTION

The XE1203F is a single chip transceiver operating in the 433, 868 and 915 MHz license-free ISM (Industry Scientific and Medical) frequency bands. Its highly integrated architecture allows for minimum external components while maintaining design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set. The XE1203F offers the excellent advantage of high data rate communication at rates of up to 152.3 kbit/s, without the need to modify the number or parameters of the external components. The XE1203F is optimized for low power consumption while offering high RF output power and exceptional receiver sensitivity. The device is suitable for applications which have to satisfy either the European (ETSI-300-220) or the North American (FCC part 15) regulatory standards. TrueRF™ technology enables a low –cost external component count (elimination of the SAW filter) whilst still satisfying ETSI and FCC regulations.

APPLICATIONS

- Automated Meter Reading (AMR)
- Home Automation and Access Control
- High-Quality Speech, Music and Data over RF
- Applications requiring Konnex-compatibility

KEY PRODUCT FEATURES

- RF output power: up to +15 dBm
- High reception sensitivity: down to –114 dBm (typical)
- Low power consumption:
  R_X = 14 mA; T_X = 62 mA @15 dBm (typical)
- Supply voltage down to 2.4V
- Data rate from 1.2 to 152.3 kbit/s, NRZ coding
- Konnex-compatible operation mode
- 11-bit Barker encoder/decoder
- On-chip frequency synthesizer with minimum frequency resolution of 500 Hz
  Continuous phase 2-level FSK modulation
  Received data pattern recognition
- Bit-Synchronizer for incoming data/clock synchronization and recovery
- RSSI (Received Signal Strength Indicator)
- FEI (Frequency Error Indicator)
- RoHS green package

ORDERING INFORMATION

Part number	Temperature range	Package
XE1203FI063TRLF	-40 °C to +85 °C	MLPQ48

Table of Contents

The XE1203F is a single-chip UHF transceiver integrated circuit intended for use as a low cost FSK transceiver to establish a frequency-agile, half-duplex, bi-directional RF link, with NRZ (non-return to zero) data coding. Barker encoder/decoder hardware can be activated to modulate/demodulate the transmitted signal to reduce the effects of fixed-frequency in-band interference. The device is available in a MLPQ48 package and is designed to provide a fully functional multi-channel FSK transceiver. It is intended for applications in the 868 MHz European band and the North American 902-928 MHz ISM band. The single chip transceiver operates down to 2.4V and provides a low power solution for battery-operated and power sensitive applications. The XE1203F is capable of operating data rates up to 152.3 kbit/s, making it ideally suited for applications where high data rates are required.

1 FUNCTIONAL BLOCK DIAGRAM

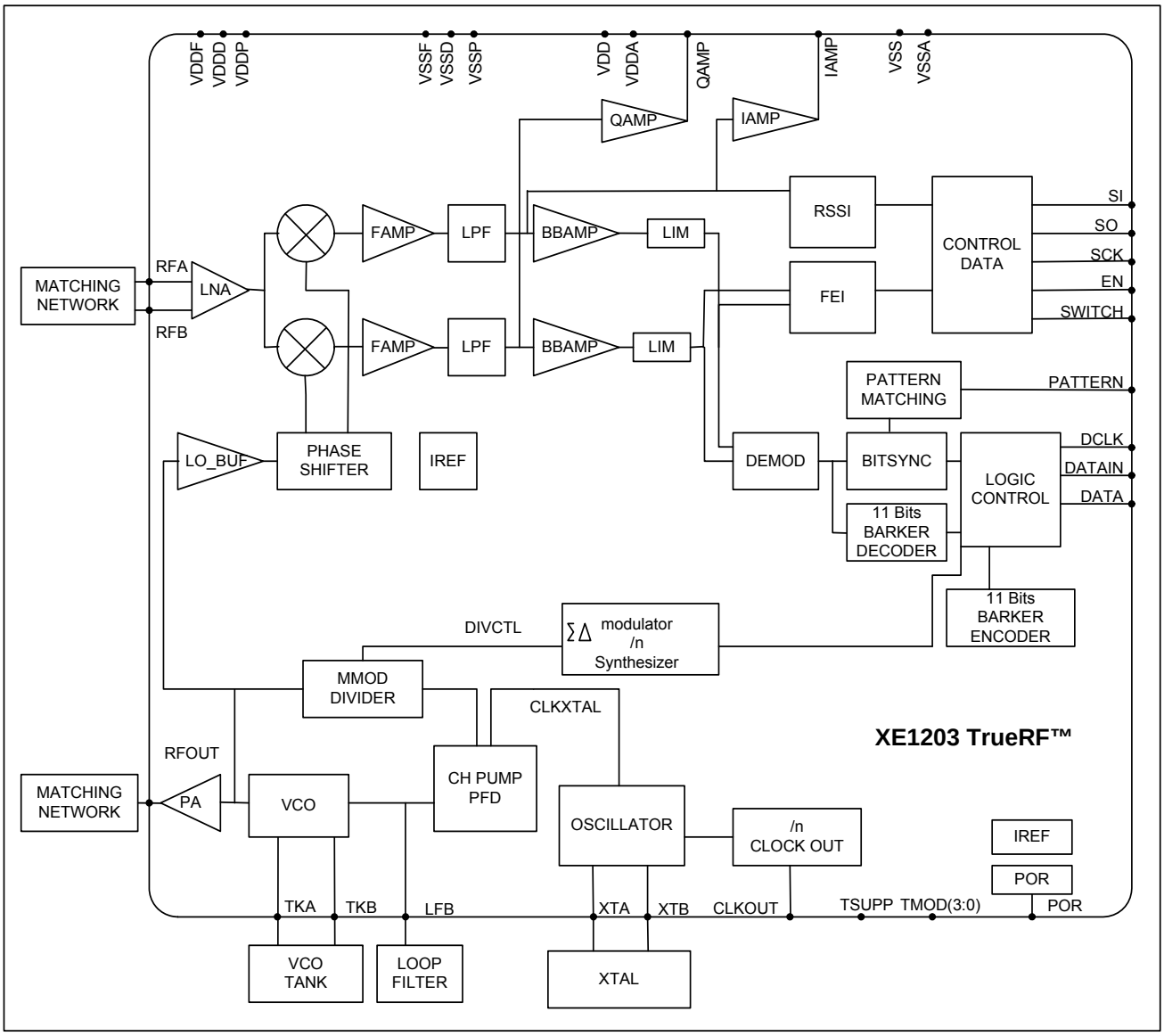


Figure 1: XE1203F Block Diagram

2 PIN DESCRIPTION

PIN	NAME	I/O	Description
1	N.C.		Not connected
2	N.C.		Not connected
3	N.C.		Not connected
4	VSSF		Ground for the RF analog blocks
5	RFA	IN	RF input
6	RFB	IN	RF input
7	VSSP		Ground for the RF power amplifier
8	VSSP		Ground for the RF power amplifier
9	RFOUT	OUT	RF output
10	VDDP		Power supply for the RF power amplifier
11	Test pin	IN	Connected to ground
12	VDDF		Power supply for the RF analog blocks
13	VSSF		Ground for the RF analog blocks
14	TKA	IN/OUT	VCO tank
15	TKB	IN/OUT	VCO tank
16	VSSF		Ground for the RF analog blocks
17	LFB	IN/OUT	Loop filter of the PLL
18	VDDD		Power supply for the RF digital blocks
19	VSSD		Ground for the RF digital blocks
20	Test pin	IN	Connected to ground
21	Test pin	IN	Connected to ground
22	N.C.		Not connected
23	Test pin	IN	Connected to ground
24	Test pin	IN	Connected to ground
25	VSSA		Ground for the analog blocks
26	XTA	IN/OUT	Crystal and input of external clock
27	VSSA		Ground for the analog blocks
28	XTB	IN/OUT	Crystal
29	VDDA		Power supply for the analog blocks
30	QAMP		Buffered Q output
31	IAMP		Buffered I output
32	Test pin	IN	Connected to ground
33	Test pin	IN	Connected to ground
34	Test pin	IN	Connected to ground
35	EN	IN	3-wire interface communication enable signal
36	VDD		Power supply for the digital blocks
37	SWITCH	IN/OUT	Receiver or Transmitter mode selection
38	SO	OUT	Data output of the 3-wires interface
39	SI	IN	Data input of the 3-wires interface
40	SCK	IN	Input clock of the 3-wires interface
41	CLKOUT	Out	Output clock at quartz frequency divided by 4, 8, 16 or 32
42	VSS		Ground for the digital blocks
43	DCLK	OUT	Transmitter or Receiver clock
44	DATA	IN/OUT	Transmitter input data or Receiver output data
45	DATAIN	IN	Transmitter input data
46	PATTERN	Out	Output of the pattern recognition block
47	N.C.		Not connected
48	N.C.		Not connected

3 ELECTRICAL CHARACTERISTICS

3.1 ABSOLUTE MAXIMUM OPERATING RANGES

Stresses above the values listed below in Table 1 may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Description	Min.	Max.	Unit
VDDmax	Supply voltage	-0.4	3.9	V
ML	Receiver input level		-5	dBm
Tmax	Storage temperature	-55	125	°C

Table 1: Absolute Maximum Ratings

The device is ESD sensitive and should be handled with precaution.

3.2 SPECIFICATIONS

3.2.1 Operating Range

Symbol	Description	Min.	Max.	Unit
VDD	Supply voltage	2.4	3.6	V
T	Temperature	-40	85	°C
CLop	Load capacitance on digital ports	-	25	pF

Table 2: Operating Range

3.2.2 Electrical Specifications

Table 3 below gives the electrical specifications of the transceiver under the following conditions: Supply Voltage VDD = 3.3V, temperature = 25 °C, 2-level FSK without pre-filtering, carrier frequency fc = 915 MHz, frequency deviation Δf = 55 kHz, bit rate BR = 4.8 kbit/s, Base band filter bandwidth BBW = 200 kHz, bit error rate BER = 0.1% (measured at the output of the bit synchronizer), LNA input and RF PA output matched to 50Ω, environment as defined in Section 6, unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.2	1	uA
IDDST	Supply current in standby mode	Quartz oscillator (39 MHz) enabled	-	0.85	1.10	mA
IDDR	Supply current in receiver mode		-	14	17	mA
IDDT	Supply current in transmitter mode (with optimum load-matching)	RFOP = 5 dBm	-	33	40	mA
		RFOP = 15 dBm	-	62	75	mA
RFS	RF sensitivity	BR = 4.8 kbit/s Mode A (*1)	-	-114	-111	dBm
		BR = 4.8 kbit/s Mode B (*1)	-	-101	-98	dBm
		BR = 32.7 kbit/s Mode A (*1)	-	-109	-106	dBm
		BR = 32.7 kbit/s Mode B (*1)	-	-96	-93	dBm
		Δf = 200 kHz, BBW = 600 kHz				
		BR = 152.3 kbit/s Mode A (*1)	-	-101	-98	dBm
		BR = 152.3 kbit/s Mode B (*1)	-	-89	-86	dBm
RFSB	RF sensitivity with Barker Coding/decoding enabled	BR = 1154 bit/s Mode A (*1)	-	-113	-110	dBm
		BR = 1154 bit/s Mode B(*1)	-	-100	-97	dBm
FDA	Frequency deviation	Programmable	1	-	255	kHz
CCR	Co-channel rejection		-13	-10	-	dBc

Symbol	Description	Conditions	Min	Typ	Max	Unit
IIP3	Input intercept point	$f_1 = f_{LO} + 1$ MHz $f_2 = f_{LO} + 1.945$ MHz				
		Mode A (*1)	-36	-33	-	dBm
		Mode B (*1)	-21	-18	-	dBm
BBW	Base band filter bandwidth DSB	Programmable (*2)	-	200	-	kHz
			-	600	-	kHz
ACR	Adjacent channel rejection	funw = f_{LO} + 650 kHz Pw= - 108dBm, mode A (*1)	45	48	-	dBc
BR	Bit rate	Programmable	1.2		152.3	kbit/s
RFOP	RF output power	Programmable RFOP1	-3	0	-	dBm
		RFOP2	+2	+5	-	dBm
		RFOP3	+7	+10	-	dBm
		RFOP4	+12	+15	-	dBm
FR	Synthesizer frequency range	Programmable	433	-	435	MHz
		Each range with its own	868	-	870	MHz
		external components	902	-	928	MHz
TS_TR	Transmitter wake-up time	From oscillator enabled	-	150	250	us
TS_RE	Receiver Baseband wake-up time	From oscillator enabled	-	0.5	0.8	ms
TS_RSSI	RSSI wake-up time	From receiver enabled	-	-	1	ms
TS_RSSIM	RSSI measurement time			0.5		ms
TS_OS	Crystal oscillator wake-up time	Fundamental	-	0.3	0.5	ms
		3rd overtone	-	2.5		ms
TS_FEI	FEI wake-up time		-	-	2/BR	ms
TS_SYNC_AQ	Time for synchronization of the Barker decoder	Input power of –106 dBm Data rate = 1154 bits/s Chip rate = 12.7 kcps From Rx enabled	-	5	-	ms
XTAL	Crystal oscillator frequency	Fundamental or 3rd overtone	-	39	-	MHz
FSTEP	Frequency synthesizer step	Exact step is XTAL / 77 824	-	500	-	Hz
VTHR	RSSI equivalent input thresholds	Mode A (*1)				
		Low range:VTHR1	-	-100	-	dBm
		VTHR2	-	-95	-	dBm
		VTHR3	-	-90	-	dBm
		High range:VTHR1	-	-85	-	dBm
		VTHR2	-	-80	-	dBm
		VTHR3	-	-75	-	dBm
SPR	Spurious emissions in Rx mode	(*4)	-	-65	-	dBm
SCK	Serial Clock frequency				1	MHz
VIH	Digital input level high (*3)	% VDD	75	-	-	%
VIL	Digital input level low (*3)	% VDD	-	-	25	%
VOH	Digital output level high	% VDD	75	-	-	%
VOL	Digital output level low	% VDD	-	-	25	%

Table 3: Electrical Specifications

Notes:
(*1) Mode A: High sensitivity mode; Mode B: High Linearity mode. As defined in Paragraph 4.1.1.
(*2) An intermediate bandwidth of 300 kHz can also be selected by using additional settings described in section 5.2.8.
(*3) Throughout this document, digital signal levels are named “high” or “1”, and “low” or “0”.
(*4) SPR strongly depends on the design of the application board and the choice of the external components. Values down to -70 dBm can be achieved with careful design.

4 GENERAL DESCRIPTION

The XE1203F is a direct conversion (Zero-IF) half-duplex data transceiver. The circuit operates in three different ISM frequency bands (433 MHz, 868 MHz and 915 MHz) and uses 2-level FSK modulation/demodulation to provide a complete transmission link. It is capable of operating at data rates between 1.2 and 152.3 kbit/s, making it ideally suited for applications where high data rates are required. It also supports the Konnex standard where the bit rate is 32.7 kbit/s. The device includes dedicated Barker encoder/decoder hardware that may be activated to modulate/demodulate the transmitted signal to reduce in-band interferences.

The XE1203F is a highly programmable device – channel, bit rate, frequency deviation, output power, base band filter bandwidth, sensitivity vs. linearity, RSSI feature, and many other parameters – which makes it extremely flexible, to meet a large number of end user requirements.

The main functional blocks of the XE1203F are the receiver, the transmitter, the frequency synthesizer and some service blocks. The device also includes a series of configuration and status registers. In a typical application, the XE1203F is programmed by a microcontroller via the 3-wire serial bus SI, SO, SCK to write to and read from these registers.

The Receiver converts the incoming 2-level FSK modulated signal into a synchronized bit stream.

The Transmitter performs the modulation of the carrier by an input bit stream and the transmission of the modulated signal.

The Frequency Synthesizer generates the local oscillator (LO) signal for the receiver section as well as the continuous phase FSK modulated signal for the transmitter section.

The Service Blocks provide the internal voltage and current sources and provide all the necessary functions for the circuit to work properly.

The Configuration Registers are a set of variable-length registers that are used to store various settings to operate the XE1203F transceiver circuit. They are listed below in Table 4. Refer to Section 5.2 for the detailed descriptions of these registers. These registers are accessed in write or read mode through the 3-wire serial bus, as described in Section 5.1.

Name	Description
ConfigSwitch	1-bit data to switch between 2 sets of user-predefined SWParam Configuration Registers
RTParam	Receiver and transmitter parameters
FSParam	LO, Bitrate, Deviation and other frequency parameters
SWParam	2 sets of user-predefined configuration registers
DataOut	Status register which can be read through the 3-wire serial interface
ADParam	Additional parameters
Pattern	Reference pattern for the “pattern recognition” feature

Table 4: Configuration Registers

Naming convention: throughout this document, each individual bit in a particular Configuration Register includes the name of this register followed by a bit identifier. For example, RTParam_Band are the “Band” bits within the RTParam register.

The Digital Interface provides internal control signals for the whole circuit according to the configuration register settings.

4.1 THE RECEIVER SECTION

The receiver converts the incoming 2-level FSK modulated signal into a synchronized bit stream. The receiver is composed of a low-noise amplifier, two down-conversion mixers, two base band filters, two base band amplifiers, two limiters, a demodulator and a bit synchronizer. The bit synchronizer translates the output of the demodulator into a glitch-free bit stream available on the pin DATA. It also generates a synchronized clock, DCLK, which can be

used to sample the DATA signal without additional external signal processing. In addition, the receiver includes a digital Received Signal Strength Indicator (RSSI), a Frequency Error Indicator (FEI) that provides information about the local oscillator frequency error, and a pattern recognition function to detect preprogrammed sequences in the received serial data stream. Finally, a user-selectable Barker coding/decoding feature can be activated to spread the outgoing data with an 11-bit Barker code upon transmission and decode the incoming data upon reception by correlating the spread data with the 11-bit Barker code.

4.1.1 LNA & Receiver modes

The LNA of the receiver has two programmable operation modes: the high sensitivity mode, Mode A, for reception of weak signals; and the high linearity mode, Modxe B, for strong signals. The operation mode is defined by the contents of the SWParam_Rmode1 and SWParam_Rmode2 Configuration Register bits.

- **Mode A**: High sensitivity mode, approximately 13dB better than in Mode B (see 3.2.2, RFS parameter)
- **Mode B**: High Linearity mode, IIP3 approximately 15dB higher than in Mode A (see 3.2.2, IIP3 parameter)

4.1.2 Demodulation chain

The demodulation chain consists of an FSK demodulator, bit synchronizer, Barker decoder and a Pattern Recognition block. Figure 2 below illustrates the interaction between each section of the demodulation chain.

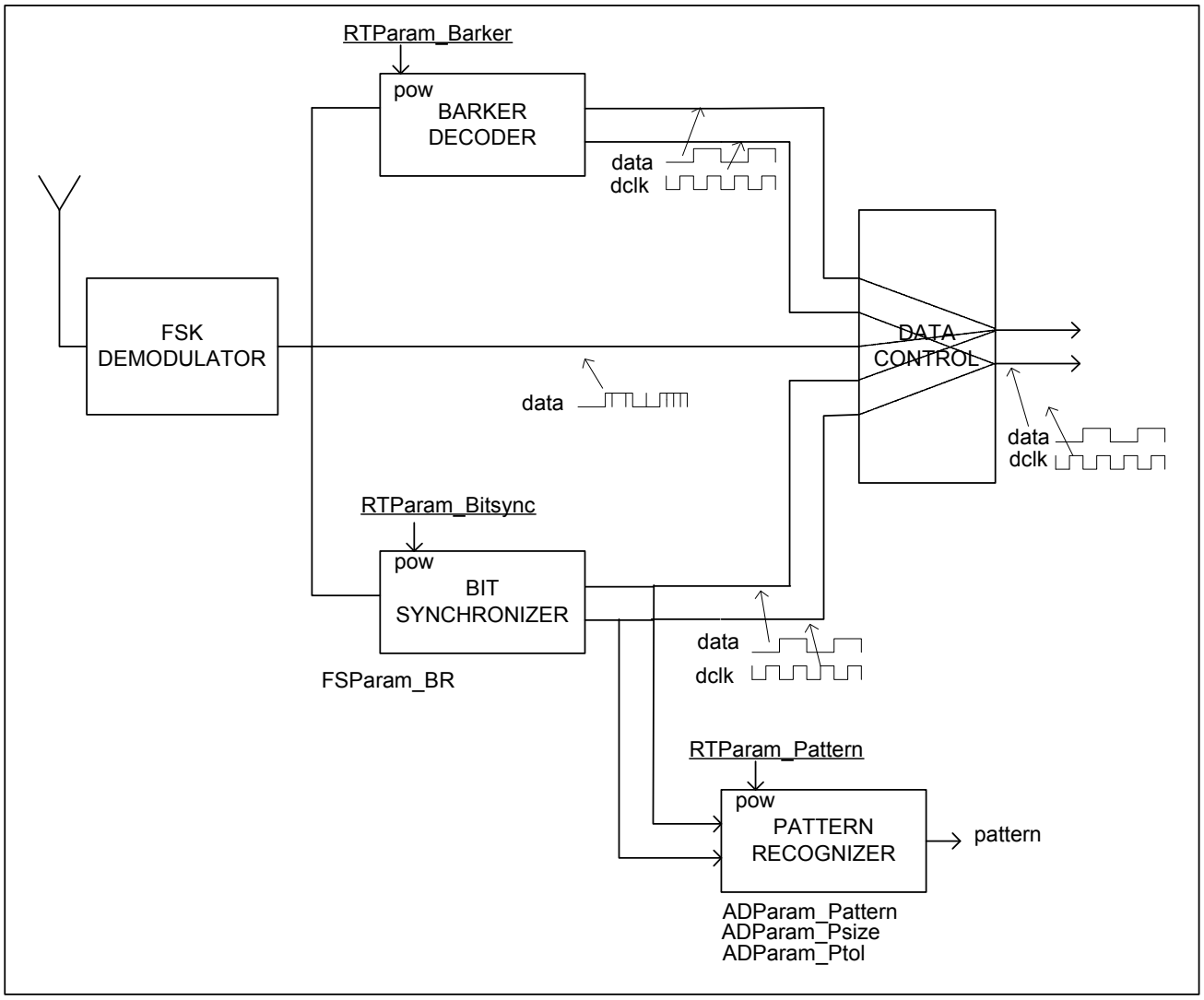


Figure 2: Demodulation architecture

4.1.3 Demodulator

The demodulator provides a demodulated data stream from the received FSK modulated base band limited signals, I_lim and Q_lim. If the end-user application requires direct access to the output of the demodulator, then the RTParam_Bitsync and RTParam_Barker Configuration Register bits are set low (disabled). In this case the

demodulator output is directly connected to the DATA pin and the DCLK pin is set to low. Otherwise, the demodulator output is processed by the bit synchronizer.

For correct operation of the demodulator the modulation index β of the input signal should meet the following condition:

$$\beta = \frac{2 \cdot \Delta f}{BR} \geq 2,$$

where Δf is the frequency deviation and BR the bit rate.

4.1.4 Bit synchronizer

The raw output signal from the demodulator usually contains jitter and glitches. The bit synchronizer transforms the data output of the demodulator into a glitch-free bit stream available on the DATA pin and generates a synchronized clock DCLK to be used for sampling the DATA output (see Figure 3, below).

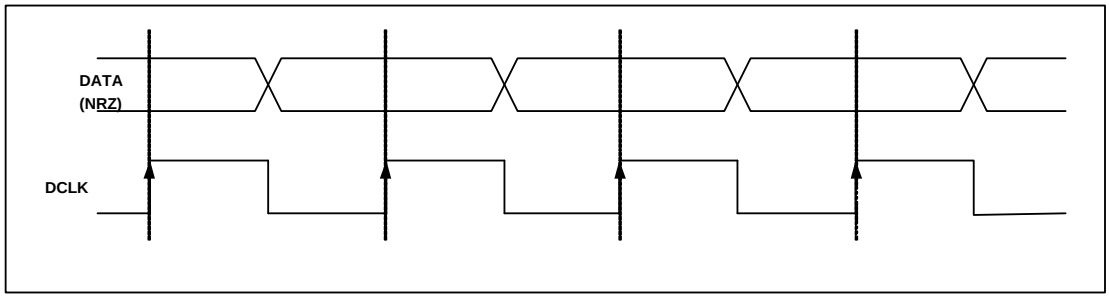


Figure 3: Bit synchronizer timing diagram.

For proper operation, in addition to the requirement for the modulation index defined in 4.1.3 above, the Bit Synchronizer must first receive three bytes of alternating logic value preamble, i.e. “0101” sequences. After this startup phase, the rising edge of DCLK signal is centered on the demodulated bit. Subsequent data transitions will preserve this centering.

This has two implications:

- If the Bit Rates of Transmitter and Receiver are known to be the same, the XE1203F will be able to receive an infinite unbalanced sequence (all “0s” or all ”1s”) with no restriction.
- If there is a difference in Bit Rate between Tx and Rx, the amount of adjacent bits at the same level that the BitSync can withstand can be estimated as:

$$\text{Number of Bits} = 0.5 \cdot \frac{BR}{\Delta BR}$$

This implies approximately 6 consecutive unbalanced bytes when the Bit Rate precision is 1%, which is easily achievable (crystal tolerance is in the range of 50 to 100 ppm). It is recommended that the bit rate accuracy be better than ±5% (3% for Konnex mode operation).

The bit synchronizer is enabled when RTParam_Bsync Configuration Register bit is high. If this bit set low, the bit synchronizer is disabled. In this case the output of the demodulator is directed to the DATA pin and the DCLK output is set to “0”.

The received bit rate is defined by the value of the FSParam_BR Configuration Register, and is calculated as follows:

$$\text{Bit rate} = \frac{152.34e3}{\text{int}(\text{FSParam\_BR}(6:0)) + 1}$$

where int(x) is the integer value of the unsigned binary representation of (x).

Note: for Konnex standard operations, the bit rate is fixed at 32.7 kbit/s. ADParam_enable_konnex should be set to a ‘1’.

4.1.5 The DATA and DATAIN pins

The pin DATA is by default used by both the transmitter and the receiver sections. By default it is set as a bidirectional I/O pin. When in receive mode, demodulated data appears at DATA as an output signal. In transmit mode, the transmitted bit stream is applied to this pin as an input.

Some applications may require separate input and output pins for the transmitted and received data. In this case the user has to set the ADParam_disable_data_bidir Configuration Register bit to '1'. As a result the DATA pin is set as an output only for the received data, while the transmit data is controlled via the DATAIN input pin.

4.1.6 Pattern recognition block

When in receiver mode, this feature is activated by setting RTParam_Pattern Configuration Register bit high. The demodulated data signal is compared with a pattern stored in the PATParam_Pattern Configuration Register. The PATTERN output pin is driven by the output of this comparator and is synchronized by DCLK. It is set to high when a matching condition is detected, otherwise set to low. The PATTERN output is updated at the rising edge of DCLK. The number of bits used for comparison is defined in the ADParam_Psize Configuration Register and the number of tolerated errors for the pattern recognition is defined in the ADParam_Ptol register. Figure 4, below, illustrates the pattern matching process.

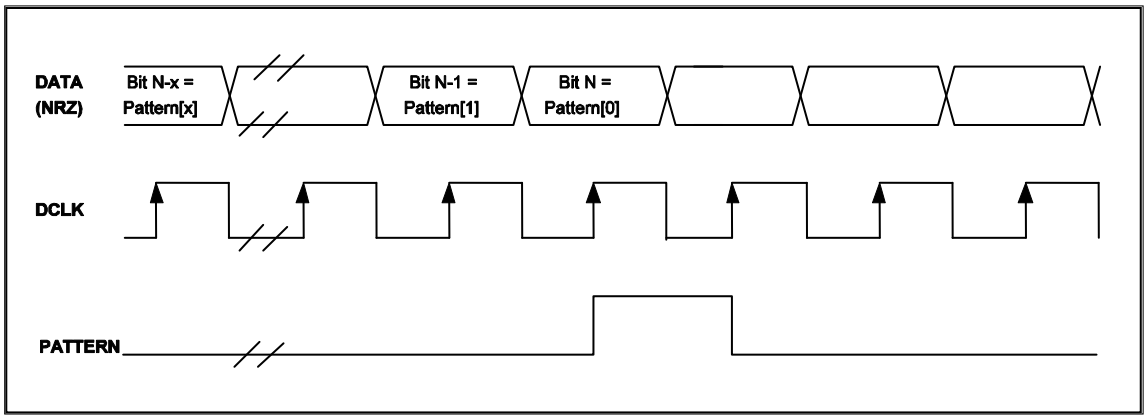


Figure 4: Pattern Matching Operation.

4.1.7 RSSI

When enabled, this function provides a Received Signal Strength Indication based on the signal at the output of the base-band filter. To enable the RSSI function, the RTParam_RSSI Configuration Register bit should be set to "1". When enabled, the status of the RSSI in the DataOut_RSSI register is a 2-bit word which can be read via the serial control interface. The content of the register is defined in Table 5, below, where V_{RFFIL} is the differential amplitude equivalent to the RF input signal with the receiver operated in A-mode. The thresholds, V_{TH} are the equivalent of the signal at the output of the base-band filter stage, divided by the signal gain.

DataOut_RSSI	Description
0 0	$V_{RFFIL} \leq$ VTHR1
0 1	VTHR1 < $V_{RFFIL} \leq$ VTHR2
1 0	VTHR2 < $V_{RFFIL} \leq$ VTHR3
1 1	VTHR3 < V_{RFFIL}

Table 5 RSSI status description

Two possible ranges, each having a set of three V_{TH} threshold values, VTHR1, VTHR2, and VTHR3 (see 3.2.2 for actual values), are selected with the RTParam_RSSIR Configuration Register bit. They provide an overall RSSI range of typically 25 dB.

The timing diagram of an RSSI measurement is illustrated in the Figure 5 below. When the RSSI function has been activated, the signal strength is periodically measured and the result is stored in the register DataOut_RSSI each time this DataOut_RSSI register is read via the 3-wire serial interface. Note that TS_RS is the wake-up time required after the function has been enabled to ensure that a valid reading of RSSI is obtained.

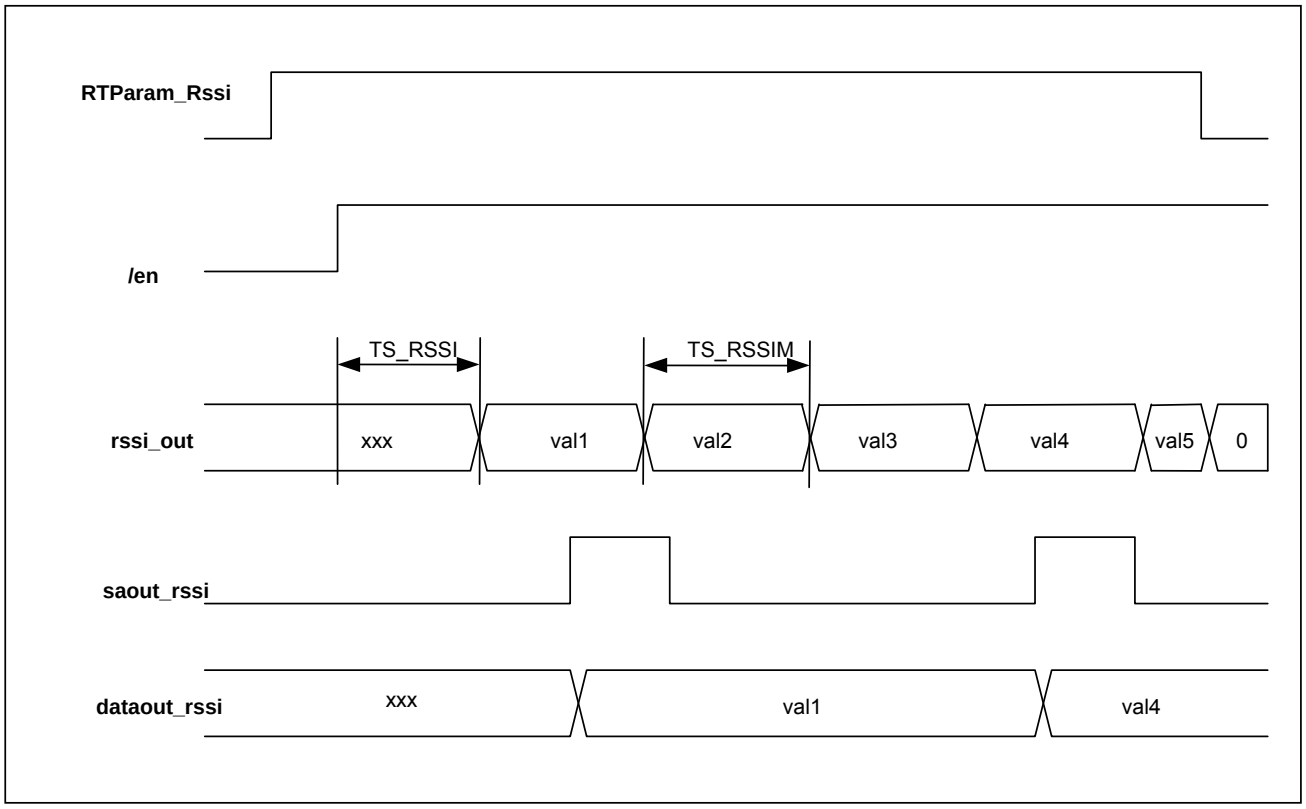


Figure 5: RSSI measurement timing diagram

Note on the Dataout_RSSI update: during a read sequence of the Dataout_RSSI Status Register, the Saout_rssi signal is generated internally as illustrated in the Figure 6 below. It can be seen the value of the Dataout_RSSI Status Register is updated upon transmission of the bit A0 on the SI line. The maximum frequency of SCK during the read operation of the RSSI value is 100 kHz.

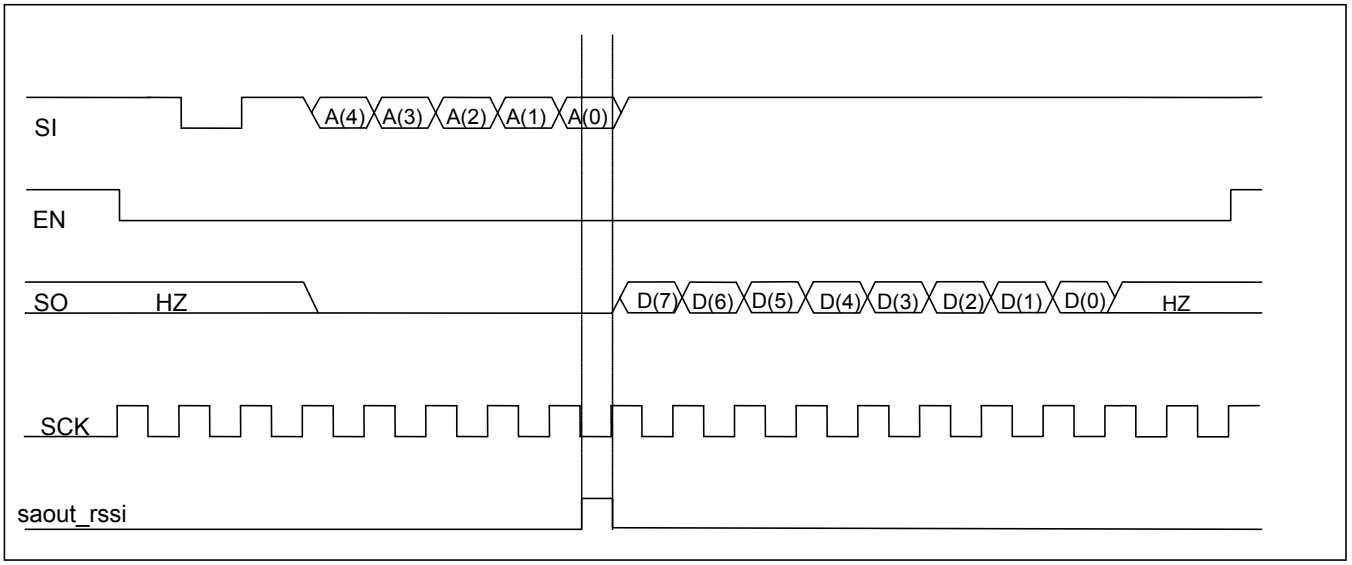


Figure 6: Generation of saout_rssi

4.1.8 Frequency Error Indicator – FEI

When enabled this function provides an indication of the frequency error of the local oscillator compared with the received carrier frequency. For guaranteed operation of the FEI function the following two conditions should be met:

1) The modulation index, β, should meet the following condition:

$$\beta = \frac{2 \cdot \Delta f}{BR} \geq 2,$$

where: Δf = frequency deviation of the modulated input signal, BR = input data bit-rate.

2) The bandwidth of the baseband filter (BBW) must be greater than the sum of the frequency offset and the received peak signal bandwidth, as defined below:

$BBW > f_{OFFSET} + BW_{SIGNAL}$

where BBW is the baseband filter bandwidth defined by the RTParam_BW register. f_{OFFSET} is the difference between the carrier frequency and the LO frequency, and BW_{SIGNAL} is equal to $\left(\frac{BR}{2} + \Delta f\right)$.

Note on the timing for FEI measurement: The timing diagram of the FEI measurement process is illustrated in Figure 7 below. As long as the FEI function remains enabled, the frequency error is continuously measured every 2/BR seconds, starting TS_FEI (see Paragraph 3.2.2) after the FEI function is enabled. The measurement results are loaded into the status registers Dataout_MSB_fei and Dataout_LSB_fei each time the Dataout_LSB_fei register is read through the 3-wire serial interface. In the diagram below, Saout_fei is generated internally during a read sequence from the "Dataout_LSB_fei '' status register.

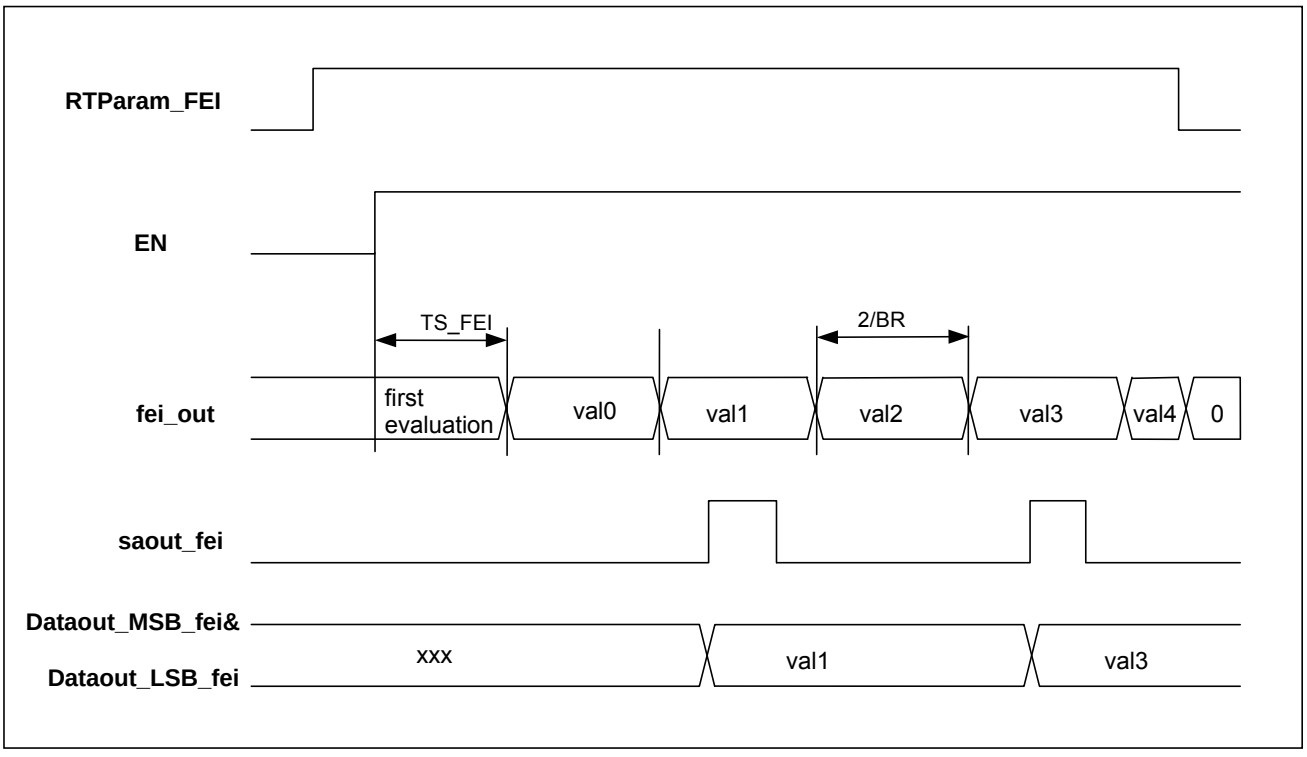


Figure 7: Timing diagram of the FEI measurement process

The maximum frequency of SCK during the FEI read operation is 100 kHz. When using the Konnex standard, the bit ADParam_enable_konnex Configuration Register must be set to '1'.

The frequency error can then be calculated by using the following formula:

$$\text{Frequency error} = (BR/8)*\text{int}(\text{Dataout\_FEI}(11:0)),$$

where Dataout_FEI(11:0) = Dataout_MSB_fei(3:0) + Dataout_LSB_fei(7:0), and int(x) is the integer value of the **signed binary** representation of x.

4.2 THE TRANSMITTER SECTION

The Transmitter performs the modulation of the carrier by an input bit stream and the transmission of the modulated signal. Carrier modulation is achieved directly through the frequency synthesizer via a Sigma-Delta modulator. The frequency deviation and the bit-rate of the modulated carrier are programmable. An on-chip power amplifier then amplifies the RF signal. The output power can be programmed with 4 possible settings:

RTParam_Tpow	Output power
0 0	RFOP1
0 1	RFOP2
1 0	RFOP3
1 1	RFOP4

Table 6: Output power settings

4.2.1 Transmitter

The transmit data should be applied to DATA or DATAIN pins depending on the setting of the ADParam_disable_data_bidir configuration bit. If the parameter is set to “1”, then the DATAIN pin is used, otherwise the bidirectional pin DATA is used.

The modulating signal on DATA or DATAIN can be pre-processed before modulating the local oscillator to produce the outgoing FSK RF signal. This is the pre-filtering feature. The pre-filtering is selected by setting the RTParam_Filter configuration bit to “1”. When RTParam_Filter is set to “1”, the input baseband data is pre-filtered before being applied to the frequency synthesizer. This means that the rising and falling edge of each bit is linearly smoothed with a staircase transition. When RTParam_Filter is set to “0”, the input baseband data is applied directly to the frequency synthesizer without any pre-filtering function.

The two possible modulation methods are shown in Figure 8, where “datain” is the input bit stream from DATA or DATAIN pins.

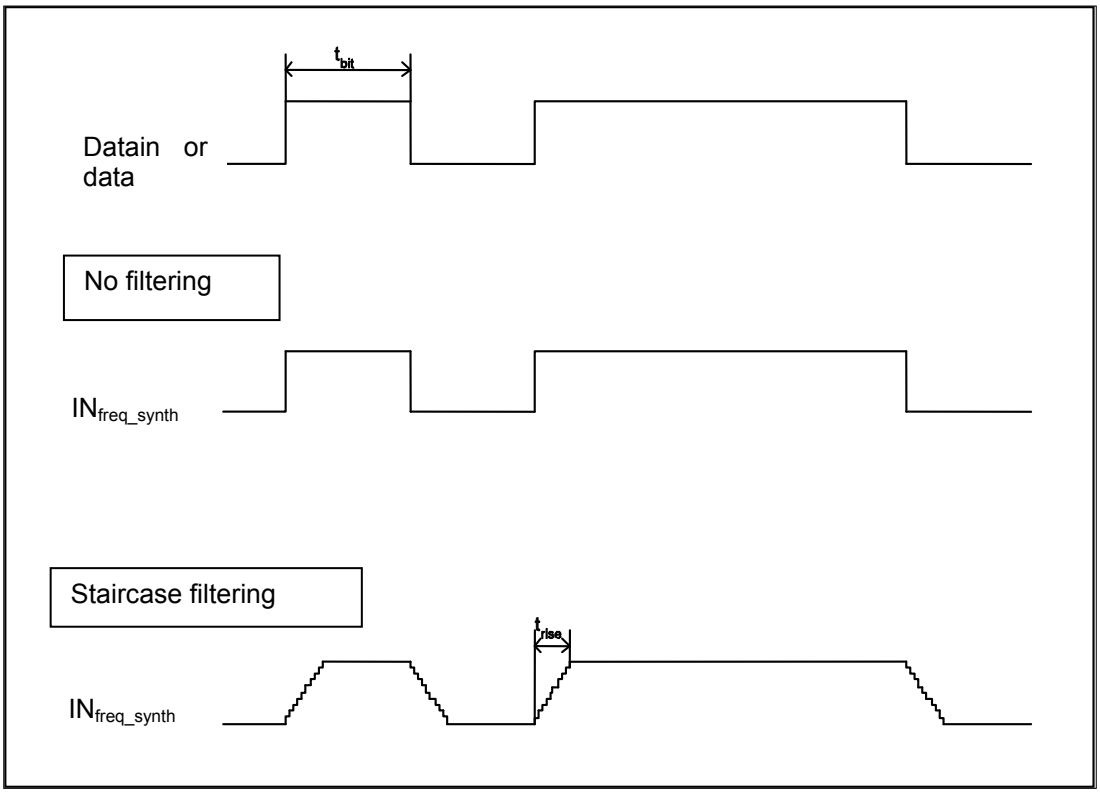


Figure 8: Modulation with and without pre-filtering

The main characteristic of this pre-filtering function is the ratio between the rise/fall time to the bit duration, t_{rise}/t_{bit}. The value of this ratio can be programmed between two pre-defined values in the RTParam_Stair configuration bit, as shown in the Table 7.

RTParam_Stair	t_{rise}/t_{bit}
0	10%
1	20%

Table 7: t_{rise}/t_{bit} ratio

When the pre-filtering function is enabled (RTParam_Filter set to “1”), only the following bit rates and frequency deviations can be used:

FSParam_Dev	Frequency deviation
00101000	40 kHz
00110111	55 kHz
01010000	80 kHz
10100000	160 kHz
11001000	200 kHz

FSParam_Br	Bit rate (bit/s)
1111110	1200
0111111	2400
0011111	4800
0001111	9600
0000111	19200
0000011	38400
0000001	76800
others (*)	153000

Table 8: Possible bit rates and frequency deviations when pre-filtering is enabled

(*) For any programmed value of FSParam_Br which is not in the Table 8 above, the data-rate is fixed to 153 kbit/s and the pre-filtering is applied as defined by the user.
If ADParam_enable_konex is set high, then the pre-filtering option is available for a bit rate of 32.7 kbit/s and one of the frequency deviations defined above.

4.2.2 Barker encoder/decoder

The Barker encoder/decoder hardware can be activated to modulate/demodulate the transmitted signal to reduce in-band interferences The Barker decoder provides an alternative to the bit synchronizer only for a **fixed data rate of 1154bits/s**. The Barker block is selected when the RTParam_Barker configuration bit is set to "1". In transmission, the information data at a bit rate of 1154bits/s is spread using an 11-bit Barker code. The result is an encoded bit stream at 12.7 kilochips per second (kcps), which is applied to the frequency synthesizer. On the receiver part, the signal is demodulated using the FSK demodulator (at 12.7 kcps) and then fed into the Barker decoder to recover the un-encoded data at 1154 bit/s, together with a synchronized clock to sample it. Figure 8 on the next page, illustrates the coding/decoding process.

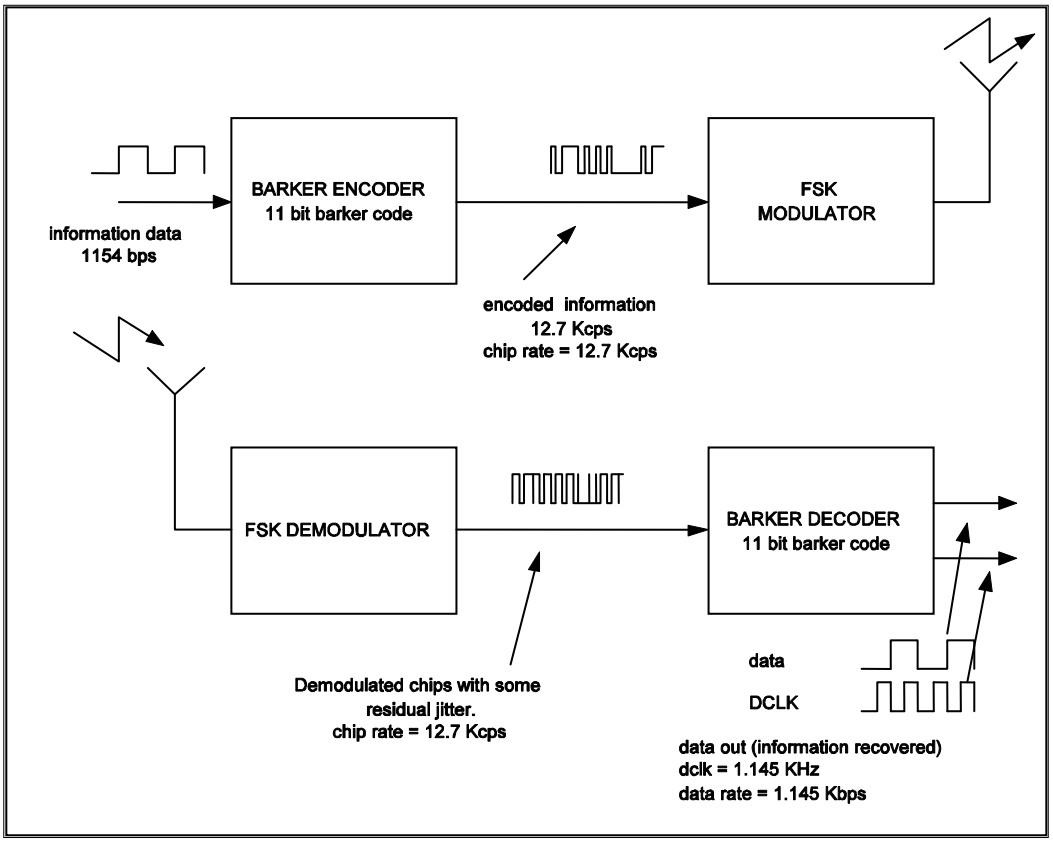


Figure 9: Barker Encoding and Decoding Channels.

In receiver mode, the XE1203F provides a clock output, DCLK, to a microcontroller. The data can be sampled at the rising edge of the clock. When using the Barker decoding process, DCLK is used to detect the sync acquisition. If there is no valid data, DCLK remains high. The first falling edge of the clock means that the sync acquisition phase has been reached and that the output data is now available. This is illustrated below in Figure 10.

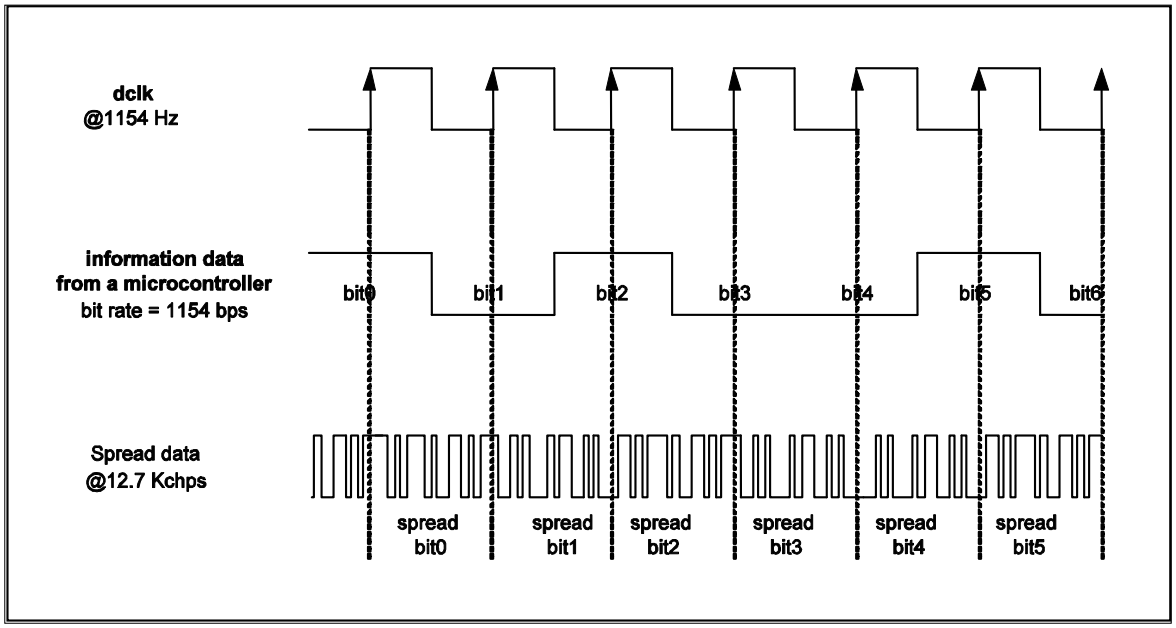


Figure 10: Data exchange during reception mode with Barker the feature enabled

When using the Barker encoding in transmitter mode, the RTParam_Barker parameter is set to "1" and the baseband data at 1154 bit/s is applied through either the DATA or DATAIN depending to the status of ADParam_disable_data_bidir. The data is spread into an encoded chip stream at 12.7 kcps by the Barker encoder. This chip stream is directly applied to the frequency synthesizer without any pre-filtering.

When using the Barker coder/decoder feature in transmission mode, the DCLK pin is used to synchronize the data coming from a microcontroller or another source. This DCLK clock is generated by the XE1203F. At the falling edge of the each clock a new data bit (on DATA or DATAIN) should be supplied by the microcontroller or another source. This data is sampled by the XE1203F at the next rising edge of DCLK. It is then spread by using an 11-bit length Barker code. The Figure 11 shows the data exchange during the transmission mode when the Barker feature is enabled.

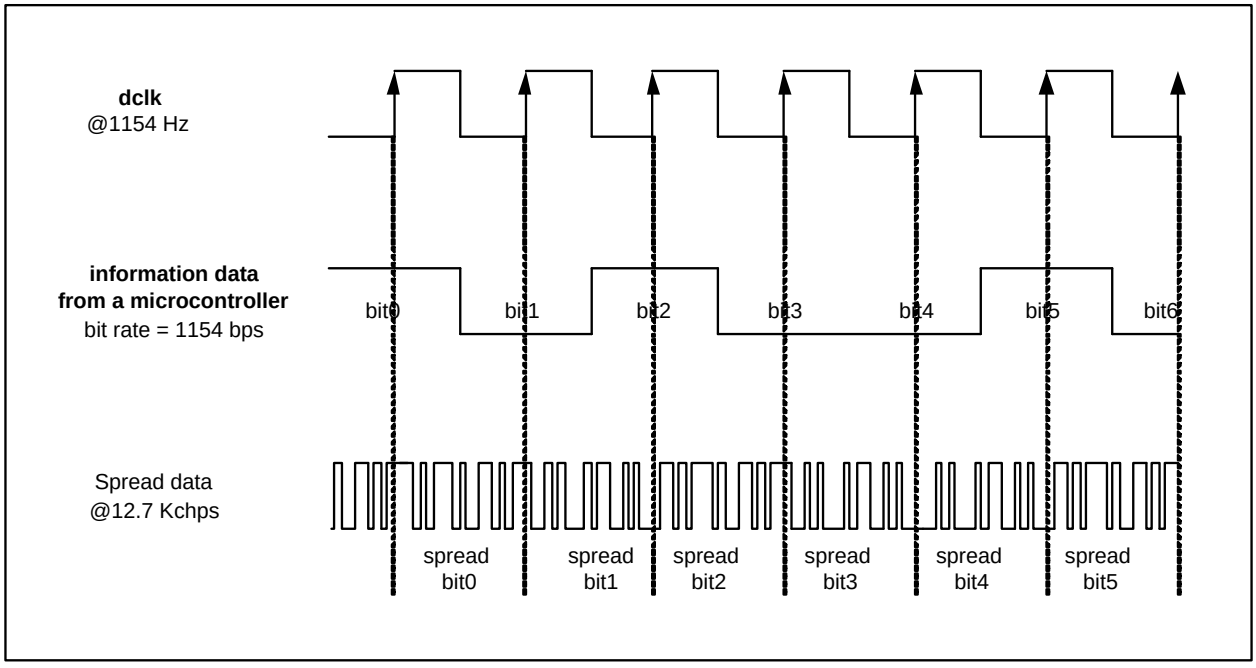


Figure 11: Data exchange during transmission mode with the Barker feature enabled

4.3 THE FREQUENCY SYNTHESIZER

The Frequency Synthesizer generates the local oscillator (LO) signal for the receiver section as well as the continuous phase FSK (CPFSK) modulated signal for the transmitter section. The core of the synthesizer is implemented with a Sigma-Delta PLL architecture. The frequency is programmable with a minimum step-size of 500 Hz in the 433, 868 and 915 MHz frequency bands. This block includes a crystal oscillator which provides the frequency reference for the PLL. This reference frequency can also be used as a reference clock for the external microcontroller on the CLKOUT pin.

4.3.1 Clock Output for external processor

A reference clock can be generated by XE1203F for use by an external microcontroller. The RTParam_Clkout configuration bit determines the status of the CLKOUT pin. When set high CLKOUT is enabled, otherwise it's disabled. The output frequency at CLKOUT is defined by the value of the ADParam_Clkfreq parameter. The output frequency at CLKOUT is the reference oscillator frequency divided by 4, 8, 16 or 32. With the reference oscillator frequency at 39 MHz this provides a reference clock at 9.75 MHz, 4.87 MHz, 2.44 MHz or 1.22 MHz, respectively. This clock signal is disabled in Sleep Mode.

5 SERIAL INTERFACE DEFINITION AND PRINCIPLES OF OPERATION

5.1 SERIAL CONTROL INTERFACE

A 3-wire bi-directional bus (SCK, SI, SO) is used to communicate with the XE1203F. SCK and SI are input signals supplied externally, for example by the microcontroller. The XE1203F configures the SO signal as an output pin during read operation, and it is tri-stated in other modes. The falling edge of the SCK signal is used to sample the SI pin to write data into the internal shift register of the XE1203F. The rising edge of the SCK signal is used to output data to SO pin by XE1203F, so the microcontroller should sample data at the falling edge of SCK.

The signal EN must be low during the whole write and read sequences. In write mode the content of the particular configuration register (see 5.2) is updated on the next rising edge of the EN signal. Before this rising edge, the new data is stored in temporary registers which do not affect the transceiver settings.

The timing diagram of a write sequence is illustrated in Figure 12 below. The sequence is initiated when a Start condition is detected, defined by the SI signal being set to “0” during one period of SCK. The next bit is a read/write (R/W) bit which should be “0” to indicate a write operation. The next 5 bits contain the address of the configuration/status registers A[4:0] to be accessed, MSB first (see 5.2). Then, the next 8 bits contain the data to be written into the register. The sequence ends with 2 stop bits set to “1”. The data on SI should change on the rising edges of SCK, and is sampled on the falling edge of SCK. After the 2 stop bits, the data transfer is terminated. The SI line should be at “1” for at least one extra SCK clock cycle before a new write or read sequence can start. This mode of operation allows data to be written into multiple registers keeping the EN line low.

The maximum frequency of SCK is 1 MHz, except as defined above when reading the RSSI or FEI outputs, where the maximum frequency of SCK is limited to 100 kHz. The minimum clock pulse width is 0.5 us. Over the operating supply and temperature range, set-up and hold time for SI on the falling edge of SCK are 200 ns.

The register at address 0 is one bit long. When writing this register, the sequence described above is valid except that only one data bit is required instead of 8. However, if a single write procedure is used for all registers 8 data bits must be sent when writing at address 0, but only the MSB will be stored at address 0. The remaining 7 data bits must all be “1”.

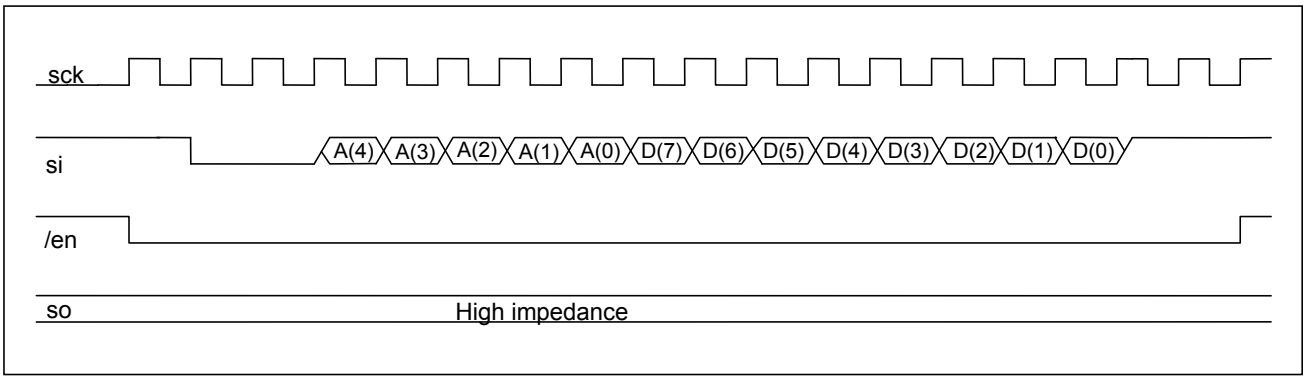


Figure 12: Write sequence into configuration register

Figure 13 illustrates a write sequence at address zero.

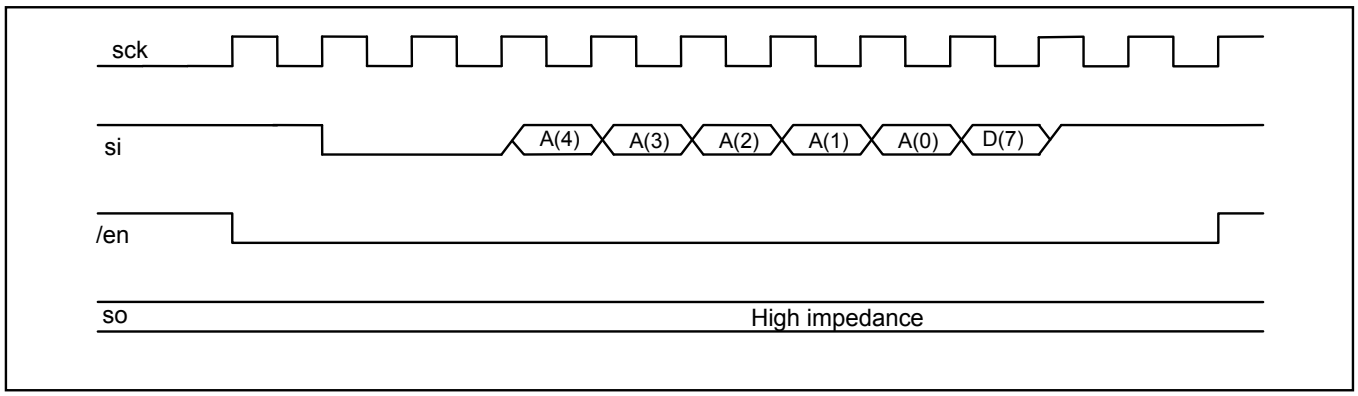


Figure 13: Write sequence into configuration register at address zero

The time diagram of a read sequence is illustrated in Figure 14 below. The sequence is initiated when a Start condition is detected, defined by the SI signal being set to “0” during a period of SCK. The next bit is a read/write (R/W) bit which should be “1” to indicate a read operation. The next 5 bits are the address of the control register A[4:0] to be accessed, MSB first. The data from the register is then output on the SO pin. The data become valid at the rising edges of SCK and should be sampled at the falling edge of SCK. After this, the data transfer is terminated. The SI line must stay high for at least one extra SCK clock cycle to start a new write or read sequence. The maximum current drive on SO is 2 mA at a supply voltage of 2.7V and the maximum load is CLop, as defined in Paragraph 3.2.2.

When the serial interface is not used for read or write operations, both SCK and SI should be set to “1”. Except when in read mode, SO is set to a high impedance mode.

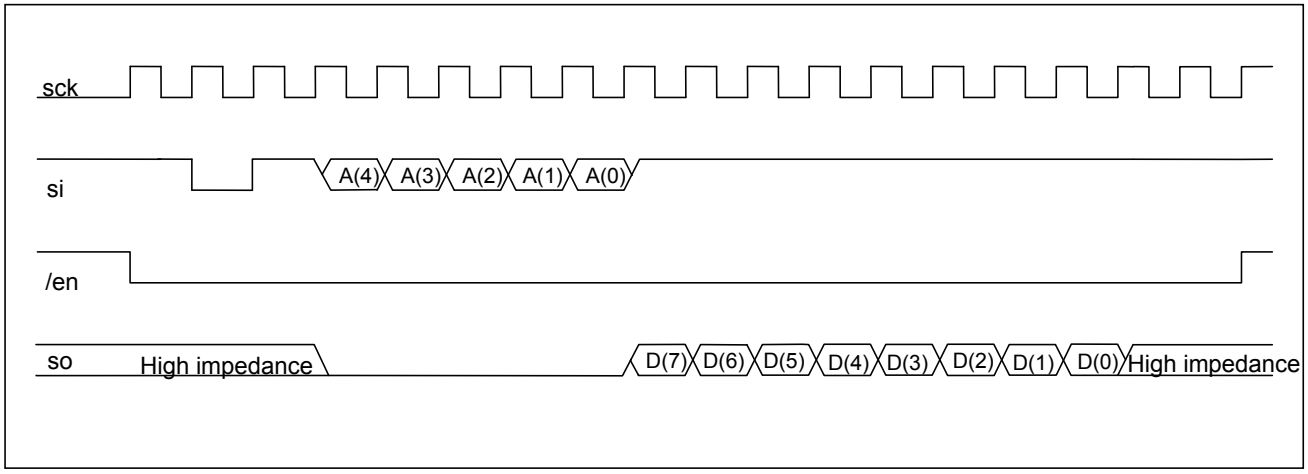


Figure 14: Read sequence of configuration register

When reading the register at address zero, the timing diagram is illustrated in Figure 15.

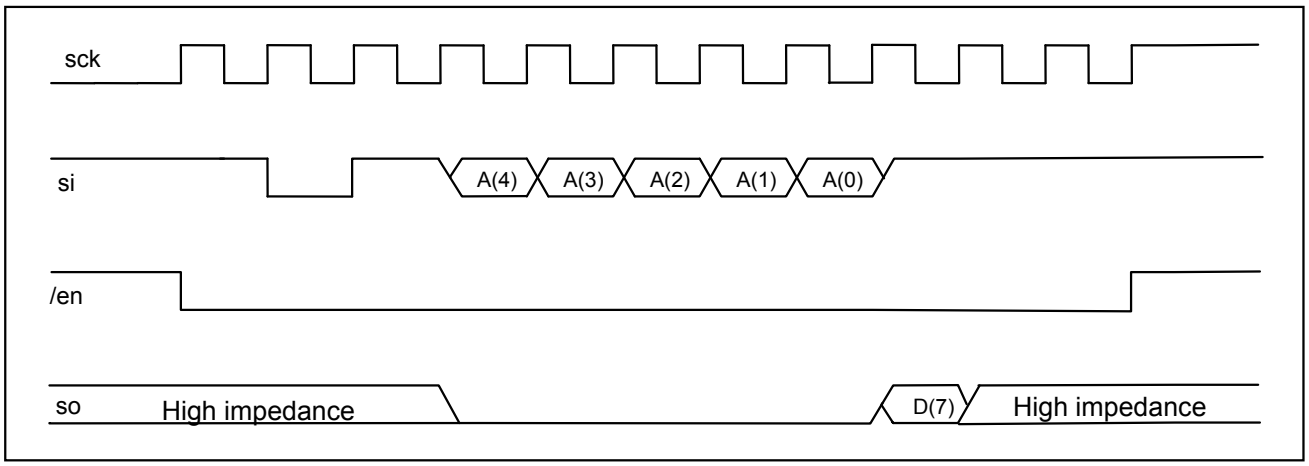


Figure 15: Read sequence of configuration register at address 0

5.2 CONFIGURATION AND STATUS REGISTERS

The XE1203F has several operating modes and configuration parameters which can be programmed by the user or the application. In addition, status information may be read from the circuit. Some of the operating modes, the status information and the configuration parameters are stored in a series of internal Configuration and Status Registers that can be accessed by the microcontroller through the 3-wire serial interface.

There are seven variable Configuration and Status Registers, as listed below in Table 9.

Name	Description	Size (bits)	Address (binary format)
ConfigSwitch	1-bit data to switch between 2 sets of user-predefined SWParam Configuration Registers	1 x 1	00000
RTParam	Receiver and transmitter parameters	2 x 8	00001 - 00010
FSParam	LO, Bitrate, Deviation and other frequency parameters	3 x 8	00011 - 00101
SWParam	2 sets of user-predefined configuration registers	6 x 8	00110 - 01011
DataOut	Status register which can be read through the 3-wire serial interface	2 x 8	01100 - 01101
ADParam	Additional parameters	5 x 8	01110 - 10010
Pattern	Reference pattern for the “pattern recognition” feature	4 x 8	10011 - 10110

Table 9: Configuration and Status Registers List

All the bits that are referred to as “reserved” in this section should be set to “0” during write operations.

5.2.1 The ConfigSwitch Register

When operating the XE1203F, it might by useful to quickly switch between two pre-defined operating modes, to save time and traffic on the 3-wire serial interface bus. This may occur when the XE1203F is required to switch quickly between receive and transmit mode, when it has to operate on two different carrier frequencies, or when it has to switch between the high linearity mode B and the high sensitivity mode A. For that purpose, the five parameters stored in the SWParam Configuration Register are duplicated: the configuration set#1 and the configuration set #2.

Depending on the ConfigSwitch 1-bit Register or the input level at the SWITCH pin, the XE1203F transceiver will use either the SWParam configuration set#1 or the set #2. If the RTParam_Switch_ext configuration parameter is low, then the SWParam configuration set is selected by the ConfigSwitch parameter – set#1 if ConfigSwitch is "0", set#2 if ConfigSwitch is "1". If the RTParam_Switch_ext configuration parameter is high, then the SWParam configuration set is selected by the SWITCH pin – set#1 if SWITCH is low, set#2 if SWITCH is high.

Table 10 below summarizes the chip configuration programming:

ConfigSwitch Register	SWITCH pin	RTParam_switch_ext configuration parameter	SWParam configuration set selected
0	SWITCH is an output: '1' in transmitter mode '0' in the other modes	0	Set #1: SWParam_mode_1 SWParam_Power_1 SWParam_Rmode_1 SWParam_t_delsig_in_1 SWParam_freq_1
1	SWITCH is an output: '1' in transmitter mode '0' in the other modes	0	Set #2: SWParam_mode_2 SWParam_Power_2 SWParam_Rmode_2 SWParam_t_delsig_in_2 SWParam_freq_2
X	0	1	Set #1: SWParam_mode_1 SWParam_Power_1 SWParam_Rmode_1 SWParam_t_delsig_in_1 SWParam_freq_1
X	1	1	Set #2: SWParam_mode_2 SWParam_Power_2 SWParam_Rmode_2 SWParam_t_delsig_in_2 SWParam_freq_2

Table 10: ConfigSwitch, SWITCH pin and SWParam Configuration Register

By default the configuration set#1 is used and register RTParam_switch_ext is set to '0'.

Note that a new value of the ConfigSwitch register or at the SWITCH pin should be modified when the EN signal is low. The actual switch to the newly selected set of SWParam register will be applied to the transceiver on the next rising edge of the EN signal.

5.2.2 RTParam Configuration Register

Receiver and transmitter parameters

Name	Bits	Address	Description
RTParam_Bitsync	7	00001	Bit synchronizer 0 -> disabled 1 -> enabled
RTParam_Barker	6	00001	BARKER coder/decoder: 0 -> disabled 1 -> enabled
RTParam_Rssi	5	00001	RSSI function: 0 -> disabled 1 -> enabled
RTParam_Rssir	4	00001	RSSI range: 0 -> low range (see 3.2.2) 1 -> high range (see 3.2.2)
RTParam_Fei	3	00001	FEI function: 0 -> disabled 1-> enabled
RTParam_BW	2	00001	Baseband filter bandwidth (BBW) 0 -> 200 kHz (DSB) 1 -> 600 kHz (DSB)
RTParam_Osc	1	00001	Reference frequency source: 0 -> internal crystal oscillator 1 -> external source
RTParam_Clkout	0	00001	CLKOUT - Reference frequency divided by 4,8,16,or 32: 0 -> disabled 1 -> enabled
RTParam_Stair	7	00010	Transmitter pre-filter rise/fall time: 0 -> 10% of bit duration 1 -> 20% of bit duration
RTParam_Filter	6	00010	Pre-filtering of the bit stream in transmitter mode 0 -> no filtering 1 -> filtering The filtering function is available only for the following bit rates and frequency deviations: FSPanam_Br = "1111110" -> BR = 1200 bit/s FSPanam_Br = "0111111" -> BR = 2400 bit/s FSPanam_Br = "0011111" -> BR = 4800 bit/s FSPanam_Br = "0001111" -> BR = 9600 bit/s FSPanam_Br = "0000111" -> BR = 19200 bit/s FSPanam_Br = "0000011" -> BR = 38400 bit/s FSPanam_Br = "0000001" -> BR = 76800 bit/s FSParam_Dev = "00101000" -> Δf = 40 kHz FSParam_Dev = "00110111" -> Δf = 55 kHz FSParam_Dev = "01010000" -> Δf = 80 kHz FSParam_Dev = "10100000" -> Δf = 160 kHz FSParam_Dev = "11001000" -> Δf = 200 kHz
RTParam_Modul	5	00010	Transmitter modulation: 0 -> enabled 1 -> disabled

Name	Bits	Address	Description
RTParam_IQAMP	4	00010	I&Q amplifiers: 0 -> disabled 1 -> enabled
RTParam_Switch_ext	3	00010	SWParam configuration set selection: 0 -> configuration set defined by ConfigSwitch. SWITCH is an output 1 -> configuration set defined by the pin SWITCH. SWITCH is an input
RTParam_Pattern	2	00010	Pattern recognition function: 0 -> disabled 1 -> enabled
RTParam_Band	1-0	00010	Frequency band: 01 -> 433 – 435 MHz 10 -> 868 – 870 MHz 11 -> 902 – 928 MHz

Table 11: RTParam Configuration Register

5.2.3 FSParam Configuration Register

LO, Bitrate, Deviation and other frequency parameters

Name	Bits	Address	Description
FSParam_Dev	7-0	00011	Frequency deviation ∆f: ∆f =int(FSParan_Dev) * 1 kHz, where int(x) = integer value of the binary representation of x. Example: 00000001 -> ∆f = 1 kHz 11111111 -> ∆f = 255 kHz
FSParam_Change_Osr	7	00100	OSR Mode (Oversampling Rate mode): 0 -> default Bit rate defined by FSParam_Br 1 -> variable OSR
FSParam_Br	6-0	00100	Bit rate (when "FSParam_Change_Osr" = "0"): Br = 152340/(int(FSParam_Br)+1), where int(x) = integer value of the binary representation of x. Example: 0000000 -> Br = 152.34 kbit/s 1111111 -> Br = 1.19 kbit/s 0000100 -> Br = 32.7 kbit/s used in Konnex mode
FSParam_OSR	7-0	00101	Define BR in terms of FSParam_BR and FS_Param_OSR: FSParam_OSR = "00011101" and FSParam_Change_Osr = '1' for Konnex standard

Table 12: FSParam Configuration Register

5.2.4 SWParam Configuration Register - switching parameters

The table below shows 2 sets of user-predefined configuration registers. Please refer to Section 5.2 for more details.

Name	Bits	Address	Description
SWParam_mode_1	7-6	00110	Chip mode configuration set#1: 00 -> Sleep mode 01 -> Stand by mode 10 -> Receiver mode 11 -> Transmitter mode
SWParam_Power_1	5-4	00110	Transmitter output power configuration set#1: 00 -> 0 dBm 01 -> 5 dBm 10 -> 10 dBm 11 -> 15 dBm
SWParam_Rmode_1	3	00110	Receiver Mode configuration set#1: 0 -> Mode A (high sensitivity) 1 -> Mode B (high linearity)
RESERVED	2-0	00110	RESERVED
SWParam_Freq_1	7-0 7-0	00111 01000	LO frequency in 2's complement representation configuration set#1: 00…0 -> Flo = middle of the range 0X…X-> Flo = higher than the middle of the range 1X…X-> Flo = lower than the middle of the range see Table 14 below
SWParam_node_2	7-6	01001	Chip mode configuration set#2: 00 -> Sleep mode 01 -> Stand by mode 10 -> RX mode 11 -> TX mode
SWParam_Power_2	5-4	01001	Transmitter output power configuration set#2: 00 -> 0 dBm 01 -> 5 dBm 10 -> 10 dBm 11 -> 15 dBm
SWParam_Rmode_2	3	010001	Receiver Mode configuration set#2: 0 -> Mode A (high sensitivity) 1 -> Mode B (high linearity)
RESERVED	2-0	01001	RESERVED
SWParam_Freq_2	7-0 7-0	01010 01011	LO frequency in 2's complement representation configuration set#2: 00…0 -> Flo = middle of the range 0X…X-> Flo = higher than the middle of the range 1X…X-> Flo = lower than the middle of the range see Table 14 below

Table 13: SWParam Configuration Register

The table following provides examples of LO frequency settings with FSParam_Freq:

SWParam_Freq_1 MSB (Byte address 00111) or SWParam_Freq_2 MSB (Byte address 01010) Bit 7 Bit 0	SWParam_Freq_1 LSB (Byte address 01000) or SWParam_Freq_1 LSB (Byte address 01011) Bit 7 Bit 0	Resulting LO setting Note: reference frequency = 39.0 MHz
00000000	00000000	F0, where F0 depends on the selected frequency band (see RTParam_Band) F0 = 434.0 MHz for the 433-435 MHz band F0 = 869.0 MHz for the 868-870 MHz band F0 = 915.0 MHz for the 902-928 MHz band
00000000	00000001	F0 + 500 Hz
00000000	00000010	F0 + 2 * 500 Hz
11111111	11111111	F0 – 500 Hz
11111111	11111110	F0 – 2 * 500 Hz

Table 14: Examples of LO frequency settings

5.2.5 DataOut Status Register

Status register which can be read through the 3-wire serial interface

Name	Bits	Address	Description
DataOut_Rssi	7-6	01100	RSSI output: 0 0 -> lowest level, ≤VTHR1 0 1 -> 2nd level, VTHR1<RSSI level≤VTHR2 1 0 -> 3rd level, VTHR2<RSSI level≤VTHR3 1 1 -> highest level, VTHR3<RSSI level
RESERVED	5-4	01100	RESERVED
DataOut_MSB_fei	3-0	01100	Fei output (MSB)
DataOut_LSB_fei	7-0	01101	Fei output (LSB) Ferror = (Br/8)*int(DataOut_MSB_fei & DataOut_LSB_fei) Where int(x) = integer value of the binary representation of x

Table 15: DataOut Status Register

5.2.6 ADParam Configuration Register

Additional parameters

Name	Bits	Address	Description
ADParam_Psize	7-6	01110	Size of reference pattern recognition word: 0 0 -> 8 bits 0 1 -> 16 bits 1 0 -> 24 bits 1 1 -> 32 bits
ADParam_Ptol	5-4	01110	Number of tolerated errors for the pattern recognition: 00 -> 0 error 01 -> 1 error 10 -> 2 errors 11 -> 3 errors

Name	Bits	Address	Description
ADParam_Clk_freq	3-2	01110	CLKOUT frequency (if enabled) 00 -> 1.22 MHz (div ratio :32) 01 -> 2.44 MHz (div ratio :16) 10 -> 4.87 MHz (div ratio :8) 11 -> 9.75 MHz (div ratio :4)
ADParam_Invert	1	01110	Inversion of Rx output data: 0 -> disabled 1 -> enabled
ADParam_RegBW	0	01110	Baseband filter bandwidth calibration: 0 -> enabled 1 -> disabled
ADParam_Regfreq	7	01111	Period of baseband filter bandwidth calibration whilst Rx enabled: 0 -> only at start-up of the receiver 1 -> 60 seconds (default mode) or 7 seconds (test mode)
ADParam_Regcond	6	01111	Baseband filter bandwidth calibration as a function of selected bandwidth: 0 -> calibration restarted each time the bandwidth is changed 1 -> no calibration when the bandwidth is changed
ADParam_Xsel	5	01111	Selection of the XOSC load capacitance mode: 0 -> CL+C0 = 15 pF 1 -> CL+C0 = 11 pF, low current mode
ADParam_Resxosc	4-1	01111	Selection of the value of the shunt resistor across ports TKA and TKB for a third overtone XTAL operation: 0000 -> 3800 kΩ 0001 -> 2.55 kΩ 0010 -> 4.65 kΩ 0011 -> 1.78 kΩ 0100 -> 8.79 kΩ 0101 -> 2.07 kΩ 0110 -> 3.22 kΩ 0111 -> 1.56 kΩ 1000 -> 16.55 kΩ 1001 -> 2.26 kΩ 1010 -> 3.79 kΩ 1011 -> 1.66 kΩ 1100 -> 6.04 kΩ 1101 -> 1.91 kΩ 1110 -> 2.81 kΩ 1111 -> 1.48 kΩ
ADParam_enable_konnex	0	01111	Konnex mode: 0 -> disabled 1 -> enabled
ADParam_Chge_thres	7	10000	Enable programming of the sync and acquisition thresholds: 0 -> threshold are hard-coded and sync-loss counter is 50 bits 1 -> threshold are defined by BParam_Sync_thres and BParam_Trac_thres Sync loss counter is variable and defined by ADParam_Sync_loss
ADParam_Sync_thres	6:0	10000	Barker mode sync acquisition threshold
ADParam_disable_data_bidir	7	10001	DATA port bidirectional mode: 0 -> enabled 1 -> disabled: DATA = output, DATAIN = input
ADParam_Trac_thres	6-0	10001	Threshold for tracking Barker mode

Name	Bits	Address	Description
ADParam_Fix_bsync	7	10010	bit synchronizer configuration: 0-> default configuration 1-> high-interference environment
ADParam_Sync_loss	6-0	10010	Number of bits before sync loss detection for Barker decoding algorithm

Table 16: ADParam Configuration Register

5.2.7 Pattern register

This register holds the user supplied reference pattern of 8, 16, 24, or 32 bits (see the ADParam_Psize parameter). The first byte of this pattern is always stored in the byte at address A[4:0] = 10011. If used, the 2nd byte is stored at address A[4:0] = 10100, the 3rd byte at address A[4:0] = 10101, and finally the 4th byte at address A[4:0] = 01011. The MSB bit of the reference pattern is always bit 7 of address 10011.

Comparing the demodulated data, the first bit received of the last word is compared with bit 7 (the MSB) of byte address 10011. The last bit received is compared with bit 0 (the LSB) in the Pattern register.

Name	Bits	Byte Address	Description
PATParam_Pattern	7-0	10011 10100 10101 10110	1st byte of the reference pattern 2nd byte 3rd byte 4th byte

Table 17: PATParam Pattern Registers

Example of pattern recognition with a 32-bit pattern:

Byte Address 10011 Bit 7 Bit 0	Byte Address 10100 Bit 7 Bit 0	Byte Address 10101 Bit 7 Bit 0	Byte Address 10110 Bit 7 Bit 0
10010011	10101010	10010011	10101010
101 10010011	10101010	10010011	10101010

previous bits from demodulator

last bit received

Figure 16: Example of pattern recognition with a 32-bit pattern

Example of pattern recognition with an 8-bit pattern:

Byte Address 10011 Bit 7 Bit 0	Byte Address 10100 Bit 7 Bit 0	Byte Address 10101 Bit 7 Bit 0	Byte Address 10110 Bit 7 Bit 0
10010011	Xxxxxxxx	Xxxxxxxx	Xxxxxxxx
101 10010011			

previous bits from demodulator

last bit received

Figure 17: Example of pattern recognition with an 8-bit pattern

5.2.8 Test Registers and additional settings

Some settings in this 9-byte register can be used to have access to additional configurations of the circuit. These settings are described in the Table 18 below:

Name	Bits	Byte Address	Description
TParam_BW	3	10111	Baseband filter bandwidth (DSB): 0 -> default values defined by RTParam_BW (200 and 600 kHz) 1 -> 300kHz
TParam_HPF	1-0	10111	SSB cut-off frequency of the HPF stage (for cancellation of DC and low-frequency offsets in the baseband circuit): 00 -> 4.3 kHz 01 -> 8.7 kHz 10 -> 17.3 kHz 11 -> 34.6 kHz

Table 18: Test registers and additional settings

5.3 OPERATING MODES

The XE1203F has four main operating modes illustrated in Table 19 below.

These modes are defined by the content of the SWParam_mode_1 parameter when configuration set #1 is selected, or by the content of the SWParam_mode_2 parameter when configuration set #2 is selected. See also Section 5.2.1.

Mode	SWParam_mode1(1:0) SWParam_mode_2(1:0)	Description
Sleep mode	0 0	-
Standby mode	0 0	Quartz oscillator enabled
Receiver mode	1 0	Quartz oscillator, Frequency synthesizer, Receiver enabled
Transmitter mode	1 1	Quartz oscillator, Frequency synthesizer, Transmitter enabled

Table 19: XE1203F Operating Modes

5.3.1 Standard power up sequence for the receiver and transmitter

The XE1203F circuit can be switched between any configuration by using the 3 wire interface (ConfigSwitch) or by using the pad SWITCH. This section describes the switching sequence of the chip. Figure 18 shows the transition sequence from sleep mode to receiver mode via stand by mode.

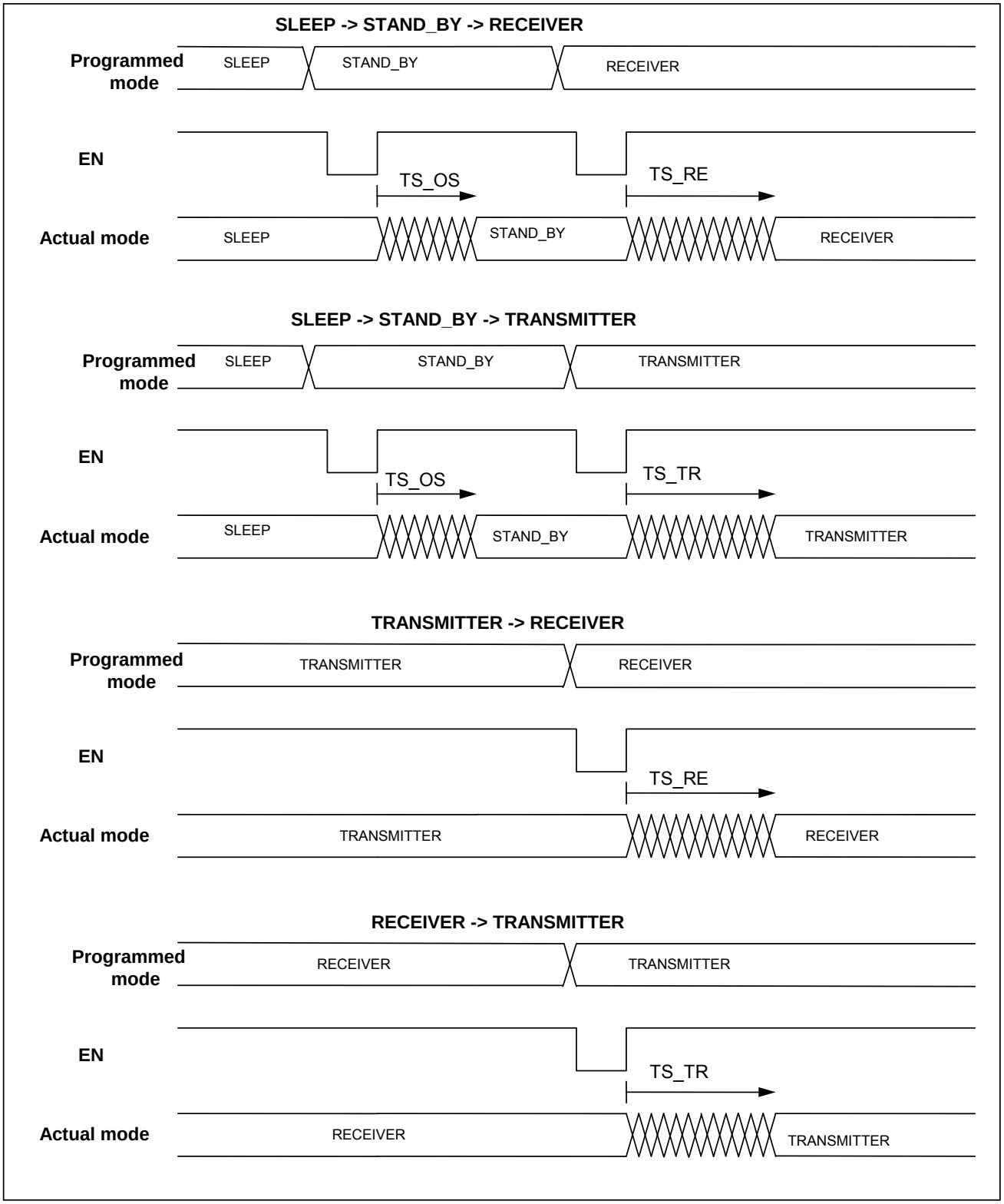


Figure 18: Mode transition

5.4 SELECTION OF THE REFERENCE FREQUENCY

The reference clock used by the frequency synthesizer and internal digital circuit can be generated internally by connecting an external crystal between XTA and XTB, or provided by an external oscillator. When using an external source, the signal should be applied to port XTA and the RTParam_Osc configuration bit should be set to "1".

The XE1203F can be used with a 39 MHz crystal operating in fundamental mode or in 3rd overtone mode. For third overtone operation, an internal resistor to be switched across the crystal terminals XTA and XTB is required. This resistor can be selected by programming the ADParam_Resxosc(3:0) parameter. The required value depends on the overtone crystal specification.

When using 3rd overtone mode, the user should be aware that during its power up the XE1203F oscillator will attempt to start at the fundamental frequency of the crystal. It will only switch to the overtone mode when properly programmed through the 3-wire interface bus. As a result, if a microcontroller uses the XE1203F CLKOUT as a clock source it is advisable to allow the oscillator frequency to settle before undertaking any time or timing sensitive operations.

For fundamental mode operation, the ADParam_Resxosc(3:0) parameter is set to the default value of ”0000’’. This switches a 3.8 MΩ resistance across the crystal terminals.

5.5 CLOCK OUTPUT INTERFACE

When register “RTParam_Clkout” is set to “1” , the reference frequency is divided by 4, 8, 16 or 32, depending on the value of the register “ADParam_Clkfreq”, and provides a reference signal at CLKOUT for a microcontroller or external circuitry. If the reference frequency is 39 MHz, then the output frequency available at CLKOUT is as defined in Table 20 below:

ADParam_Clkfreq	CLKOUT frequency
00	1.22 MHz
01	2.44 MHz
10	4.87 MHz
11	9.75 MHz

Table 20: Clock Output Frequency Selection

When the XE1203F is in sleep mode, CLKOUT is disabled even if RTParam_Clkout remains high.

5.6 DEFAULT SETTINGS AT POWER-UP

The internally generated power-on-reset signal sets the RTParam, FSParam, ADParam and Pattern registers to the 00hex value.

There is one important exception for CLKOUT. Although the RTPAram_CLkout is set to ”0” at power-on reset, meaning the feature should be disabled, the XE1203F will generate a CLKOUT signal after a power-on reset to provide a clock signal to a possible microcontroller connected to it. After a power-on reset, CLKOUT will be the lowest available frequency, e.g. 1.22 MHz with a 39 MHz reference frequency. Then, on the first rising edge of the /EN signal – for example after a programming sequence via the 3-wire interface bus - the content of the configuration registers will be updated. If the RTParam Configuration Register has not been programmed during this first sequence after a power-on reset, the CLKOUT clock signal will be disabled. It is strongly advised to initialize the RTPAram_CLkout parameter appropriately during the first programming sequence after a power-on reset, especially if an external microcontroller does use this CLKOUT clock signal to operate.

It is recommended to initialize the XE1203F registers immediately after power-up.

6 APPLICATION INFORMATION

This section provides details of the recommended component values for the frequency dependant blocks of the XE1203F. Note that these values are dependent upon circuit layout and PCB structure, and that decoupling components have been omitted for clarity.

6.1 RECEIVER MATCHING NETWORK

The schematic of the matching network at the input of the receiver is given below in Figure 19 (for a source impedance of 50Ω).

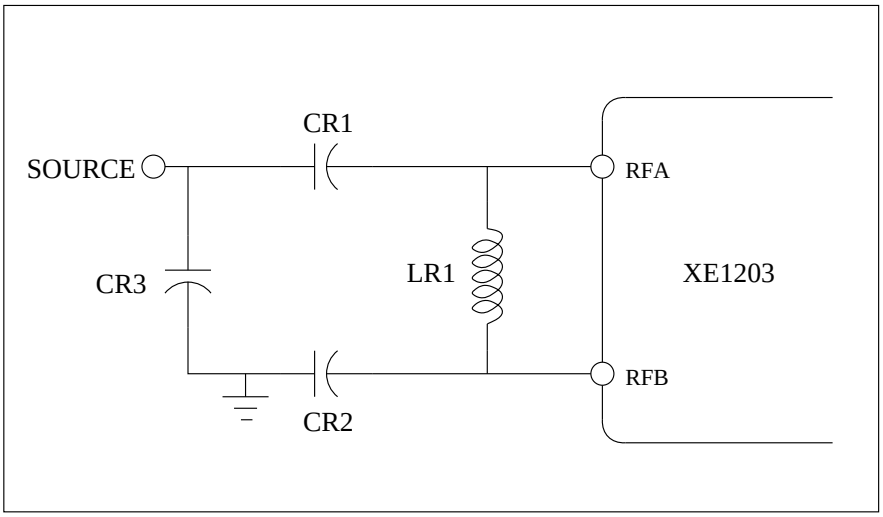


Figure 19: Receiver matching network

The typical recommended values for the external components are shown in Table 21:

Name	Typical Value for 434 MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CR1	1.5 pF	1.5 pF	1.0 pF	± 5%
CR2	1.5 pF	1.2 pF	1.0 pF	± 5%
CR3	NC	NC	NC	± 5%
LR1	100 nH	27 nH	27 nH	± 5 %

Table 21: Typical component values for the matching network

6.2 TRANSMITTER MATCHING NETWORK

The optimum load impedances for 15 dBm output power at the three main frequencies are shown in Table 22:

	434 MHz	868 MHz	915 MHz
PA optimum load	102 – 12j	78 + 19j	83 + 18j

Table 22: Optimum load impedances for 15 dBm output power

The Smith charts in Figure 20, Figure 21, and Figure 22 below show contours of output power versus load impedance when the highest transmit level is selected, i.e. 15 dBm:

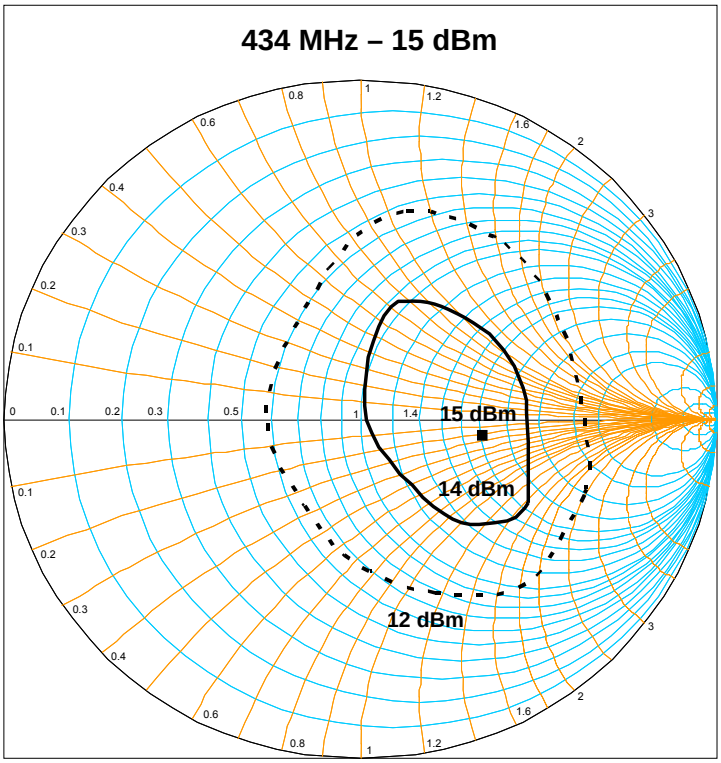


Figure 20: Output power vs. load impedance at 434 MHz

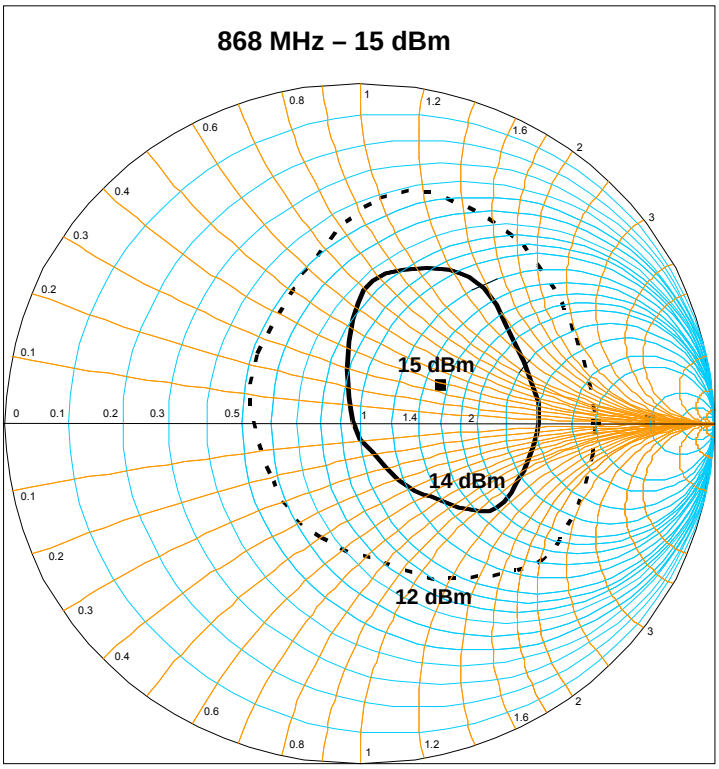


Figure 21: Output power vs. load impedance at 868 MHz

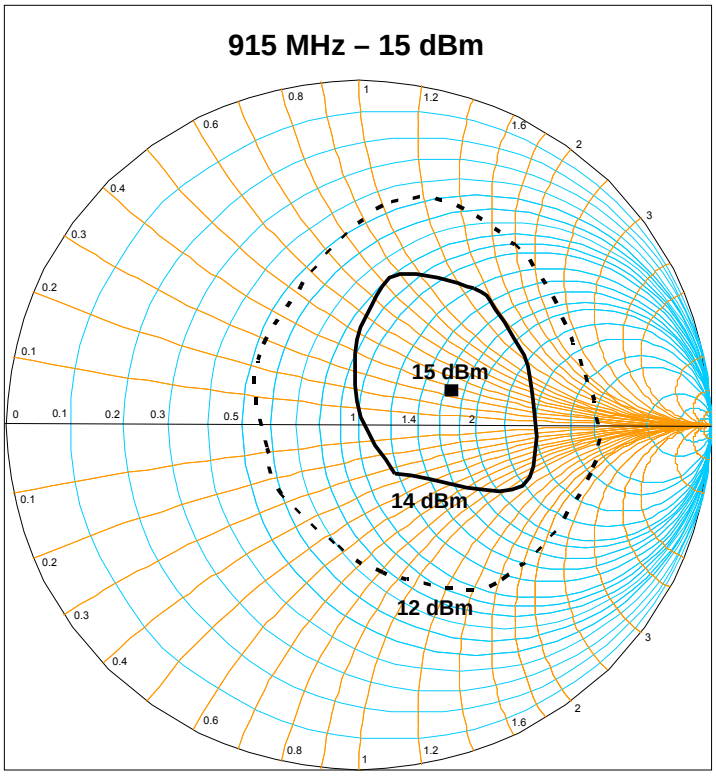


Figure 22: Output power vs. load impedance at 915 MHz

The schematic of the recommended matching network at the output of the transmitter is shown in Figure 23 below. The two Π-sections are used to provide harmonic filtering in order to satisfy FCC and ETSI regulations.

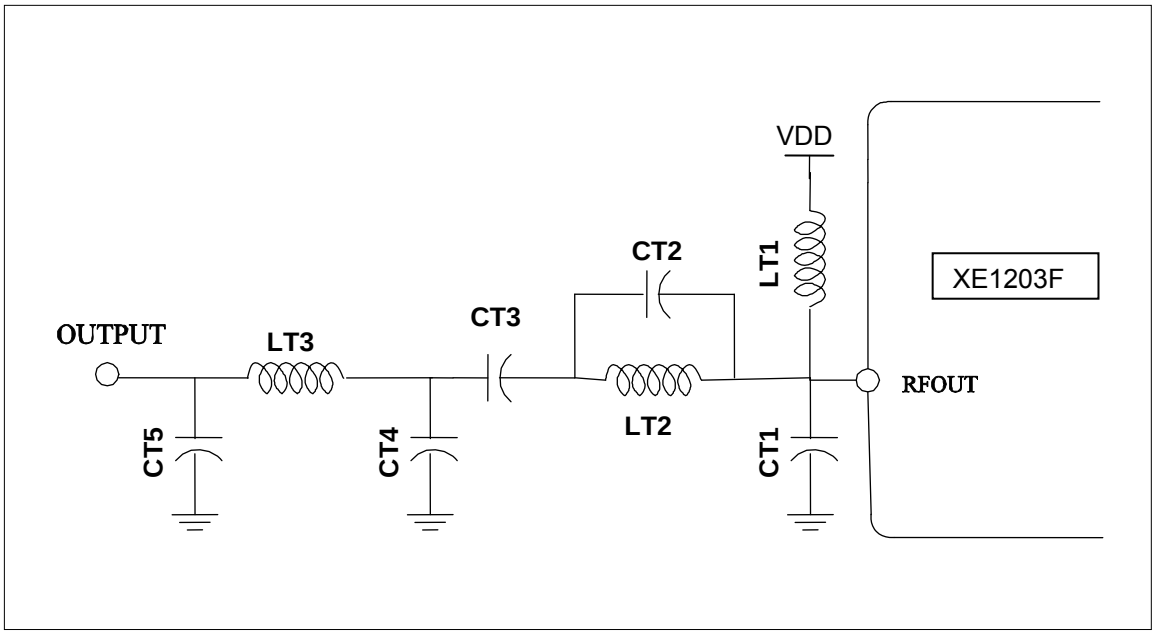


Figure 23: Transmitter output network

The typical component values of this matching circuit are shown below in Table 23:

Name	Typical Value for 434 MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CT1	6.8 pF	1.5 pF	1.8 pF	± 5%
CT2	1.0 pF	0.56 pF	NC	± 5%
CT3	22 pF	15 pF	33 pF	± 5%
CT4	6.8 pF	3.3 pF	3.3 pF	± 5%
CT5	4.7 pF	2.2 pF	2.2 pF	± 5%
LT1	33 nH	39 nH	47 nH	± 5%
LT2	22 nH	10 nH	10 nH	± 5%
LT3	22 nH	8.2 nH	8.2 nH	± 5%

Table 23: Typical component values for the recommended matching network at the output of the transmitter

6.3 VCO TANK

The tank of the VCO is implemented with one inductor in parallel with one capacitor. The characteristics of these two components must be as follows:

Name	Typical Value for 434 MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CV1	1.0 pF	NC	NC	± 5 %
LV1	33 nH	8.2 nH	6.8 nH	± 2 %

Table 24: VCO tank external components

6.4 LOOP FILTER OF THE FREQUENCY SYNTHESIZER

The loop filter of the frequency synthesizer is shown in Figure 24 below:

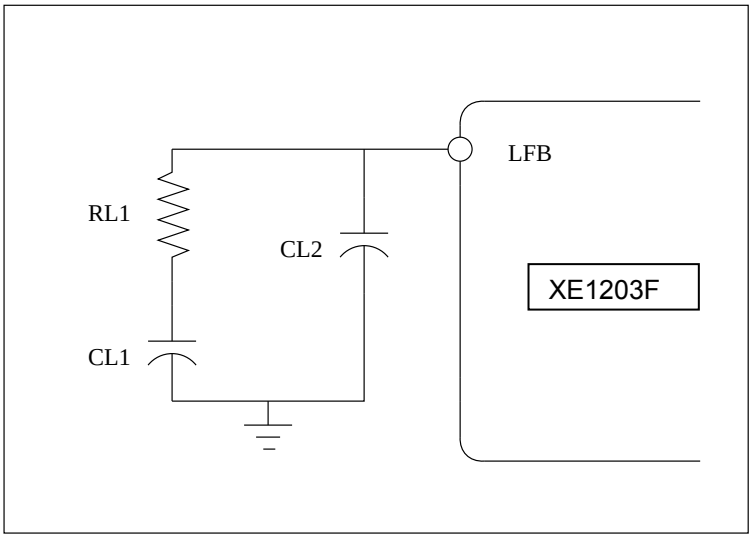


Figure 24: Loop filter of the frequency synthesizer

The values recommended for applications using bit rates up to 38.4kbit/s are given in Table 25 below:

Name	Typical Value for 434 MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CL1	22 nF	22 nF	22 nF	± 5%
CL2	1.2 nF	1.2 nF	1.2 nF	± 5%
RL1	560Ω	470Ω	470Ω	± 5%

Table 25: Typical loop filter values for bit rates up to 38.4 kbit/s

The values recommended for applications using bit rates higher than 38.4 kbit/s are given in Table 26 below:

Name	Typical Value for 434 MHz	Typical Value for 868 MHz	Typical Value for 915 MHz	Tolerance
CL1	3.3 nF	4.7nF	4.7 nF	± 5%
CL2	220 pF	330 pF	330 pF	± 5%
RL1	1.2 kΩ	1 kΩ	1 kΩ	± 5%

Table 26: Typical loop filter values for bit rates higher than 38.4 kbit/s

6.5 FREQUENCY SYNTHESIZER REFERENCE CRYSTAL

For narrow band applications, where the lowest frequency deviation and the narrowest baseband filter are selected, the crystal for reference oscillator of the frequency synthesizer should have the following typical characteristics:

Name	Description	Min. value	Typ. value	Max. value
Fs	Nominal frequency	-	39.0 MHz (fundamental)	-
CL	Load capacitance for fs (on-chip)	-	8 pF (*)	-
Rm	Motional resistance	-	-	40Ω
Cm	Motional capacitance	-	-	30 fF
C0	Shunt capacitance	-	-	7 pF (*)
Δfs(0)	Calibration tolerance at 25 °C	-	-	10 ppm
Δfs(ΔT)	Stability over temperature range (-40 °C to 85 °C)	-	-	10 ppm
Δfs(Δt)	Aging tolerance in first 5 years	-	-	5 ppm

Table 27: Crystal characteristics

(*) The on-chip oscillator mode is user-defined by programming ADParam_Xsel parameter: the first for CL = 8 pF and C0 = 7pF, and the second for CL = 8 pF and C0 = 3 pF; the latter will allow higher amplitude for the internal signal with a slightly lower consumption.

The electrical specifications given in section 3.2.2 are valid for a crystal having the specifications given in Table 27. For wide band applications requiring less frequency stability, the values for Δfs(0), Δfs(ΔT), and/or Δfs(Δt) can be relaxed. In this case foffset + BWssb should be lower than BWfilter, where foffset is the offset (error) on the carrier frequency (the sum of Δfs(0), Δfs(ΔT), and/or Δfs(Δt)), BWssb is the single side-band bandwidth of the signal, and BWfilter is the single side-band bandwidth of the base-band filter.

The overtone crystal usage may result in higher oscillator start-up time than fundamental mode. The overtone crystal should be designed for Cload = 8 to 10 pF and has parameters of Rm < 60Ω, C0 < 7 pF.

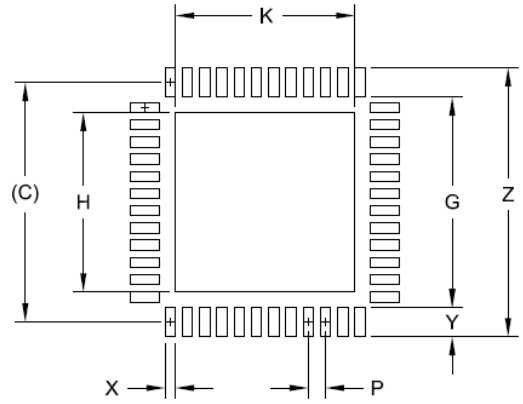
7 REVISION HISTORY

Revision 2

- Update description of Bit Synchronizer operation
- Change to package drawing and description

8 PACKAGING INFORMATION

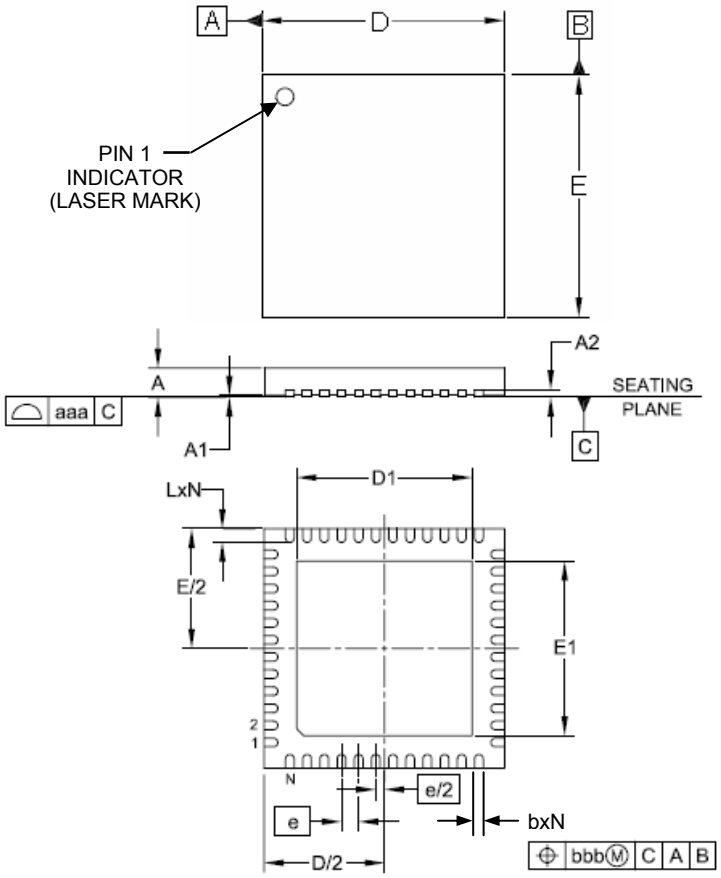
XE1203F is available in a 48-lead MLPQ RoHS green package as shown in Figure 25 below.
Please note that the Exposed Die Pad should be connected to ground.



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.274)	(6.95)
G	.240	6.10
H	.205	5.20
K	.205	5.20
P	.020	0.50
X	.012	0.30
Y	.033	0.85
Z	.307	7.80

NOTES

1. Controlling dimensions are in millimeters (angles in degrees)
2. This land pattern is for reference only. Consult your manufacturing group to ensure your company's manufacturing guidelines are met
3. Thermal vias in the land pattern of the exposed pad shall be connected to a system ground plane. Failure to do so may compromise thermal and/or functional performance of the device.
4. Square package – dimensions apply in both "X" and "Y" directions



DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2		(.008)			(0.20)	
b	.007	.010	.012	0.18	0.25	0.30
D	.272	.276	.028	6.90	7.00	7.10
D1	.197	.201	.205	5.00	5.10	5.20
E	.272	.276	.028	6.90	7.00	7.10
E1	.197	.201	.205	5.00	5.10	5.20
e		.020 BSC			0.50 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		48			48	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES

1. Controlling dimensions are in millimeters (angles in degrees)
2. Coplanarity applies to the exposed pad as well as the terminals

Figure 25: Land Pattern and Package Outline Drawings

Contact Information

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