

GENERAL DESCRIPTION

The SGM61020 is a high efficiency synchronous Buck DC/DC converter with 2A output current capability and adjustable output voltage. The input supply voltage is in the range of 2.5V to 5.5V. Using adaptive off-time peak current control, the efficiency of this device is higher than 80% for loads over 1mA and reaches 95% in the moderate load ranges (5V to 3.3V).

This device operates with a quasi-fixed 1.5MHz pulse width modulation (PWM) mode for moderate or heavy loads. But at light loads, pulse skip modulation is used for power-save mode (PSM). The PSM operating quiescent current is very low, typically 42µA, which is well suitable for battery-powered applications to increase standby time. Despite such low quiescent current, the transient response to large load variations is excellent. The device shutdown current is typically 0.03µA.

The SGM61020 provides an adjustable output voltage by an external resistor divider. The device is capable for low dropout operation with 100% duty cycle. Some other features include internal soft-start for limiting startup inrush current, over-current and thermal shutdown protections, enable input and power good output (for SGM61020P version only).

The SGM61020 is available in Green SOT-23-5 and SOT-563-6 packages.

TYPICAL APPLICATION

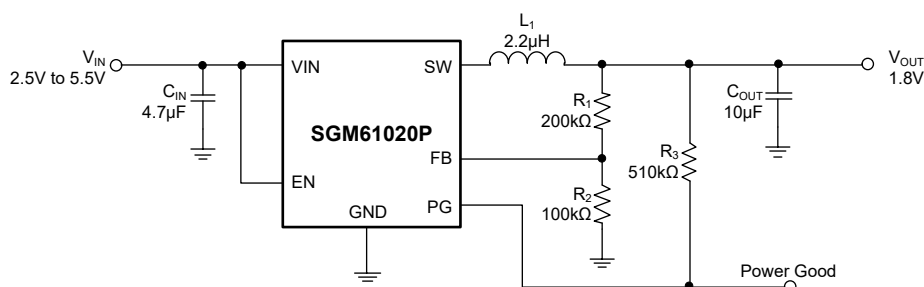


Figure 1. Typical Application Circuit

FEATURES

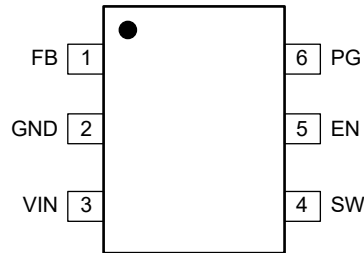
- 2.5V to 5.5V Input Voltage Range
- Adjustable Output Voltage from 0.6V to V_{IN}
- Up to 95% Efficiency
- Low $R_{DS(ON)}$ MOSFET Switches (100mΩ/55mΩ)
- Power-Save Mode for Light Load Efficiency
- 42µA (TYP) Operating Quiescent Current
- 100% Duty Cycle Capability for Low Dropout
- 1.5MHz PWM Switching Frequency
- Power Good Output (SGM61020P Only)
- Over-Current Protection
- Thermal Shutdown Protection
- Input Under-Voltage Lockout (UVLO) Protection
- Small Packaging:
 - SGM61020: Available in Green SOT-23-5 and SOT-563-6 Packages
 - SGM61020P: Available in a Green SOT-563-6 Package

APPLICATIONS

- Battery-Powered Applications
- Point-of-Load
- Processor Power Supplies
- Hard Disk Drives (HDD)/Solid State Drives (SSD)

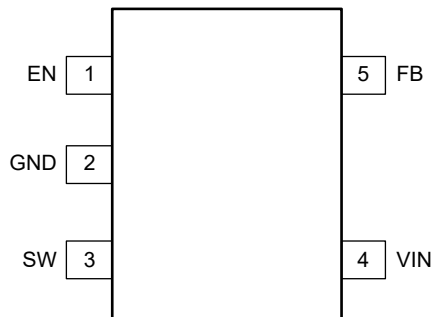
PIN CONFIGURATIONS

SGM61020P (TOP VIEW)



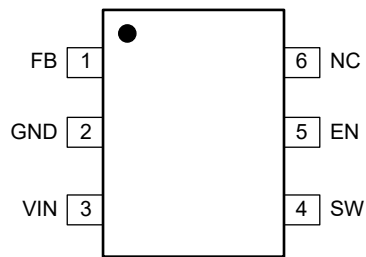
SOT-563-6

SGM61020 (TOP VIEW)



SOT-23-5

SGM61020 (TOP VIEW)



SOT-563-6

PIN DESCRIPTION

PIN		NAME	I/O	FUNCTION
SOT-23-5	SOT-563-6			
1	5	EN	I	Active High Enable Input Pin. Apply a logic low to shut down the device or pull EN up to VIN pin to enable the device. Do not leave EN floating.
2	2	GND	G	Ground Pin.
3	4	SW	P	Switching Node Output Pin. Connect to the output inductor.
4	3	VIN	P	Power Supply Input. Decouple VIN with at least 4.7µF ceramic capacitor to GND, as close to the device as possible. (If the input voltage oscillates, the input capacitance can be increased.)
5	1	FB	I	Feedback Input. Connect a resistor divider between the output voltage sense point and ground and tap it to the FB pin to set the output voltage.
—	6	NC	—	No Connection. This pin can be left open or connected to GND.
		PG	O	Open-Drain Power Good Output Pin (SGM61020P Only). Pull it up with a resistor to a positive voltage no more than 5.5V. It can be left open if not used.

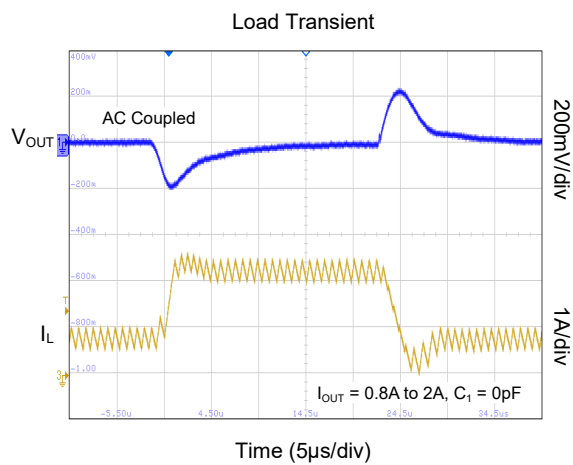
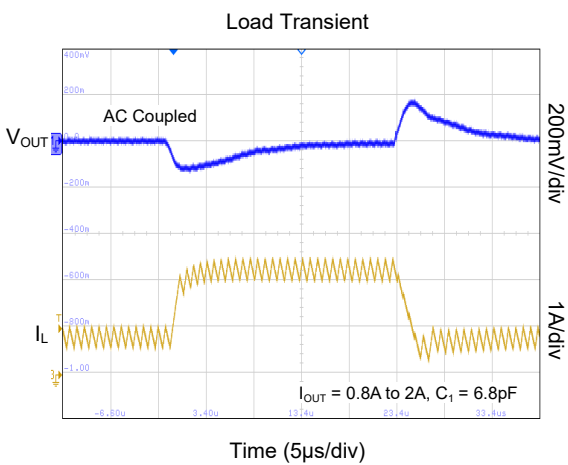
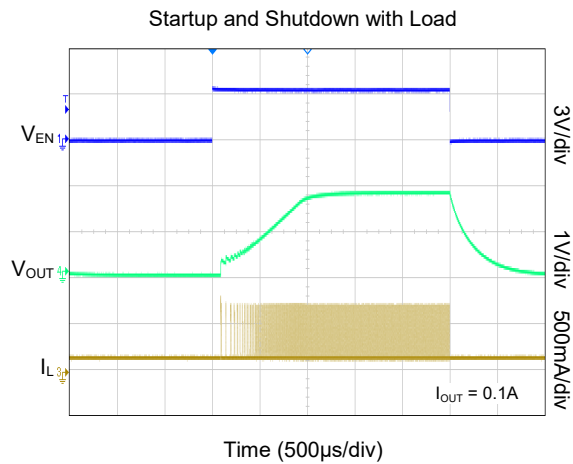
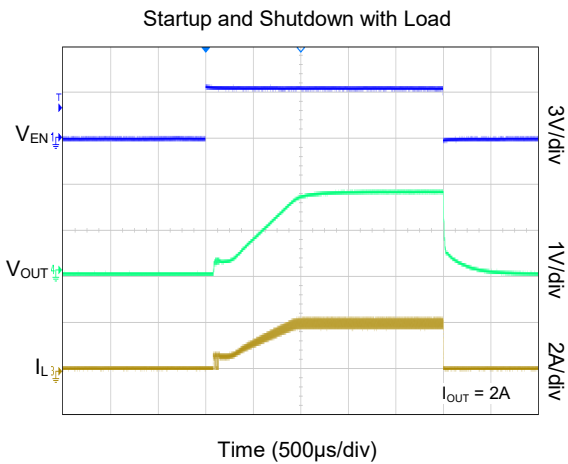
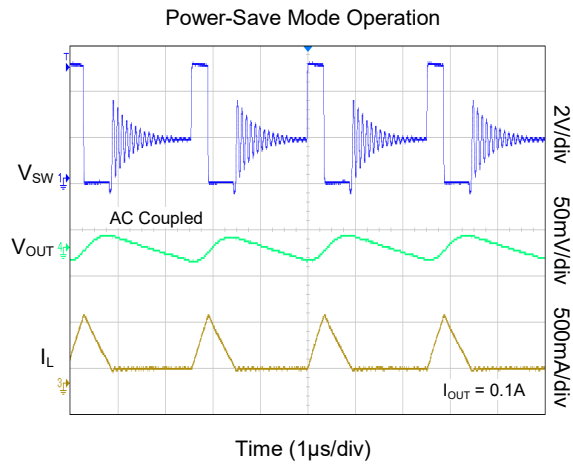
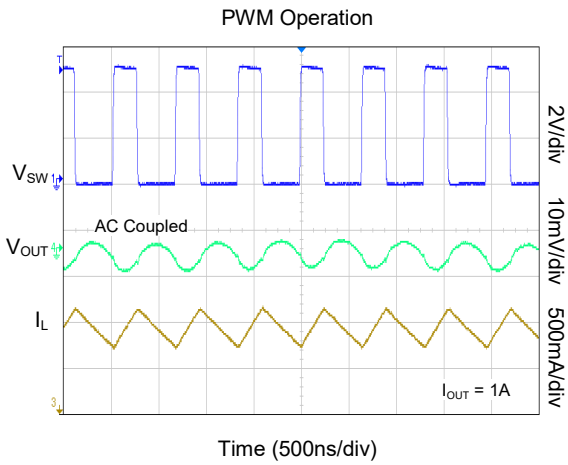
NOTE: I = input, O = output, P = power, G = ground.

ELECTRICAL CHARACTERISTICS(V_{IN} = 5V, T_J = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Power Supply							
Quiescent Current into VIN Pin	I _Q	Not switching		42		μA	
Shutdown Current into VIN Pin	I _{SD}	EN = 0V		0.03	1	μA	
Under-Voltage Lockout Threshold	V _{UVLO}	V _{IN} falling		2.30	2.40	V	
Under-Voltage Lockout Hysteresis	V _{HYS}			100		mV	
Thermal Shutdown Threshold	T _{JSD}	T _J rising		150		°C	
Thermal Shutdown Hysteresis		T _J falling		130		°C	
Logic Interface							
High-Level Threshold at EN Pin	V _{IH}	V _{IN} = 2.5V to 5.5V		0.98	1.20	V	
Low-Level Threshold at EN Pin	V _{IL}	V _{IN} = 2.5V to 5.5V	0.40	0.86		V	
Soft Startup Time	t _{SS}	Measure from 0 to 95% × V _{OUT} (set)		800		μs	
Output							
Feedback Regulation Voltage	V _{FB}	SOT-23-5	0.588	0.600	0.612	V	
		SOT-563-6	0.594	0.600	0.606		
High-side FET On-Resistance	R _{DSON}	SOT-23-5		100		mΩ	
		SOT-563-6		78			
Low-side FET On-Resistance		SOT-23-5			55		mΩ
		SOT-563-6			41		
High-side FET Current Limit	I _{LIM}		2.8	3.2	3.6	A	
Switching Frequency	f _{SW}	V _{OUT} = 2.5V		1.5		MHz	
SGM61020P Only							
Power Good Threshold	V _{PG}	V _{FB} rising, referenced to V _{FB} nominal		95% × V _{REF}		V	
		V _{FB} falling, referenced to V _{FB} nominal		90% × V _{REF}			
Power Good Low-Level Output Voltage	V _{PG_OL}	I _{SINK} = 1mA		0.1	0.4	V	
Input Leakage Current into PG Pin	I _{PG_LKG}	V _{PG} = 5.0V		0.01		μA	
Power Good Delay Time	t _{PG_DLY}	V _{FB} falling		45		μs	

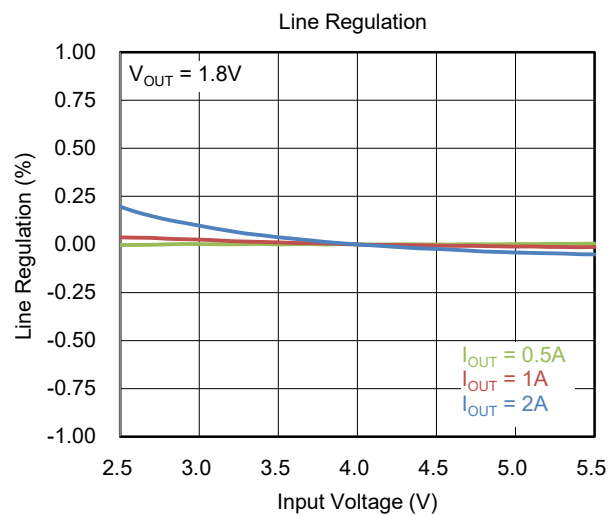
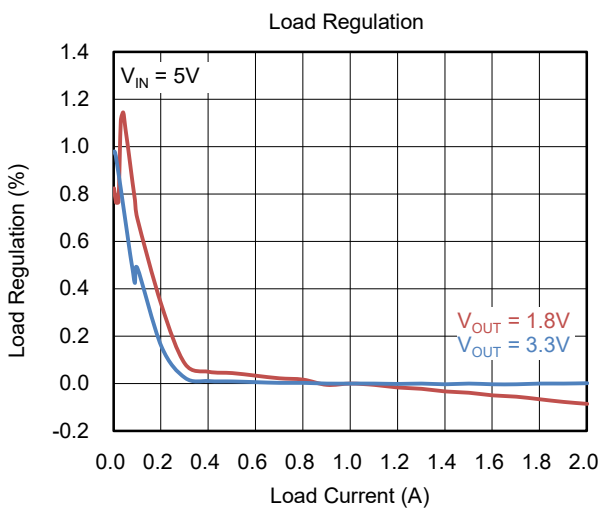
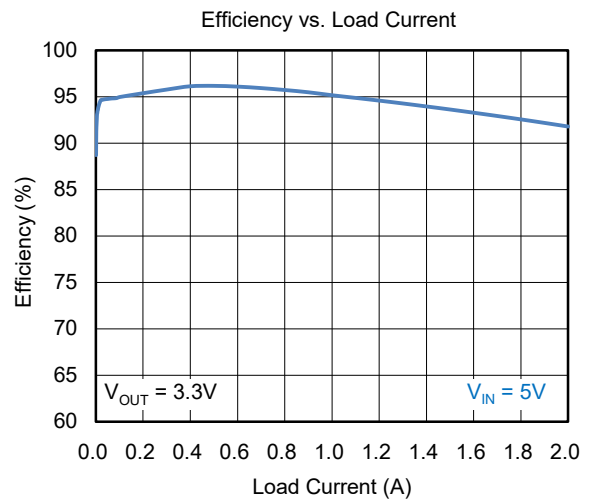
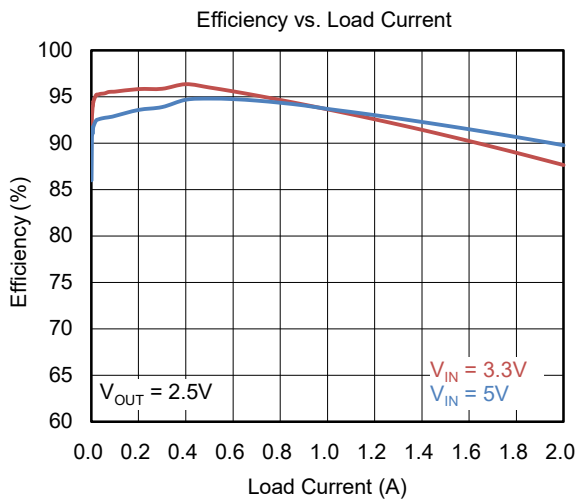
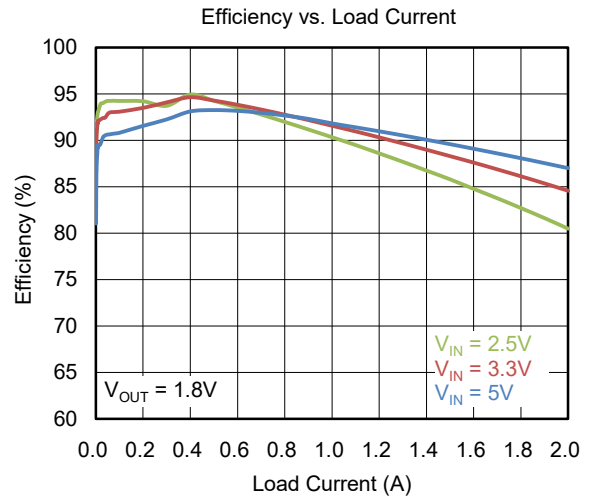
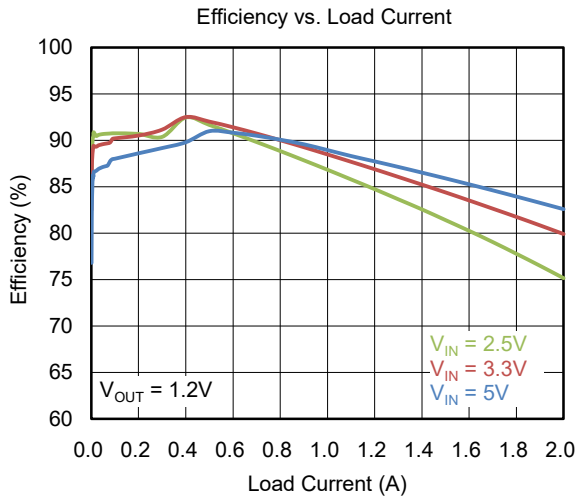
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L₁ = 2.2µH, C_{OUT} = 10µF, unless otherwise noted.



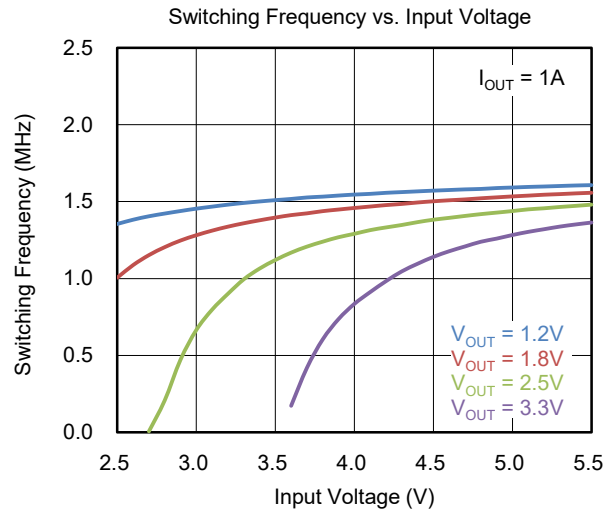
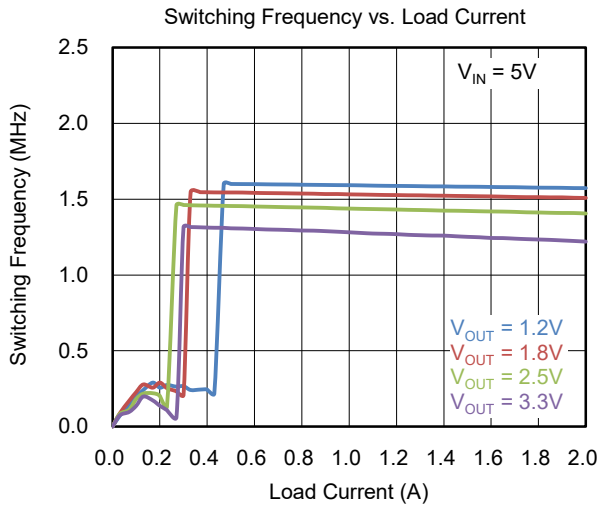
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L₁ = 2.2µH (DCR = 18mΩ), unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L₁ = 2.2µH (DCR = 18mΩ), unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

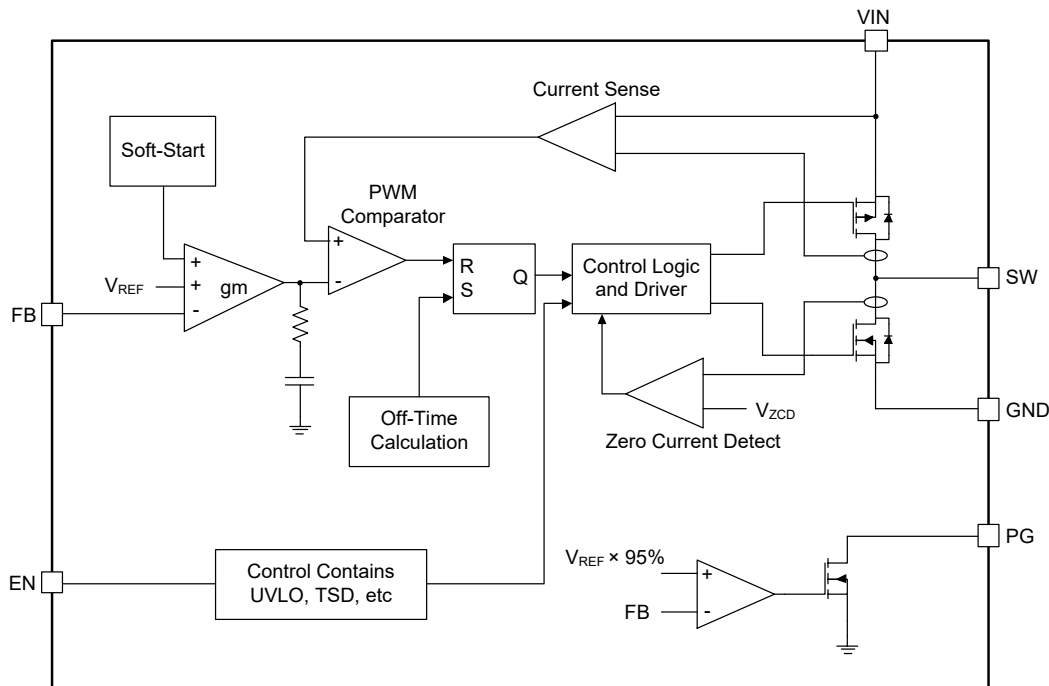


Figure 2. SGM61020/SGM61020P Block Diagram

DETAILED DESCRIPTION

Overview

The SGM61020 is a high efficiency Buck switching converter optimized for handheld battery-powered applications. It operates at a quasi-fixed frequency of 1.5MHz and uses adaptive off-time PWM control for the moderate to heavy load range. This allows using a small inductor and small capacitors for compact designs. At light load condition, this device operates in power-save mode to reduce the switching frequency and losses for longer battery life. The power-save mode quiescent current is 42µA (TYP) while the shutdown current is only 0.03µA (TYP).

Under-Voltage Lockout Protection

When the input voltage is below the UVLO threshold (2.3V, TYP), the device is shut down. If the input voltage rises above the UVLO threshold plus a 100mV hysteresis, the IC will restart.

Enable Input

The EN pin is a digital control that turns the converter on and off states. Drive EN logic high to turn on the device; drive it logic low to turn it off. Connect the EN pin directly to a voltage source that can't be higher than the VIN pin. The EN input should not be left floating.

Power Good Output (SGM61020P Only)

The PG pin is an open-drain output. PG requires a pull-up resistor (e.g. 510kΩ). PG pin is pulled to GND before the output voltage is above 95% of the nominal voltage. After FB voltage reaches 95% of VREF, the PG pin is pulled high immediately. When the FB voltage drops below 90% of VREF, the PG pin will be pulled low after a 45µs delay. Leave the PG pin unconnected when not used.

Table 1. PG Output Logic

Reason	Conditions	PG Status	
		High Z	Low
Output Voltage	EN = High, V _{FB} ≥ V _{PG}	√	
	EN = High, V _{FB} ≤ V _{PG}		√
Shutdown by EN	EN = Low		√
Thermal Shutdown	T _J > T _{JSD}		√
UVLO	1.4V < V _{IN} < V _{UVLO}		√
Power Supply Removal	V _{IN} ≤ 1.4V	√	

DETAILED DESCRIPTION (continued)

Soft Startup and Pre-biased Output

An 800 μ s internal soft-start circuit is designed to prevent input inrush current and voltage drops during startup. This circuit slowly ramps up the error amplifier reference voltage ($V_{REF} = 0.6V$) after exiting the shutdown state or under-voltage lockout (UVLO). Slow increase of the output voltage prevents the excessive inrush current for charging the output capacitors and creates a smooth output voltage rise. The other advantage of a soft-start is avoiding supply voltage drops especially on the high internal impedance sources such as the primary cells and rechargeable batteries.

The SGM61020 is also capable of starting with a pre-biased output capacitor when it is powering up or enabled. When the device is turning on, a bias on the output may exist due to the other sources connected to the load(s) such as multi-voltage ICs or simply because of residual charges on the output capacitors. For example, when a device with light load is disabled and re-enabled, the output may not drop during the off period and the device must restart under pre-biased output condition. Without the pre-biased capability, the device may not be able to startup properly. The output ramp is automatically initiated with the bias voltage and ramps up to the nominal output value.

Power-Save Mode (PSM)

At light load condition, the SGM61020 shifts to the PSM mode and operates with pulse skip modulation to reduce the switching frequency and minimize the losses. It also shuts down most of the internal circuits in PSM. In this mode, one or more PWM pulses are sent to charge the output capacitor and then the switches are kept off. The output capacitor voltage gradually drops due to small load current and when it falls below the nominal voltage threshold, the PWM pulses resume.

If the load is still low, the output will go slightly higher than normal again and the switches will be turned off. In power-save mode, the output voltage is slightly higher than nominal output voltage. This effect can be mitigated by a larger output capacitor.

Low Dropout Operation (100% Duty Cycle)

When the input voltage reduces, the on-time increases. When the input voltage is lower than the regulation output voltage, the output voltage drops, and the SGM61020 goes into 100% duty cycle mode. The high-side switch is always turned on, and the output voltage is determined by the load current times the $R_{DS(on)}$ composed by the high-side switch and inductor.

Current Limit Protection

Limiting the switch current protects the switch itself and also prevents over-current in the source and the inductor. If the high-side (HS) switch current exceeds the I_{LIM} threshold, HS switch is turned off and the low-side (LS) switch will be turned on to reduce the inductor current and limit the peak.

Note that the measured peak current limit in the closed-loop and open-loop (I_{LIM_OL}) test conditions is slightly different, mainly due to the current comparator propagation delay.

Thermal Shutdown

A thermal shutdown function is implemented to prevent damage caused by excessive heat and power dissipation. Once the junction temperature exceeds +150°C, the device is shut down. The device is released from shutdown automatically when the junction temperature decreases by 20°C.

APPLICATION INFORMATION

In this section, power supply design with the SGM61020 synchronous Buck converter and selection of the external component will be explained based on the typical application that is applicable for various input and output voltage combinations.

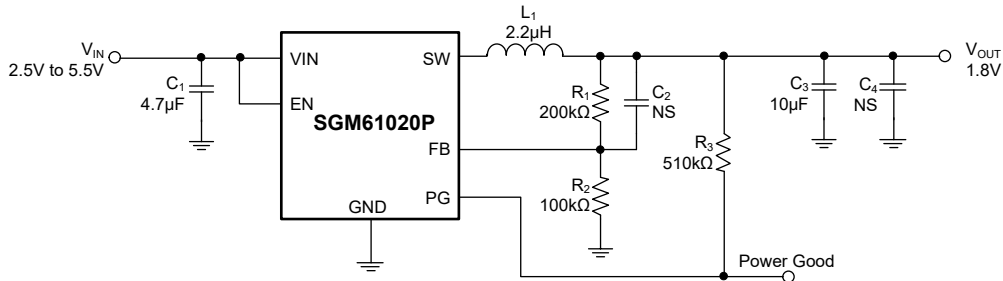


Figure 3. SGM61020P Application Example with 1.8V/2A Output

Design Requirements

Table 2 summarizes the requirements for this example as shown in Figure 3. The selected components are given in Table 3.

Table 2. Design Parameters for the Application Example

Design Parameter	Example Value
Input Voltage	2.5V to 5.5V
Output Voltage	1.8V
Output Current	≤ 2A
Output Ripple Voltage	< 30mV

Table 3. Selected Components for the Design Example

Ref	Description	Manufacturer
C ₁	4.7µF, 10V, X7R, 0805, Ceramic P/N: GRM21BR71A475ME51L	Murata
C ₂ , C ₄	NS	Standard
C ₃	10µF, 10V, X7R, 0805, Ceramic P/N: GRM21BR71A106KA73L	Murata
L ₁	2.2µH Wire Wound, DCR _{MAX} = 39mΩ, I _{SAT(30%)} = 4.9A, I _{RMS(40°C)} = 3A, 4mm × 4mm × 3mm, P/N: SWPA4030S2R2NT	Sunlord
R ₁	Value Depends on V _{OUT} , 200kΩ, 1%, 0603, 1/16W Chip Resistor	Standard
R ₂	100kΩ, 1%, 0603, 1/16W Chip Resistor	Standard
R ₃	510kΩ, 5%, 0603, 1/16W Chip Resistor	Standard

Input Capacitor Selection (C_{IN})

High frequency decoupling input capacitors with low ESR are needed to circulate and absorb the high frequency switching currents of the converter. Place this capacitor right beside the VIN and GND pins. A 4.7µF ceramic capacitor with X5R or better dielectric and 0805 or smaller size is sufficient in most cases. A

larger value can be selected to reduce the input current ripple.

Inductor Selection

The important factors for inductor selection are inductance (L₁), saturation current (I_{SAT}), RMS rating (I_{RMS}), DC resistance (DCR) and dimensions. Use Equations 1 and 2 to find the inductor peak current (I_{L_MAX}) and peak-to-peak ripple current (ΔI_L) in static conditions:

$$I_{L_MAX} = I_{O_MAX} + \frac{\Delta I_L}{2} \tag{1}$$

$$\Delta I_L = V_{OUT} \times \frac{1-D}{L \times f_{SW}} \tag{2}$$

where:

I_{O_MAX} is the maximum load current, D = V_{OUT}/V_{IN} represents duty cycle and f_{SW} is the switching frequency.

I_{SAT} should be higher than I_{L_MAX}, and sufficient margin should be reserved. Typically, the saturation current above high-side current limit is enough, and a 10% to 30% ripple current is selected to calculate the inductance. Larger inductance values reduce the ripple current but lead to sluggish transient response.

Output Voltage Setting

Use Equation 3 to select the R₁/R₂ resistor divider to set the V_{OUT}. Select the R₂ value less than 100kΩ to compromise noise sensitivity and light load losses.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \tag{3}$$

APPLICATION INFORMATION (continued)

Output Capacitor Selection (C_{OUT})

This device is capable to operate with low ESR ceramic capacitors to get low voltage ripple and fast response. $10\mu\text{F} \sim 22\mu\text{F} \times 2$ capacitors with X7R or X5R dielectric type are recommended. Minimum capacitance of output ripple criteria can be calculated from Equation 4.

$$C_{OUT} > \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT_RIPPLE}} \quad (4)$$

For output capacitor selection, transient response and loop stability should also be considered. To simplify customer's design process, the inductor and output capacitor combinations are recommended in Table 4.

Table 4. Proper Output Capacitor and Inductor Combination

V_{OUT}	L_1	C_{OUT}
0.9V	1 μH	22 μF
		22 $\mu\text{F} \times 2$
	2.2 μH	22 μF
		22 $\mu\text{F} \times 2$
1.8V	1 μH	10 μF
		22 μF
		22 $\mu\text{F} \times 2$
	2.2 μH	10 μF
		22 μF
		22 $\mu\text{F} \times 2$
3.3V	2.2 μH	10 μF
		22 μF
		22 $\mu\text{F} \times 2$

Output Filter Design

Table 4 can be used to select the proper LC filter components for most design requirements. The inductor initial tolerance can be as high as -30% to +20% of the nominal value and proper current derating is usually required. Bias voltage may cause significant capacitance drops in the ceramic capacitors. The effective deviation of a ceramic capacitor can be as high as -50% to +20% of the nominal value.

$L_1 = 2.2\mu\text{H}$, $C_{OUT} = 10\mu\text{F}$ are the recommended values for the typical application.

Layout Guidelines

A good printed-circuit-board (PCB) layout is a critical element of any high performance design. Follow the guidelines below for designing a good layout for the SGM61020.

- Place the input capacitor close to the device with the shortest possible connection traces.
- Share the same GND return point for the input and output capacitors and locate it as close as possible to the device GND pin to minimize the AC current loops. Place the inductor close to the switching node and connect it with a short trace to minimize the parasitic capacitances coupled to the SW node.
- Keep the signal traces like the FB sense line away from SW or other noisy sources.
- Use GND planes in mid-layers for shielding and minimizing the ground potential drifts.

Refer to Figure 4 and Figure 5 for a recommended PCB layout.

APPLICATION INFORMATION (continued)

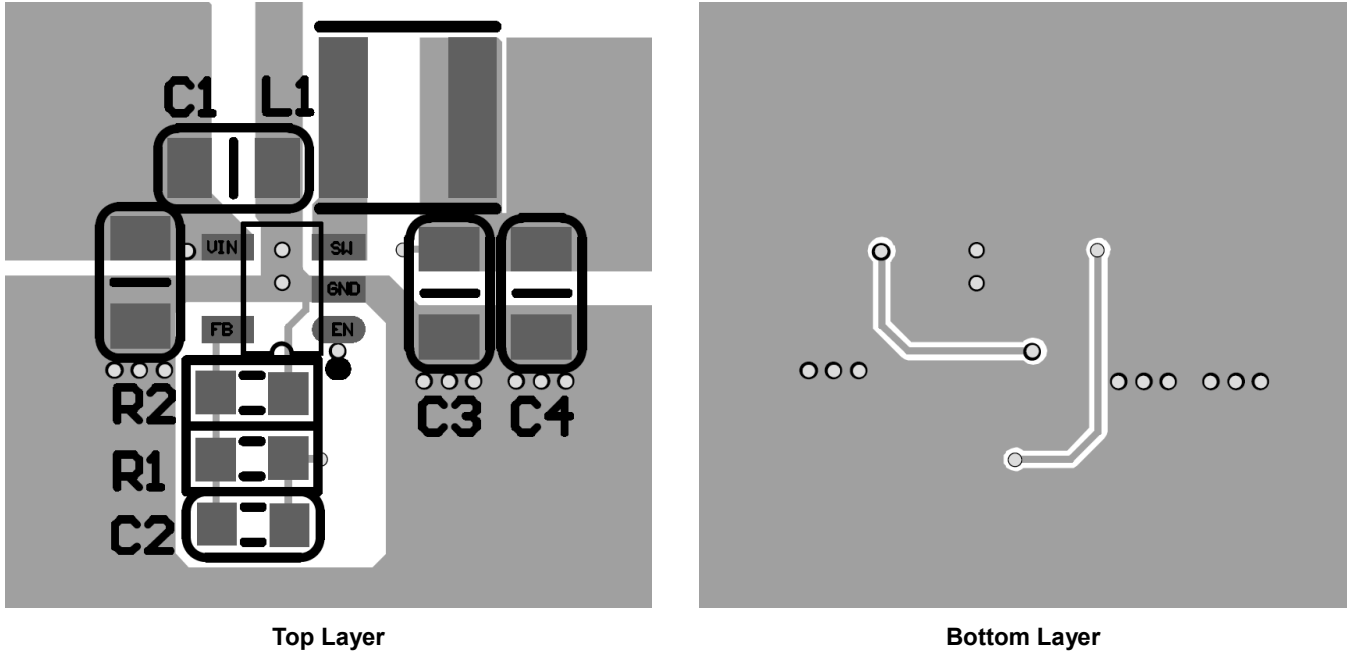


Figure 4. SOT-23-5 PCB layout

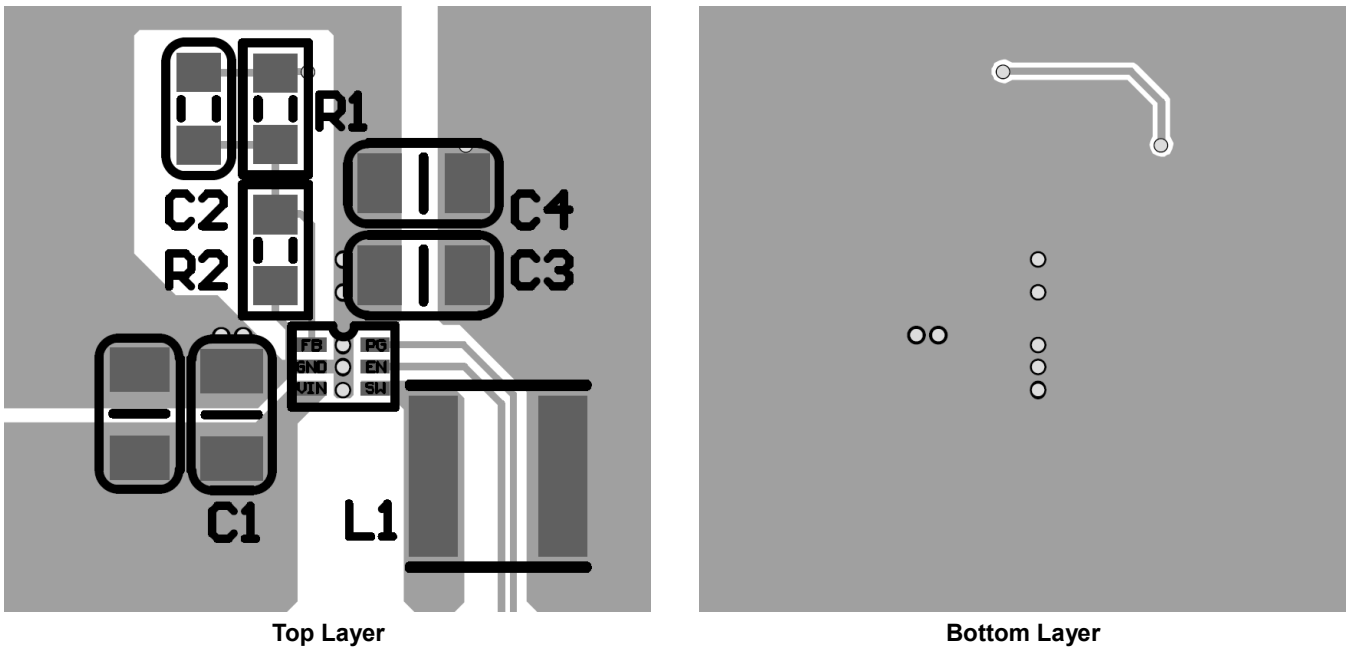


Figure 5. SOT-563-6 PCB layout

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

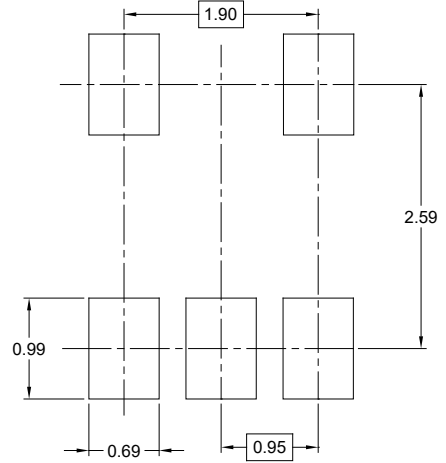
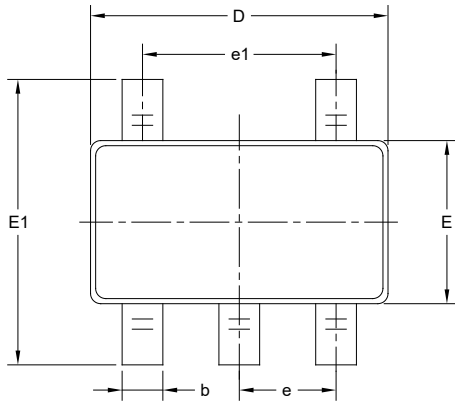
Changes from REV.A (AUGUST 2022) to REV.A.1	Page
Updated Electrical Characteristics	4

Changes from Original (MARCH 2022) to REV.A	Page
Changed from product preview to production data.....	All

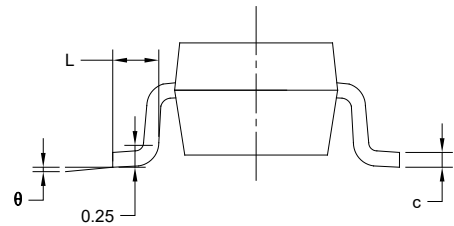
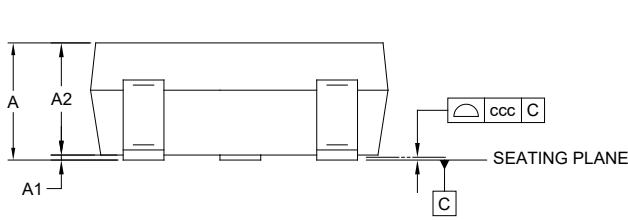
PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

SOT-23-5



RECOMMENDED LAND PATTERN (Unit: mm)



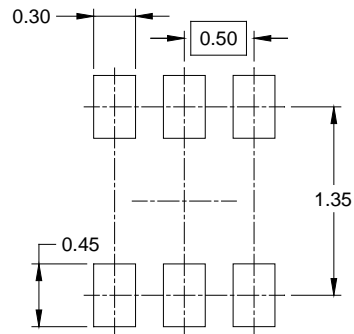
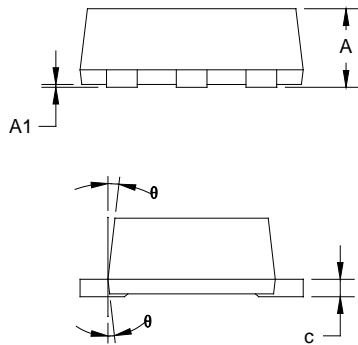
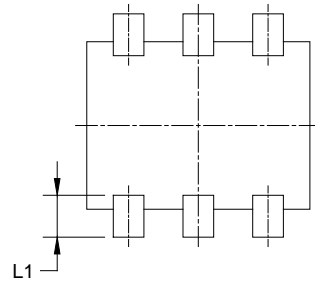
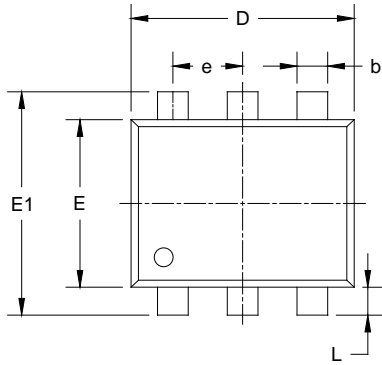
Symbol	Dimensions In Millimeters		
	MIN	MOD	MAX
A	-	-	1.450
A1	0.000	-	0.150
A2	0.900	-	1.300
b	0.300	-	0.500
c	0.080	-	0.220
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.600	-	3.000
e	0.950 BSC		
e1	1.900 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

NOTES:

1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-178.

PACKAGE OUTLINE DIMENSIONS

SOT-563-6



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
b	0.170	0.270	0.007	0.011
c	0.090	0.180	0.004	0.007
D	1.500	1.700	0.059	0.067
E	1.100	1.300	0.043	0.051
E1	1.500	1.700	0.059	0.067
e	0.450	0.550	0.018	0.022
L	0.100	0.300	0.004	0.012
L1	0.200	0.400	0.008	0.016
θ	9° REF		9° REF	

NOTES:

1. Body dimensions do not include mode flash or protrusion.
2. This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT-23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
SOT-563-6	7"	9.5	1.78	1.78	0.69	4.0	4.0	2.0	8.0	Q3

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PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7" (Option)	368	227	224	8
7"	442	410	224	18

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