

## Features

- ❑ Transient protection for high-speed data lines  
IEC 61000-4-2 (ESD) ±16kV (Air)  
±8kV (Contact)  
Cable Discharge Event (CDE)
- ❑ Package optimized for high-speed lines
- ❑ Ultra-small package (2.5mm×1.0mm×0.55mm)
- ❑ Protects four data lines
- ❑ Low capacitance: 0.65pF(Typical)
- ❑ Low leakage current: 0.1µA @ VRWM(Maximum)
- ❑ Low clamping voltage
- ❑ Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge
- ❑ ROHS compliant

## Description

TT0334TPX is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With Typical capacitance 0.65pF only, TT 0334 TP X is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4 (±15kV air, ±8kV contact discharge), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

TT0334TPX uses ultra-small DFN-10L package.

TT0334TPX Each device can protect four high-speed data lines. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make TT0334TPX ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the TT0334TPX guarantees a minimum stress on the protected IC.

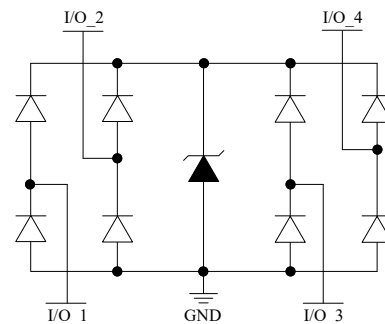
## Applications

- ❑ Serial ATA
- ❑ PCI Express
- ❑ Desktops, Servers and Notebooks
- ❑ MDDI Ports
- ❑ USB 2.0/3.0/3.1 Power and Data Line Protection
- ❑ Display Ports
- ❑ High Definition Multi-Media Interface (HDMI)
- ❑ Digital Visual Interfaces (DVI)

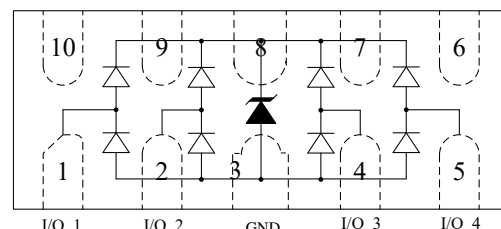
## Mechanical Characteristics

- ❑ DFN-10L package
- ❑ Flammability Rating: UL 94V-0
- ❑ Marking: Part number
- ❑ Packaging: Tape and Reel

## Circuit Diagram



## Pin Configuration



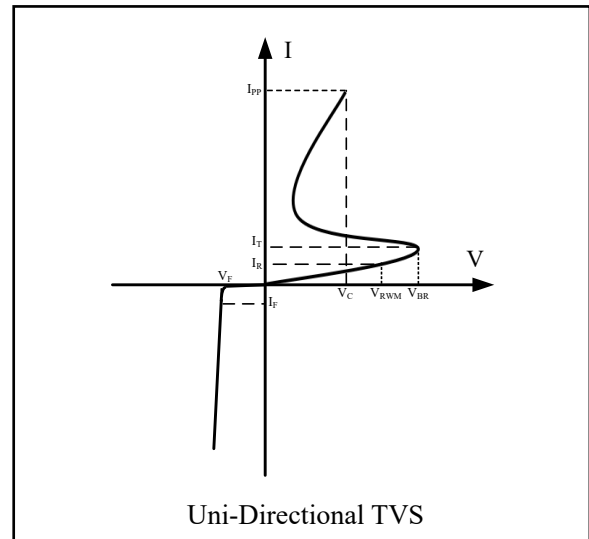
DFN-10L  
(Top View)

### Absolute Maximum Rating

Symbol	Parameter	Value	Units
$I_{PP}$	Peak Pulse Current( $t_p=8/20\mu s$ )	5.0	A
$V_{ESD}$	ESD per IEC 61000-4-2(Air) ESD per IEC 61000-4-2 (Contact)	$\pm 16$ $\pm 8$	kV
$T_{OPT}$	Operating Temperature	-55/+125	°C
$T_{STG}$	Storage Temperature	-55/+150	°C

### Electrical Characteristics (T = 25°C)

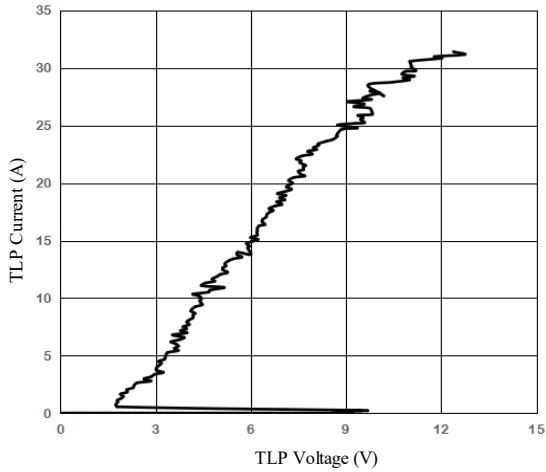
Symbol	Parameter
$V_{RWM}$	Nominal Reverse Working Voltage
$I_R$	Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Reverse Breakdown Voltage @ $I_T$
$I_T$	Test Current for Reverse Breakdown
$V_C$	Clamping Voltage @ $I_{PP}$
$I_{PP}$	Maximum Peak Pulse Current
$C_{ESD}$	Parasitic Capacitance
$V_R$	Reverse Voltage
f	Small Signal Frequency
$I_F$	Forward Current
$V_F$	Forward Voltage @ $I_F$



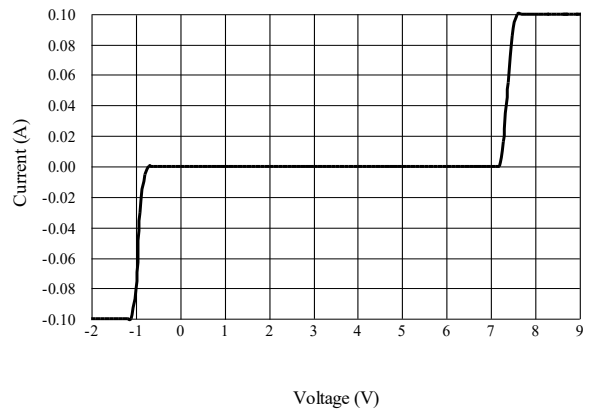
Symbol	Test Condition	Minimum	Typical	Maximum	Units
$V_{RWM}$				3.3	V
$I_R$	$V_{RWM} = 3.3V, T = 25^\circ C$		0.01	0.1	$\mu A$
$V_{BR}$	$I_T = 1mA$	5.5	7.5		V
$V_C$	$I_{PP} = 5.0A, t_p = 8/20\mu s$		3.0	6.0	V
$V_C$	$I_{PP} = 8.0A, t_p = 100ns^{(1)}$		4.0		V
	$I_{PP} = 16.0A, t_p = 100ns^{(1)}$		8.0		V
$R_{dyn}$	$I_{PP} = 34A, t_p = 322\mu s^{(1)}$		0.47		$\Omega$
$C_{ESD}$	$V_R = 0V, f = 1MHz$ Between I/O and GND		0.65		pF
$C_{ESD}$	$V_R = 0V, f = 1MHz$ Between I/O and I/O		0.3		pF

Notes: (1) Measurements performed using a 100ns Transmission Line Pulse (TLP) system.

**TLP Measurement of I/O to GND**

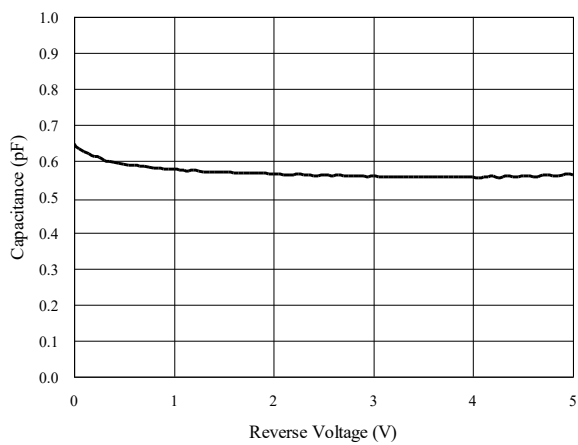


**Voltage Sweeping of I/O to GND**

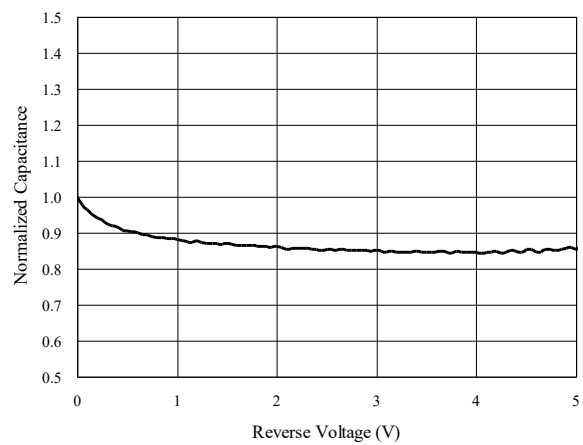


**Capacitance vs. Voltage of I/O to GND (f = 1MHz)**

Capacitance vs. Reverse Voltage



Normalized Capacitance vs. Reverse Voltage



## Application Information

### Pin Connection in PCB

TT0334TPX provides ESD protection for four data lines simultaneously. The pin connection is shown in the figure below.

Four parallel data lines, from inner IC to I/O port connector, could connect to TT0334TPX four I/O pins directly. Pin 3&8 of TT0334TPX is the GND pin, which should connect to the GND of PCB. The wire should be as short as possible in order to minimize the parasitic inductance.

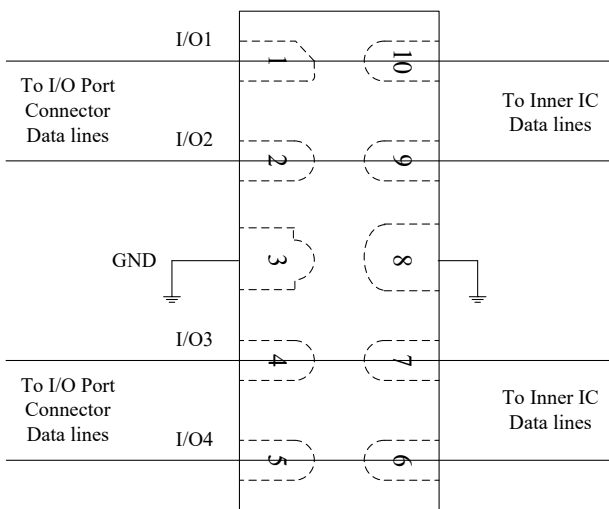


Figure 1 TT0334TPX pin connection in PCB

### PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- ❑ TT0334TPX GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- ❑ The vias connecting TT0334TPX GND pins to the PCB GND should be wide.
- ❑ Place TT0334TPX as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- ❑ Avoid running critical signals near board edges.

**Application Information**

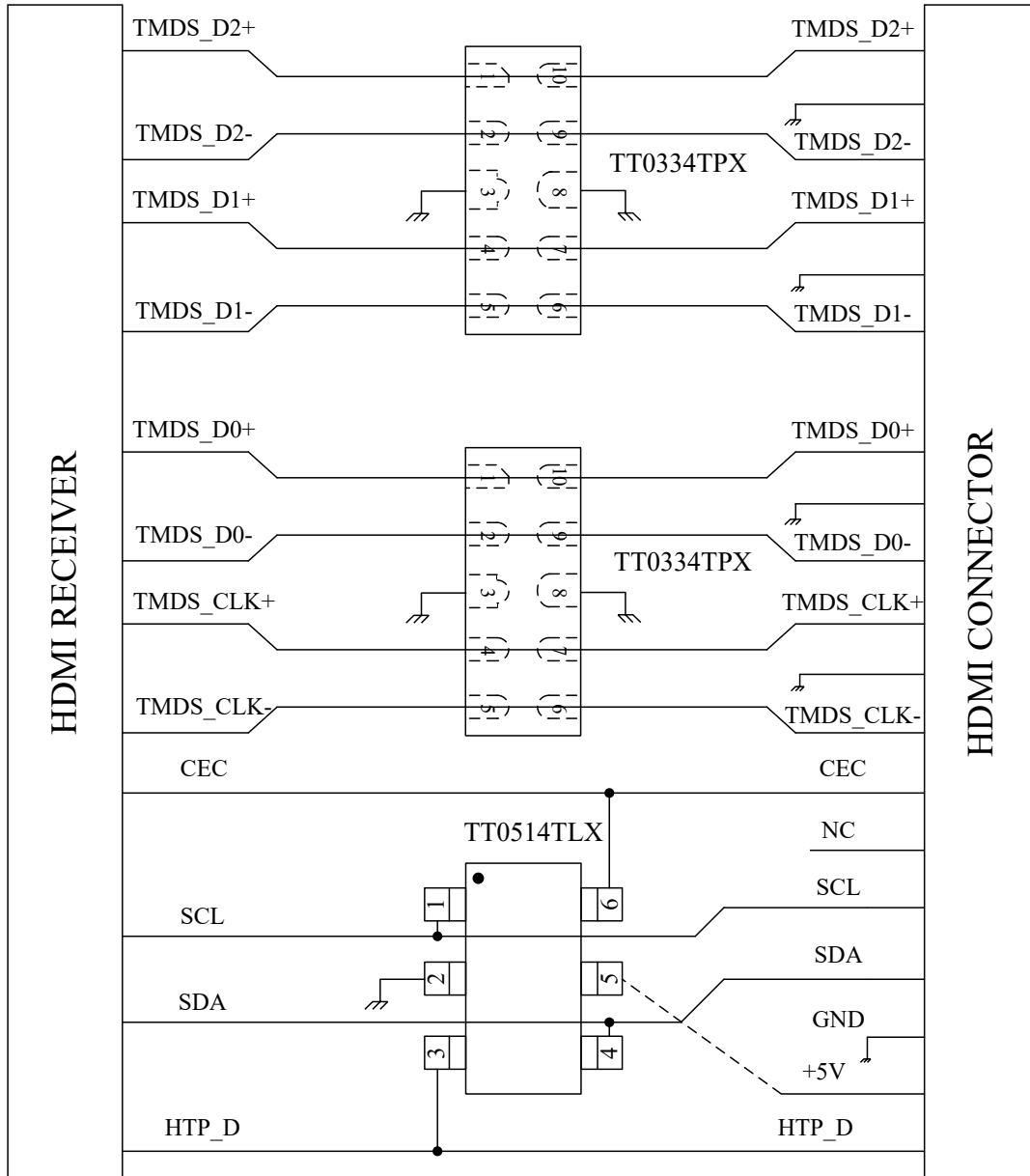
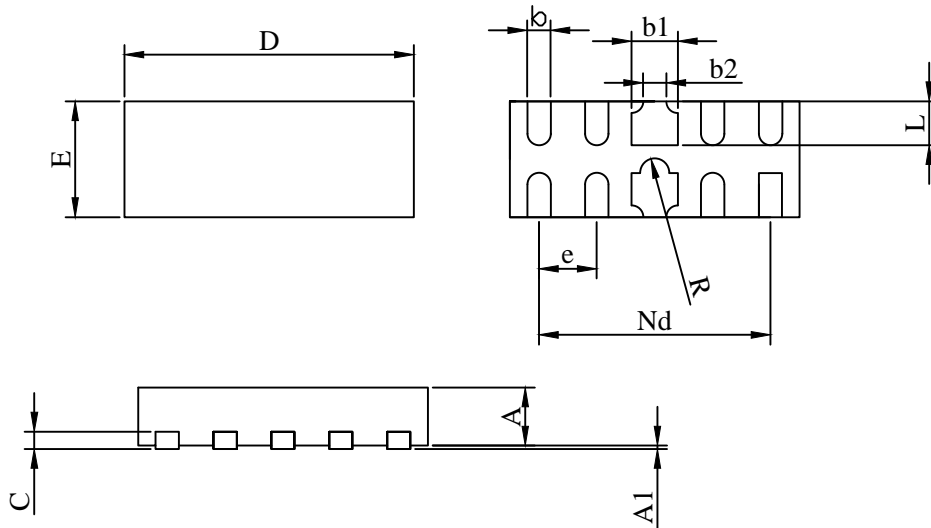


Figure 2 Layout Top View for HDMI Interface with TT0334TPX & TT0514TLX

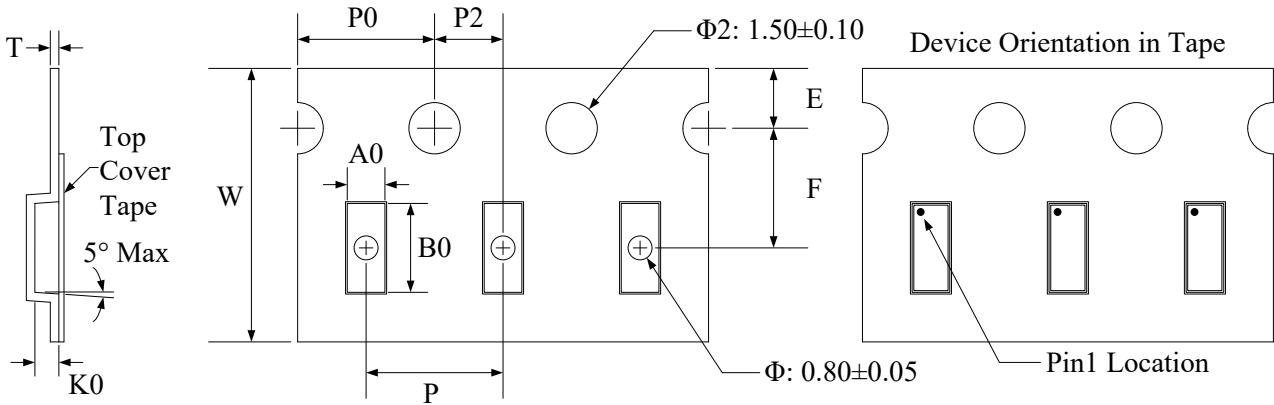
**Package Outline**

- DFN-10L package
- Thermally-Enhanced
- MSL-1 Level



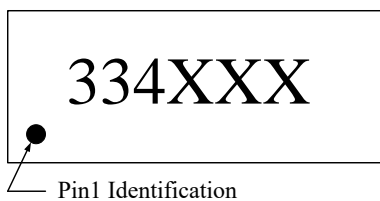
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
L			
D	2.45	2.50	2.55
E	0.95	1.00	1.05
b1	0.35	0.40	0.45
b2	0.20REF		
b	0.15	0.20	0.25
L	0.33	0.38	0.43
Nd	2.00REF		
e	0.50REF		
R	0.10	0.125	0.15
A	0.45	0.50	0.55
c	0.15REF		
A1	0.00	-	0.05

### Tape and Reel Specification

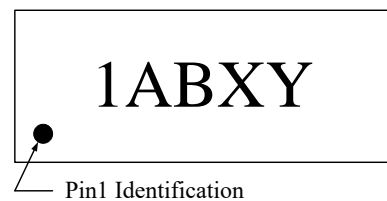


Symbol	W	A0	B0	K0	E	F	P	P0	P2	T
Dimensions (mm)	8.00+0.3 -0.1	1.23±0.05	2.7±0.05	0.7±0.05	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1	2.0±0.05	0.25±0.02

### Marking Codes



Or



**Note:**

- (1) "334" is part number, fixed.
- (2) "XXX" is the last 3 characters of the wafer's Lot No.

**Note:**

- (1) "1" is part number, fixed.
- (2) "AB" is the wafer's Lot No. "XY" is internal code

### Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
TT0334TPX	3.3V	3,000	7 Inch

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