

Features

- ❑ Transient protection for high-speed data lines
 - IEC 61000-4-2 (ESD) ±25kV (Air)
 - ±17kV (Contact)
 - IEC 61000-4-4 (EFT) 40A (5/50 ns)
 - Cable Discharge Event (CDE)
- ❑ Small package (2.9mm × 2.8mm × 1.4mm)
- ❑ Protects four data lines
- ❑ Low capacitance: 0.5pF Typical (I/O-GND)
- ❑ Low leakage current: 0.1µA @ V_{RWM} (Typical)
- ❑ Low clamping voltage
- ❑ Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge
- ❑ Green Part ❑
RoHS Compliant

Description

TT0534TLX is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for high-speed data interfaces. With typical capacitance of 0.5pF only, TT0534TLX is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level X (±25kV air, ±17kV contact discharge), IEC 61000-4-4 (electrical fast transient - EFT) (40A, 5/50 ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc.

TT0534TLX uses small SOT23-6L package. TT0534TLX device can protect four high-speed data lines. The combined features of low capacitance, small size and high ESD robustness make TT0534TLX ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the TT0534TLX guarantees a minimum stress on the protected IC.

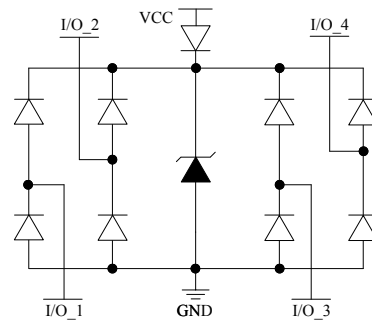
Applications

- ❑ Serial ATA
- ❑ PCI Express
- ❑ Desktops, Servers and Notebooks
- ❑ MDDI Ports
- ❑ USB 2.0/3.0 Power and Data Line Protection
- ❑ Display Ports
- ❑ High Definition Multi-Media Interface (HDMI)
- ❑ Digital Visual Interfaces (DVI)

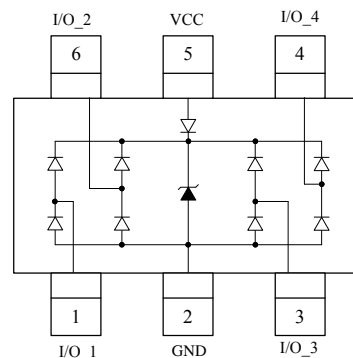
Mechanical Characteristics

- ❑ SOT23-6L package
- ❑ Flammability Rating: UL 94V-0
- ❑ Marking: Part number
- ❑ Packaging: Tape and Reel

Circuit Diagram



Pin Configuration



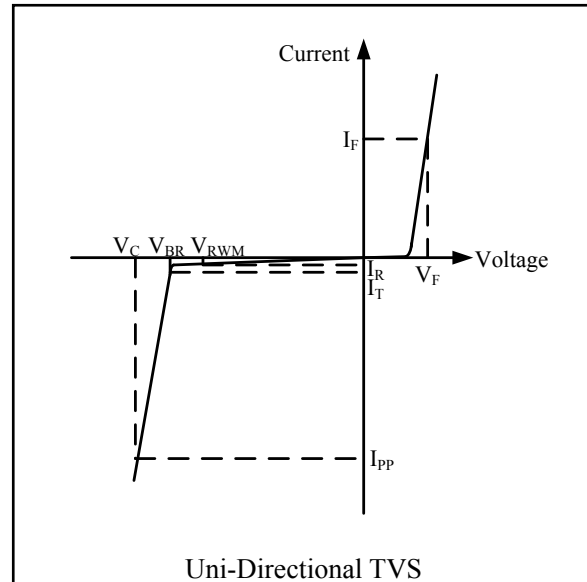
SOT23-6L
(Top View)

Absolute Maximum Rating

Symbol	Parameter	Value	Units
P_{PP}	Peak Pulse Power (8/20 μ s) (I/O pins)	60	W
I_{PP}	Peak Pulse Current($t_p=8/20\mu s$) (I/O pins)	4.5	A
V_{ESD}	ESD per IEC 61000-4-2(Air) ESD per IEC 61000-4-2 (Contact)	± 25 ± 17	kV
T_{OPT}	Operating Temperature	-55/+125	$^{\circ}C$
T_{STG}	Storage Temperature	-55/+150	$^{\circ}C$

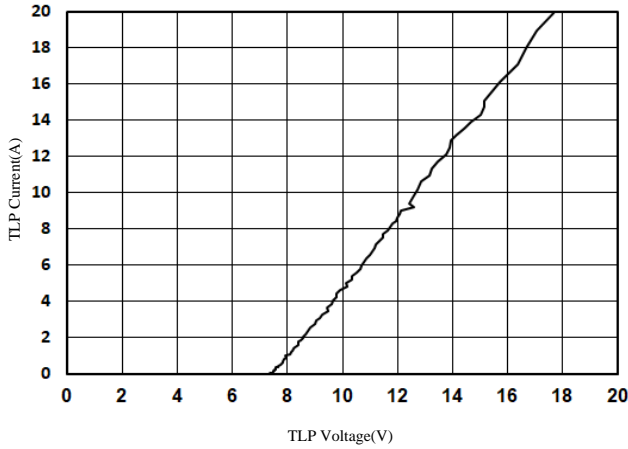
Electrical Characteristics (T = 25 $^{\circ}C$)

Symbol	Parameter
V_{RWM}	Nominal Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Reverse Breakdown Voltage @ I_T
I_T	Test Current for Reverse Breakdown
V_C	Clamping Voltage @ I_{PP}
I_{PP}	Maximum Peak Pulse Current
C_{ESD}	Parasitic Capacitance
V_R	Reverse Voltage
f	Small Signal Frequency
I_F	Forward Current
V_F	Forward Voltage @ I_F

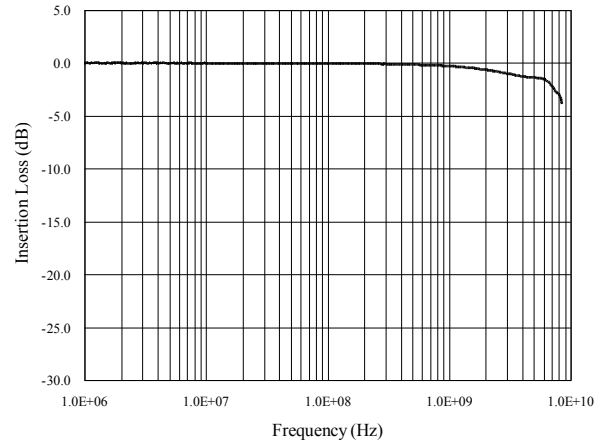


Symbol	Test Condition	Minimum	Typical	Maximum	Units
V_{RWM}				5.0	V
I_R	$V_{RWM} = 5V, T = 25^{\circ}C$ Between I/O and GND		0.1	1.0	μA
V_{BR}	$I_T = 1mA$ Between I/O and GND	6.0	8.0	10.0	V
V_C	$I_{PP} = 1A, t_p = 8/20\mu s$ Between I/O and GND			12	V
C_{ESD}	$V_R = 0V, f = 1MHz$ Between I/O and GND		0.5	0.6	pF
C_{ESD}	$V_R = 0V, f = 1MHz$ Between I/O and I/O		0.25	0.3	pF

TLP Measurement of I/O to GND

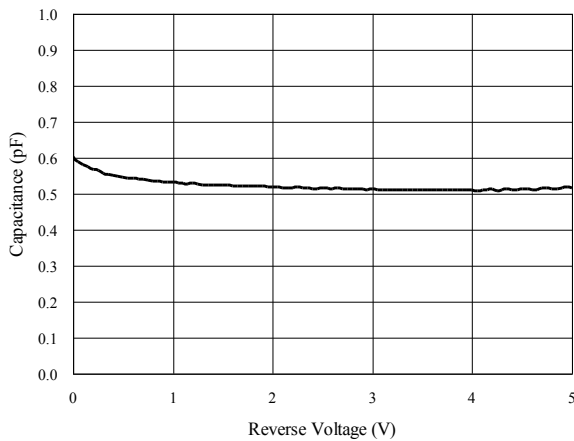


Insertion Loss S21 of I/O to GND

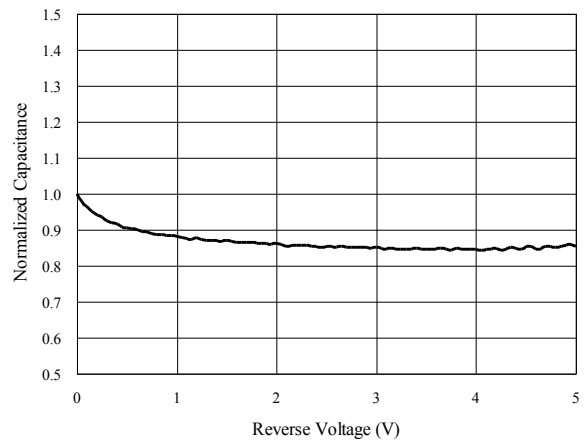


Capacitance vs. Voltage of I/O to GND (f = 1MHz)

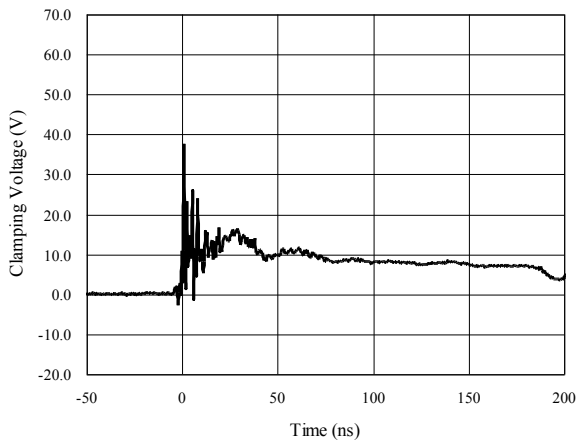
Capacitance vs. Reverse Voltage



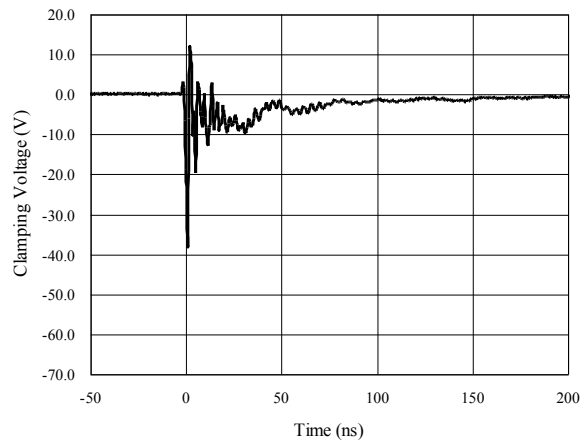
Normalized Capacitance vs. Reverse Voltage



ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



Application Information

Pin Connection in PCB

TT0534TLX is capable to provide ESD protection for four data lines simultaneously. The pin connection is shown in Figure 1.

Four parallel data lines, from inner IC to I/O port connector, could connect to TT0534TLX four I/O pins directly. Pin 2 of TT0534TLX is the negative reference pin, which should connect to the GND of PCB. The connection wires should be as short as possible in order to minimize the parasitic inductance.

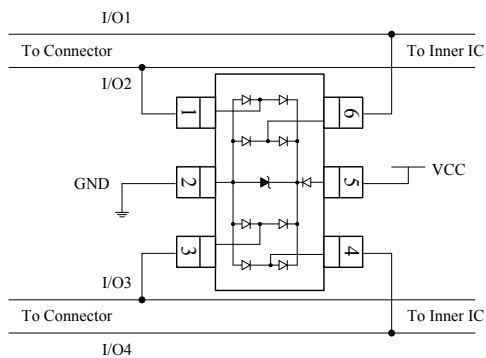


Figure 1 TT0534TLX pin connection in PCB

PCB Layout Guidelines

For optimum ESD protection and the whole circuit performance, the following PCB layout guidelines are recommended:

- ❑ TT0534TLX GND pin to the PCB GND rail path should be as short as possible. It could reduce the ESD transient return path to GND.
- ❑ The vias connecting TT0534TLX VCC&GND pins to the PCB VCC & GND should be wide.
- ❑ Place TT0534TLX as close to the connector port as possible. It could reduce the parasitic inductance and restrict ESD coupling into adjacent traces.
- ❑ Avoid running critical signals near board edges.

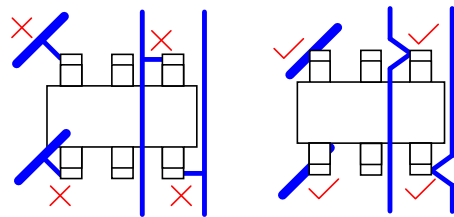
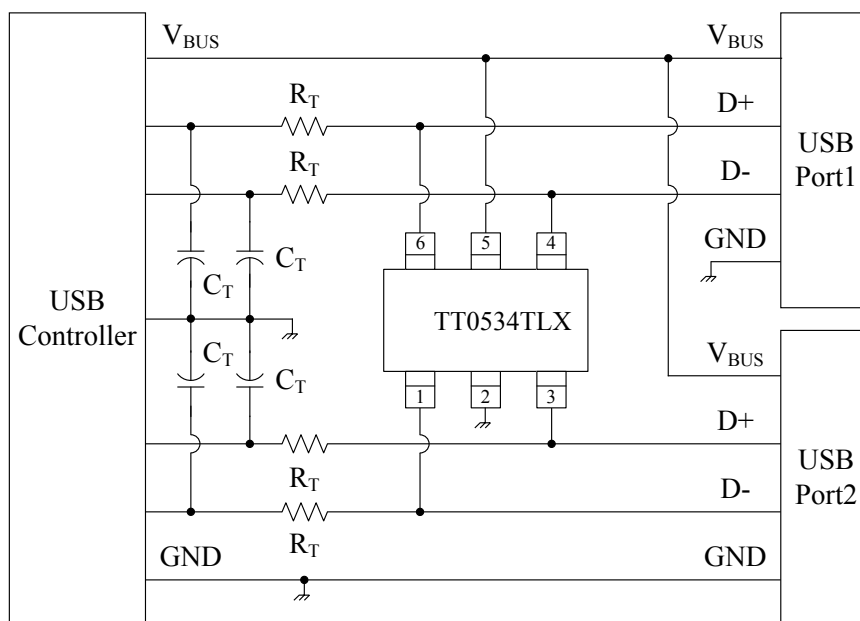
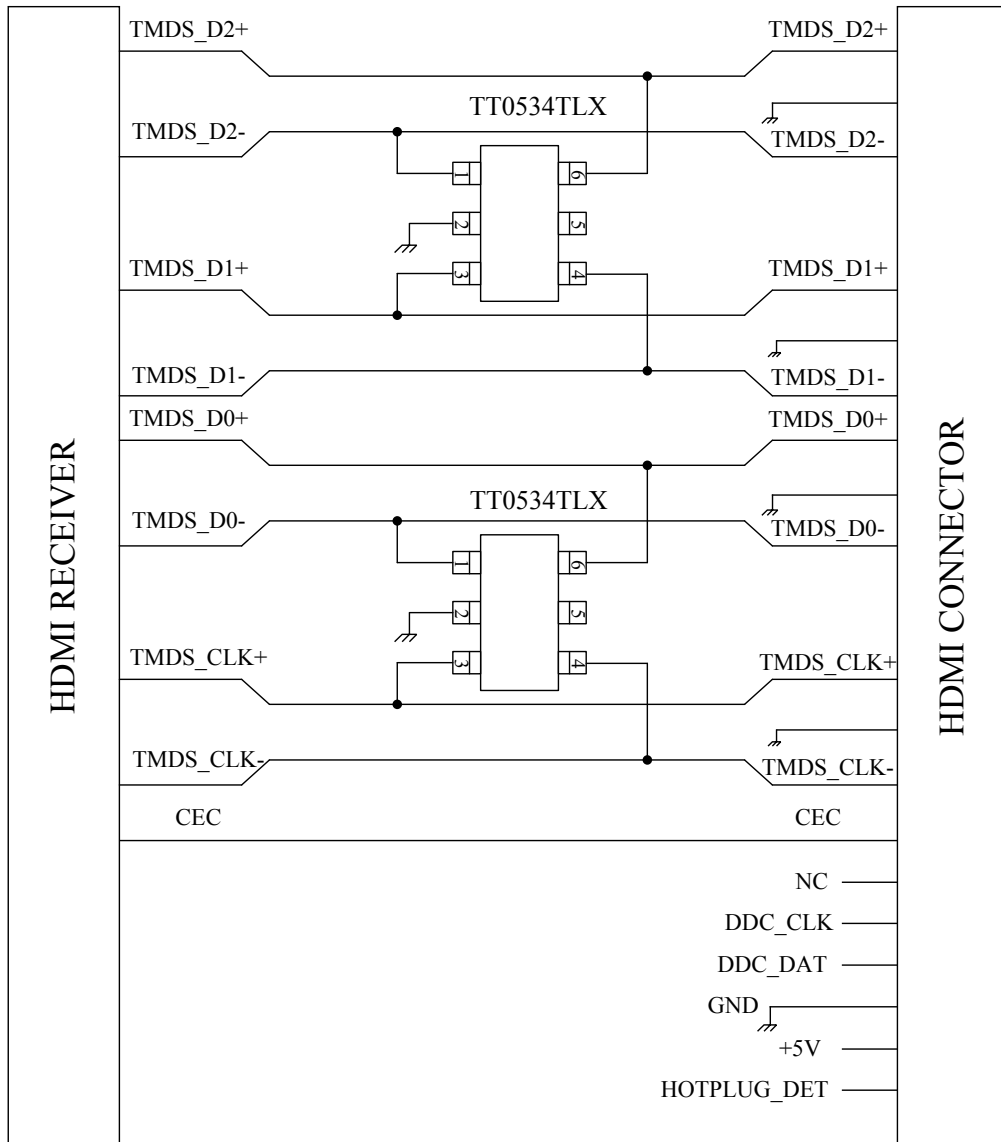


Figure 2 TT0534TLX Layout Guideline

Universal Serial Bus ESD Protection

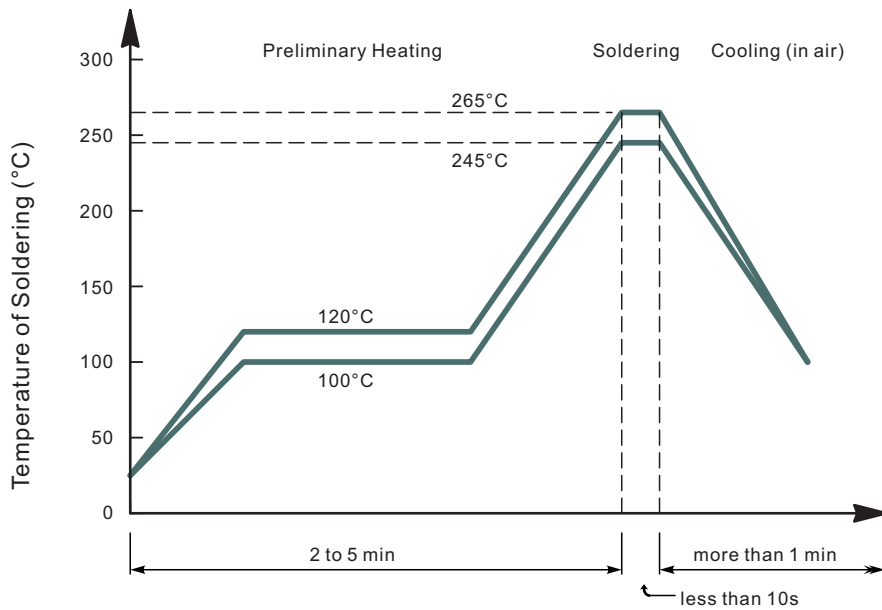


Application Information (continued)

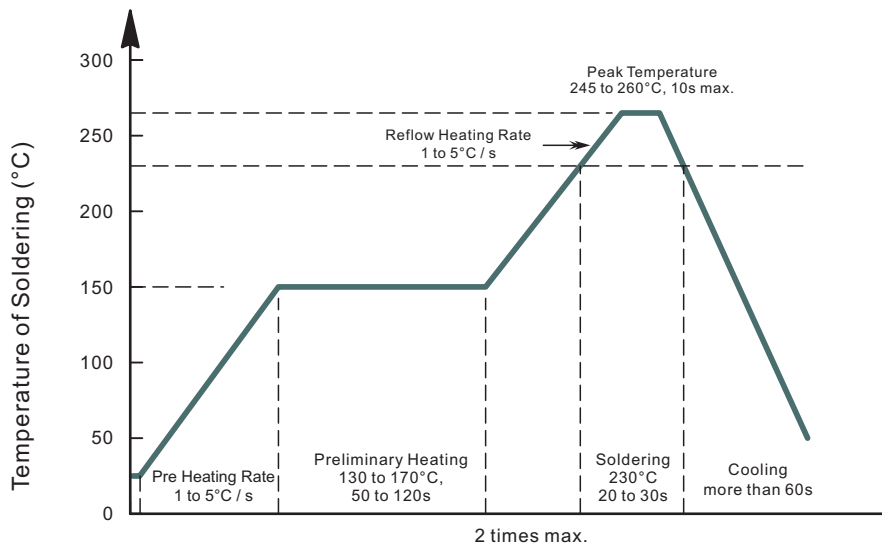


Layout Top View for HDMI Interface with TT0534TLX

• Recommended condition of flow soldering

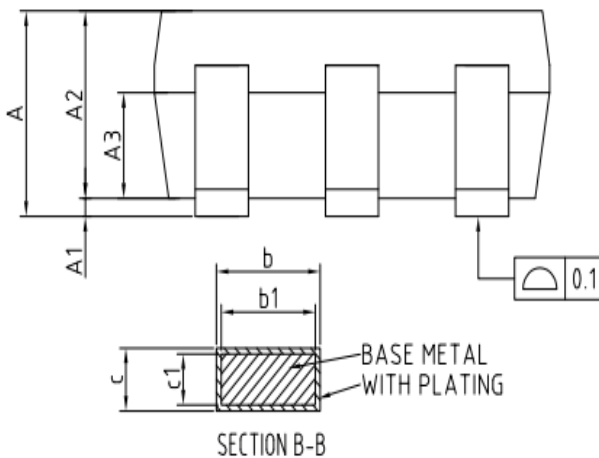
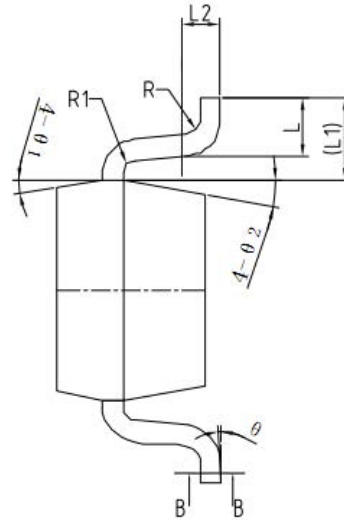
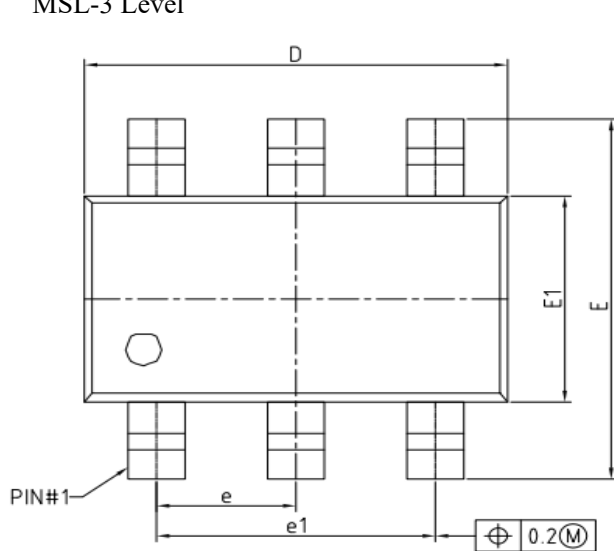


• Recommended condition of reflow soldering



Package Outline

- SOT23-6L package
- MSL-3 Level

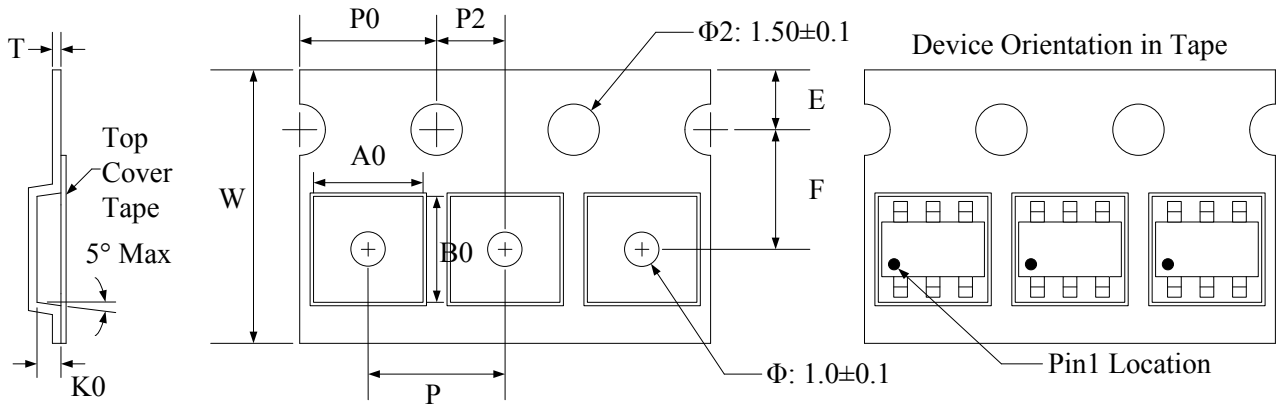


COMMON DIMENSIONS (UNITS OF MEASURE MILLIMETER)			
SYMBOL	MIN	NOM	MAX
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.6	2.8	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
R	0.10	-	-
R1	0.10	-	0.20
θ	0°	-	8°
θ 1	3°	5°	7°
θ 2	6°	-	14°

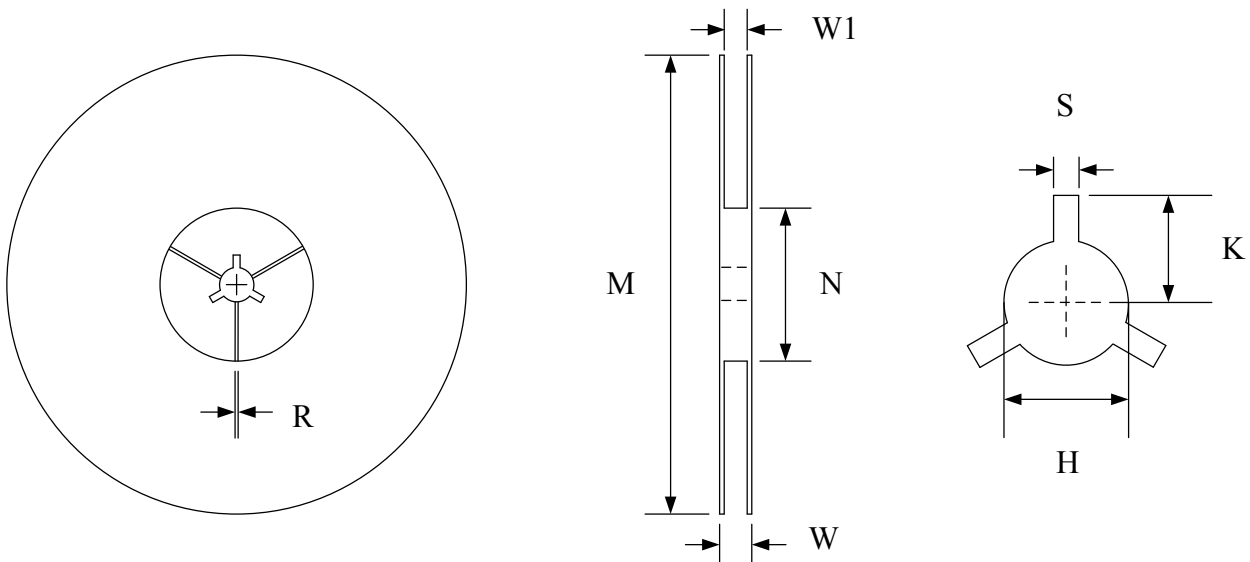
Notes:

- This dimension complies with JEDEC outline standard MO-178 Variation AB.

Tape and Reel Specification

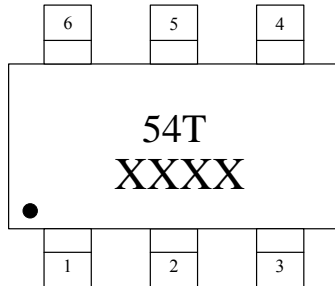


Symbol	W	A0	B0	K0	E	F	P	P0	P2	T
Dimensions (mm)	8.00+0.3 -0.1	3.23±0.05	3.17±0.05	1.37±0.05	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1	2.0±0.05	0.25±0.02



Symbol	Reel Size	M	N	W	W1	H	S	K	R
Dimensions (mm)	$\Phi 178$	178.0±1.0	60.0±1.0	11.5±0.5	9.0±0.5	13.0±0.5	2.0±0.1	11.0±0.2	1.0±0.05

Marking Codes



Note:

- (1) “54T” is part number, fixed.
- (2) “XXXX” is internal code.

Ordering Information

Part Number	Working Voltage	Quantity Per Reel	Reel Size
TT0534TLX	5V	3,000	7 Inch

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