

# P72LF7R5SL

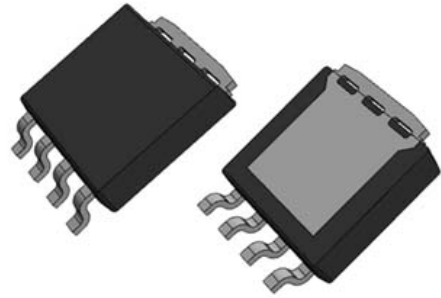
**Power MOSFETs**  
**75V, 72A, N-channel**

**Feature**

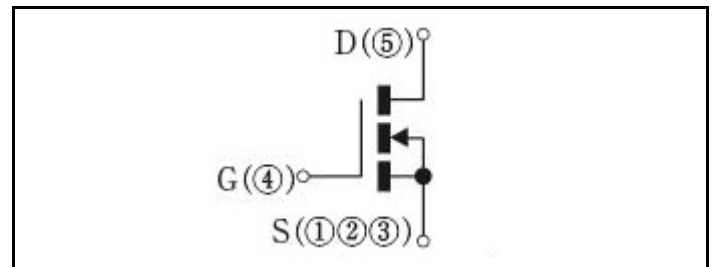
- N-channel
- Small SMD
- Large Current
- Low Ron
- 4.5V Gate Drive
- Low Capacitance
- Halogen free
- Pb free terminal
- RoHS:Yes

**OUTLINE**

**Package (House Name):** LF  
**Package (JEDEC Code):** MO-235B similar



**Equivalent circuit**



**Absolute Maximum Ratings** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	°C
Channel temperature	Tch		-55 to 175	°C
Drain-source voltage	V <sub>DSS</sub>		75	V
Gate-source voltage	V <sub>GSS</sub>		±20	V
Continuous drain current(DC)	I <sub>D</sub>		72	A
Continuous drain current(Peak)	I <sub>DP</sub>	Pulse width 10µs, duty=1/100	288	A
Total power dissipation	P <sub>T</sub>		217	W
Single avalanche current	I <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	43	A
Single avalanche energy	E <sub>AS</sub>	Starting T <sub>ch</sub> =25°C T <sub>ch</sub> ≤150°C	215	mJ

\* : See the original Specifications

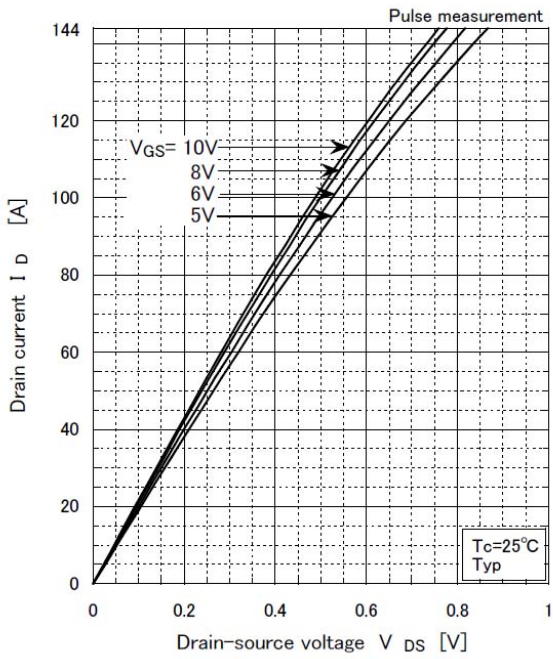
**Electrical Characteristics** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	75			V
Zero gate voltage drain current	$I_{DSS}$	VDS=75V, VGS=0V			1	μA
Gate-source leakage current	$I_{GSS}$	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	$g_{fs}$	ID=36A, VDS=10V	20			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=36A, VGS=10V		0.0046	0.0058	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=36A, VGS=4.5V		0.0055	0.0074	Ω
Gate threshold voltage	$V_{th}$	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	$V_{SD}$	IS=72A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case, with heatsink			0.69	°C/W
Total gate charge	$Q_g$	VDD=60V, VGS=10V, ID=72A		100		nC
Gate to source charge	$Q_{gs}$	VDD=60V, VGS=10V, ID=72A		18		nC
Gate to drain charge	$Q_{gd}$	VDD=60V, VGS=10V, ID=72A		31		nC
Input capacitance	$C_{iss}$	VDS=25V, VGS=0V, f=1MHz		4870		pF
Reverse transfer capacitance	$C_{rss}$	VDS=25V, VGS=0V, f=1MHz		230		pF
Output capacitance	$C_{oss}$	VDS=25V, VGS=0V, f=1MHz		439		pF
Turn-on delay time	$t_{d(on)}$	ID=36A, RL=1.04Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		6		ns
Rise time	$t_r$	ID=36A, RL=1.04Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		19		ns
Turn-off delay time	$t_{d(off)}$	ID=36A, RL=1.04Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		99		ns
Fall time	$t_f$	ID=36A, RL=1.04Ω, VDD=37.5V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		32		ns
Diode reverse recovery time	$t_{rr}$	IF=72A, VGS=0V, di/dt=100A/μs		49		ns
Diode reverse recovery charge	$Q_{rr}$	IF=72A, VGS=0V, di/dt=100A/μs		83		nC

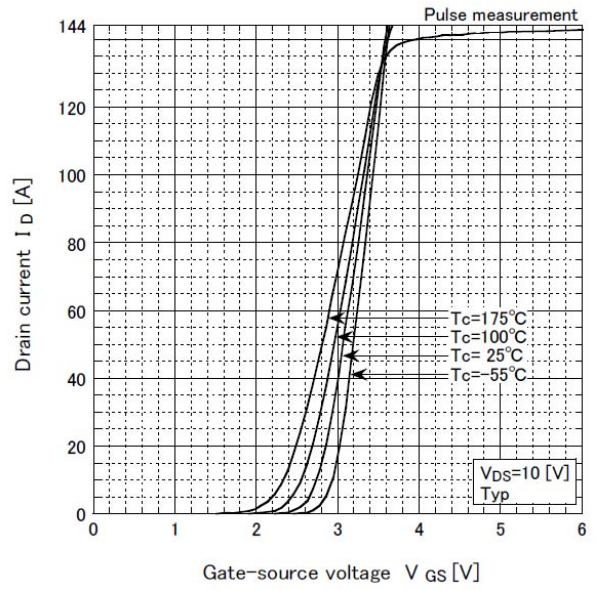
\* : See the original Specifications

# CHARACTERISTIC DIAGRAMS

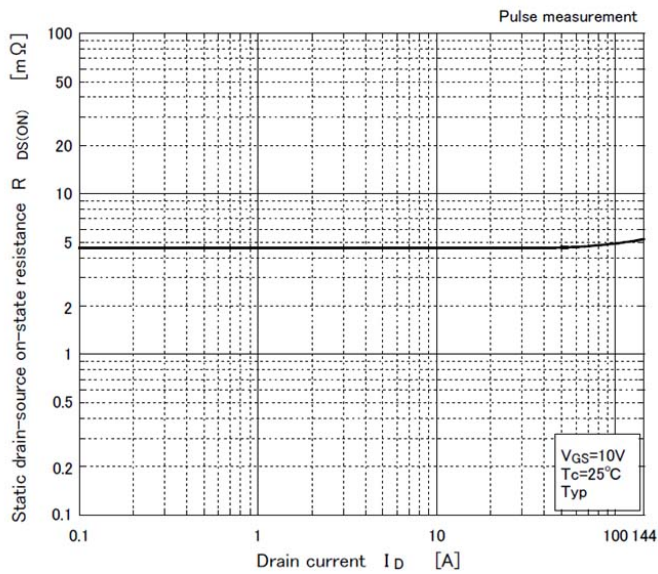
Typical output characteristics



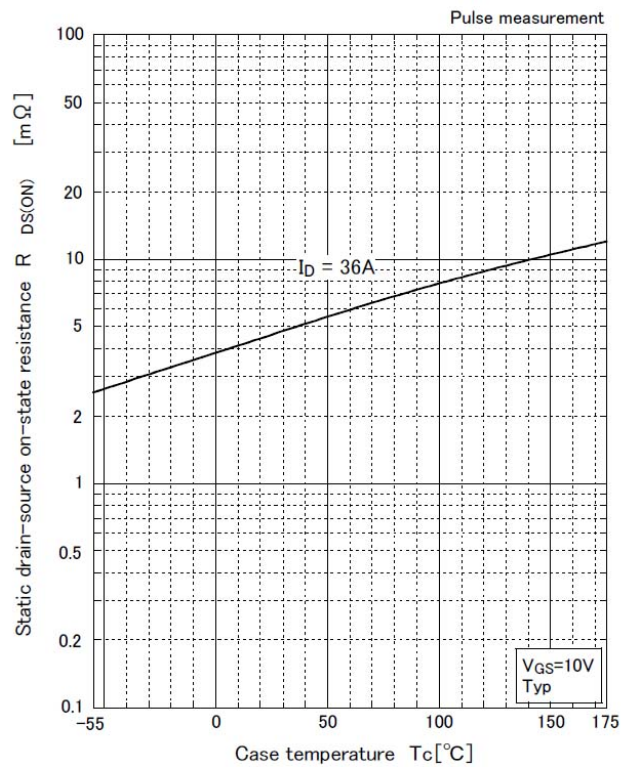
Transfer characteristics

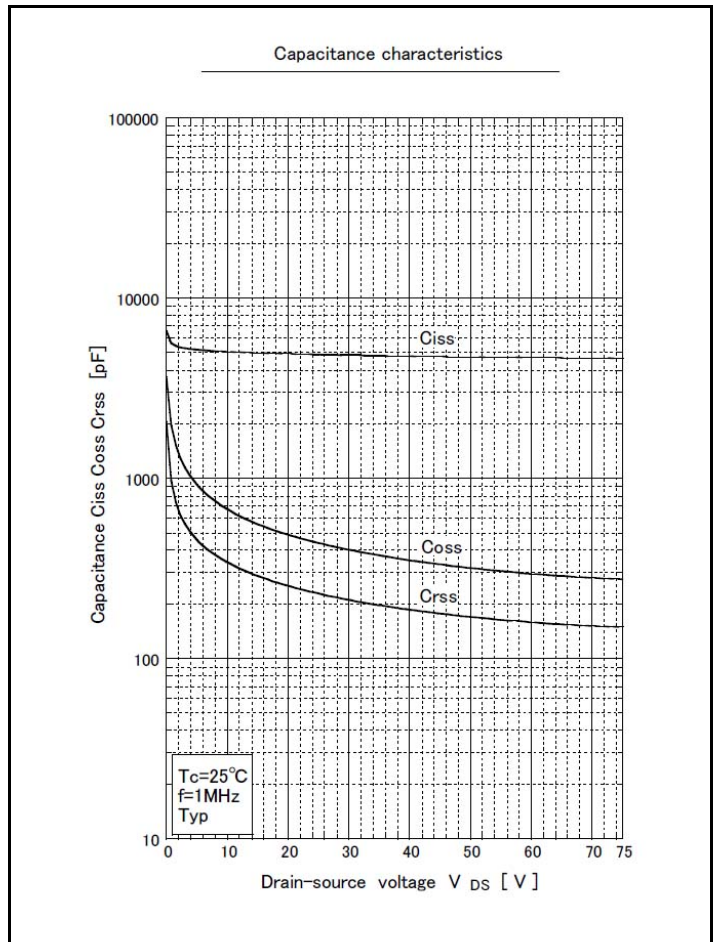
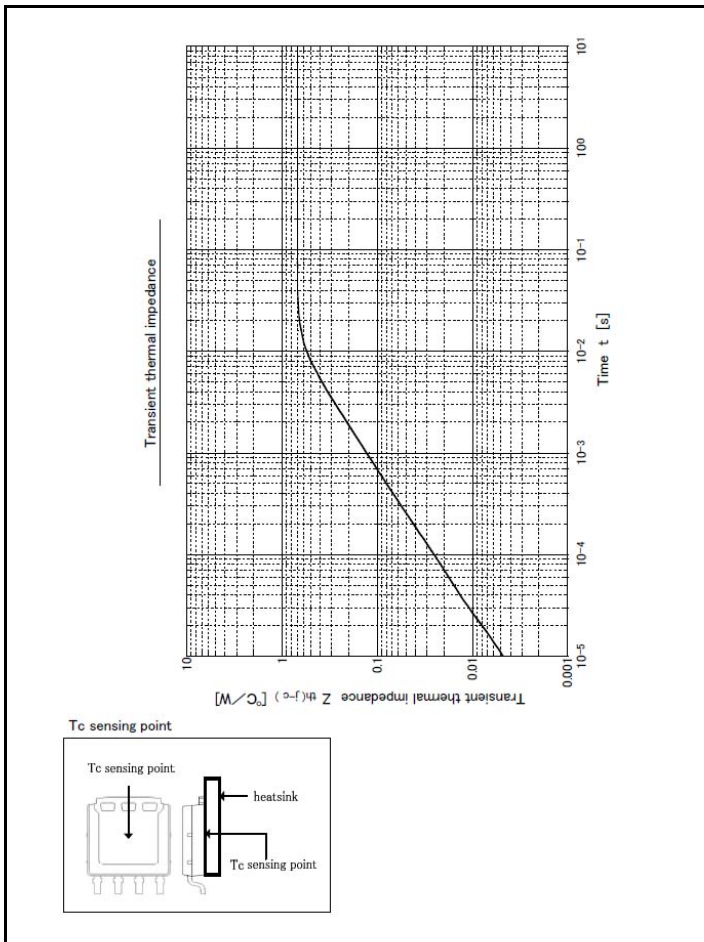
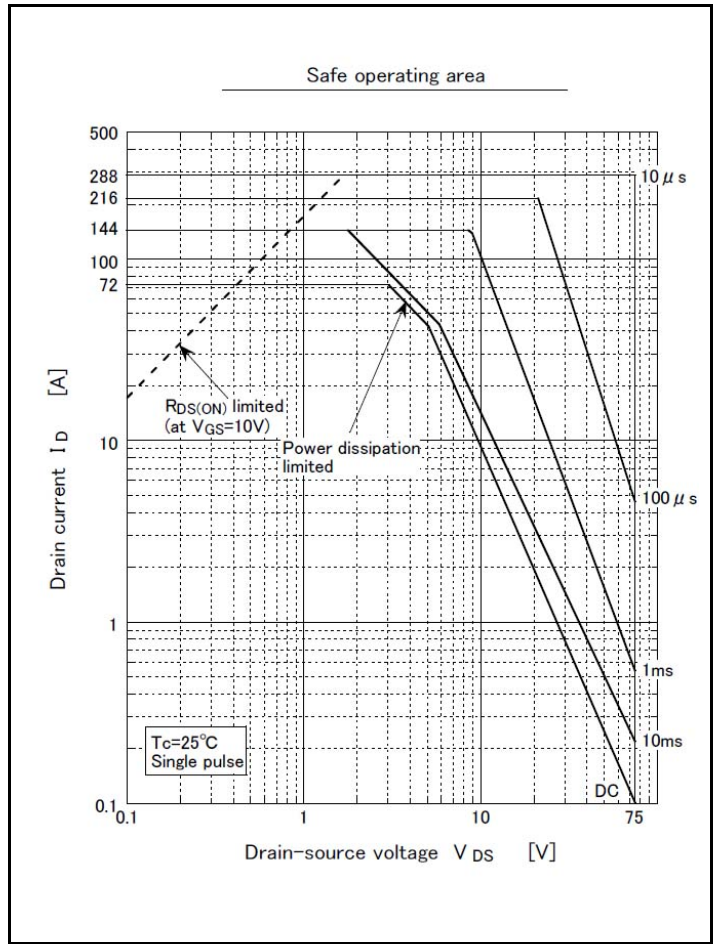
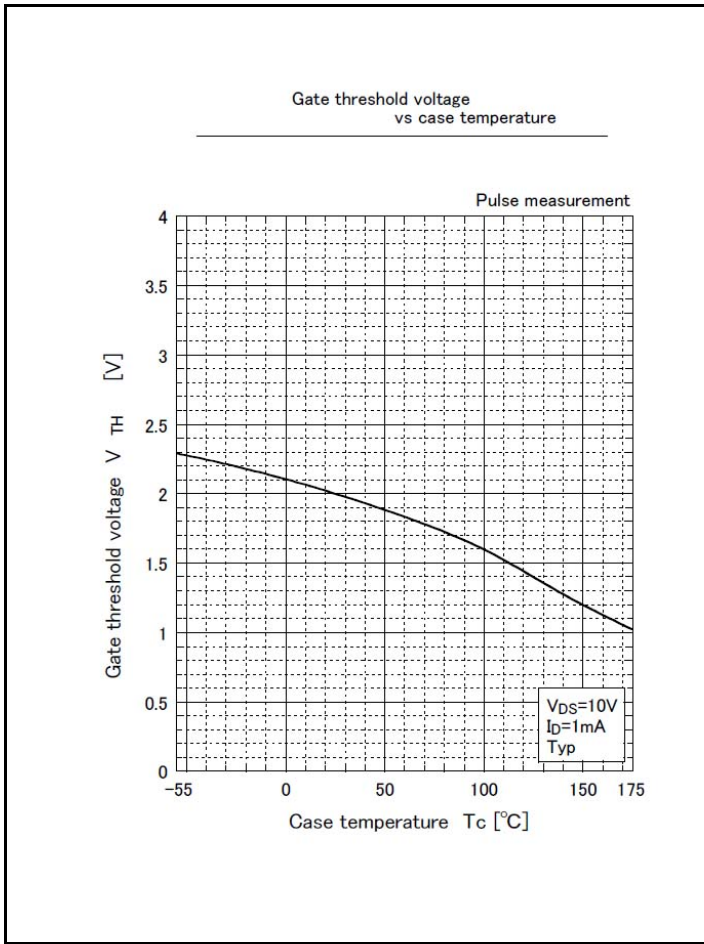


Static drain-source on-state resistance vs drain current



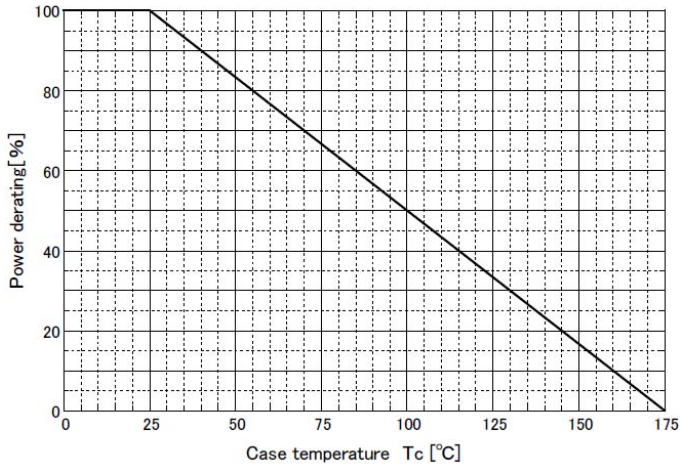
Static drain-source on-state resistance vs case temperature



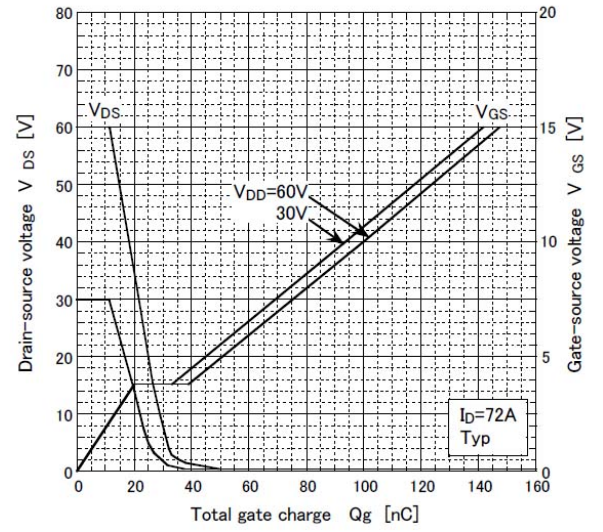




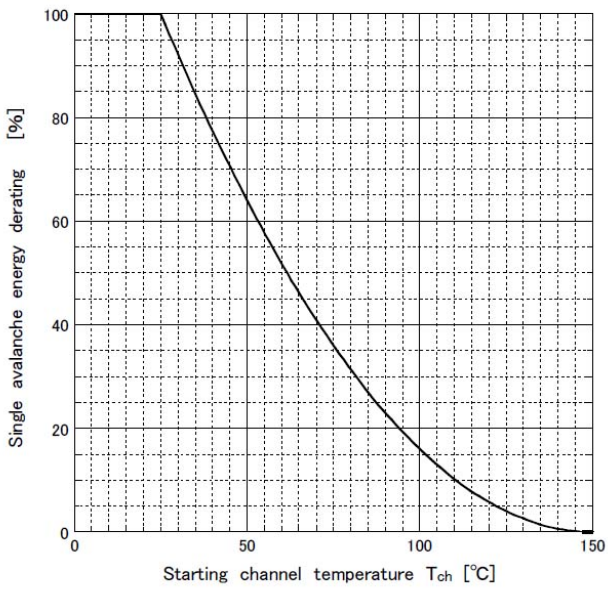
Power derating - case temperature



Gate charge characteristics

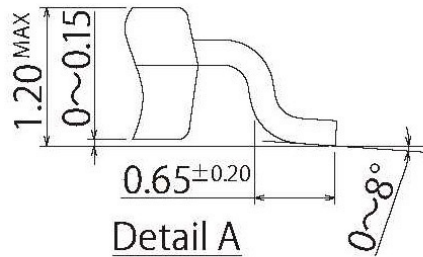
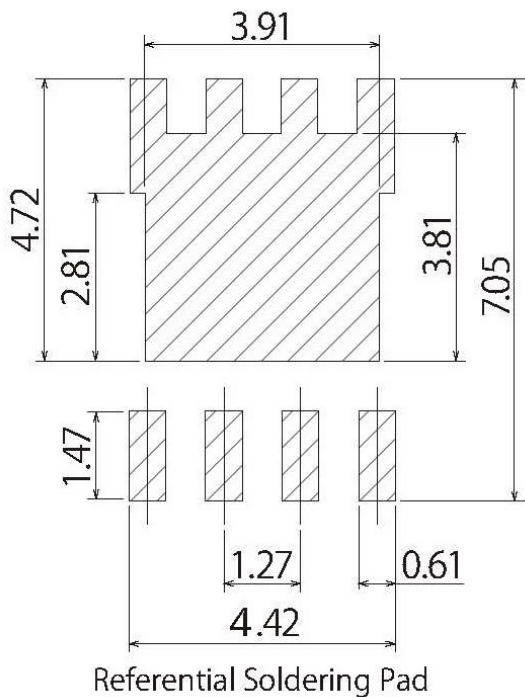
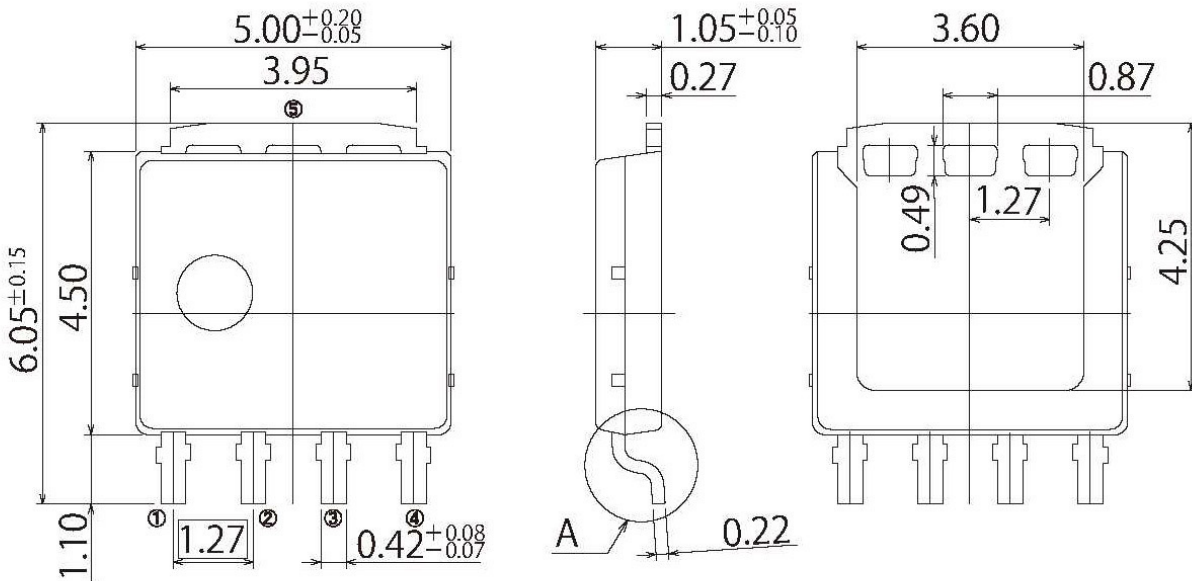


Single avalanche energy derating vs channel temperature



G7

JEDEC Code	MO-235B similar
JEITA Code	—
House Name	LF



• Optimize soldering pad to the board design and soldering condition.

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