

super-QR/PSR™ CV/CC Power Switch

FEATURES

- ◆ **Meet EPS Level 6**
- ◆ **Built-in 650V Power MOSFET**
- ◆ **Proprietary *super-QR/PSR™* (Quasi-Resonant & Primary Side Regulation) Control for High Efficiency and Low EMI**
- ◆ **Proprietary Cable Drop Compensation**
- ◆ **Max. Frequency Clamping to Limit Power MOSFET Vds Spike @ Output Short Circuit**
- ◆ **Less than 70mW Standby Power**
- ◆ **±5% CC and CV Precision**
- ◆ **Multi-Mode Control**
- ◆ **Cycle-by-Cycle Current Limiting**
- ◆ **Leading Edge Blanking (LEB)**
- ◆ **Soft Start**
- ◆ **Output Over Voltage Protection**
- ◆ **VDD UVLO, OVP & Clamp**

APPLICATIONS

- ◆ **Battery chargers for cellular phones, cordless phones, PDA, digital cameras, etc**
- ◆ **Replaces linear transformer and RCC SMPS**
- ◆ **AC/DC LED lighting**

GENERAL DESCRIPTION

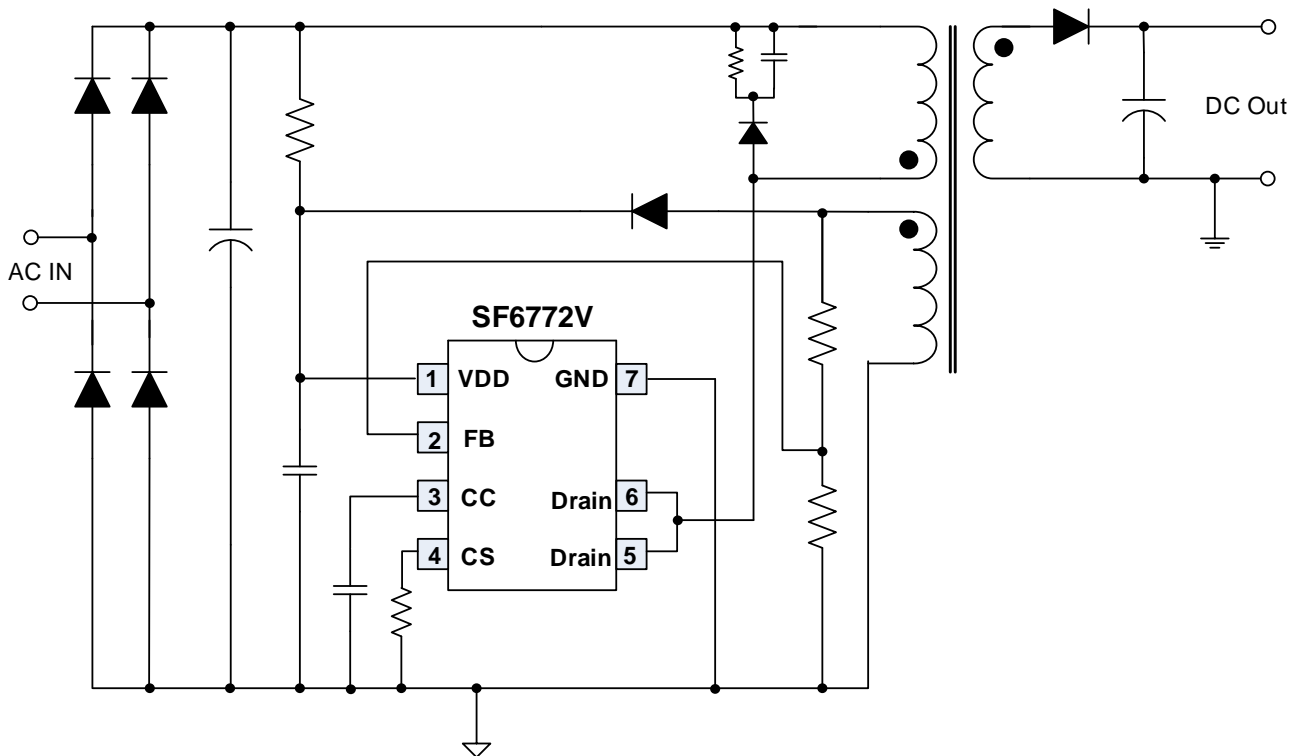
SF6772V is a high performance, highly integrated QR (Quasi Resonant Mode) and Primary Side Regulation (PSR) power switch for offline small power converter applications.

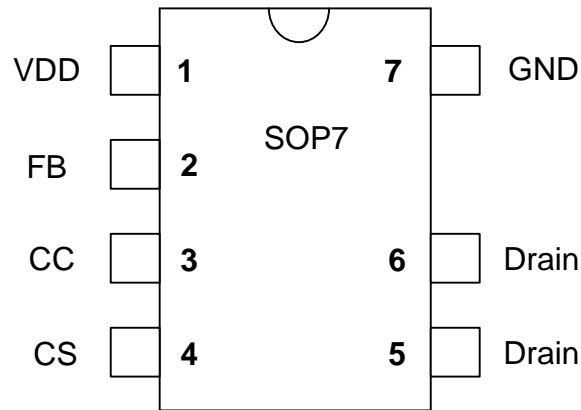
SF6772V has proprietary *super-QR/PSR™* control for high efficiency and low EMI, which can ensure system to meet EPS Level 6 energy standard. The IC also has built-in cable drop compensation function to achieve excellent CV performance.

SF6772V uses **Multi Mode Control** to improve efficiency and reliability and to decrease audio noise energy @ light loadings. SF6772V also integrates the function of "**Max. Frequency Clamping @ Output Short Circuit**" to limits power MOSFET Vds spike when output short circuits occurs.

SF6772V integrates functions and protections of FB Short Protection, Under Voltage Lockout (UVLO), VDD Over Voltage Protection (VDD OVP), Output Over Voltage Protection (Output OVP), Soft Start, Cycle-by-cycle Current Limiting (OCP), Pin Floating Protection, VDD Clamping.

SF6772V is available in SOP7 package.

TYPICAL APPLICATION


Pin Configuration

Ordering Information

| Part Number | Top Mark | Package | | Tape & Reel |
|-------------|-----------|---------|-------|-------------|
| SF6772VTG | SF6772VTG | SOP7 | Green | |
| SF6772VTGT | SF6772VTG | SOP7 | Green | Yes |

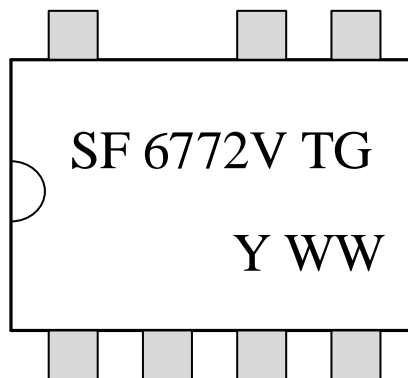
Output Power Table⁽¹⁾

| Part Number | 230VAC \pm 15% ⁽²⁾ | 85-265VAC |
|-------------|---------------------------------|------------------------|
| | Adapter ⁽³⁾ | Adapter ⁽³⁾ |
| SF6772V | 13W | 10W |

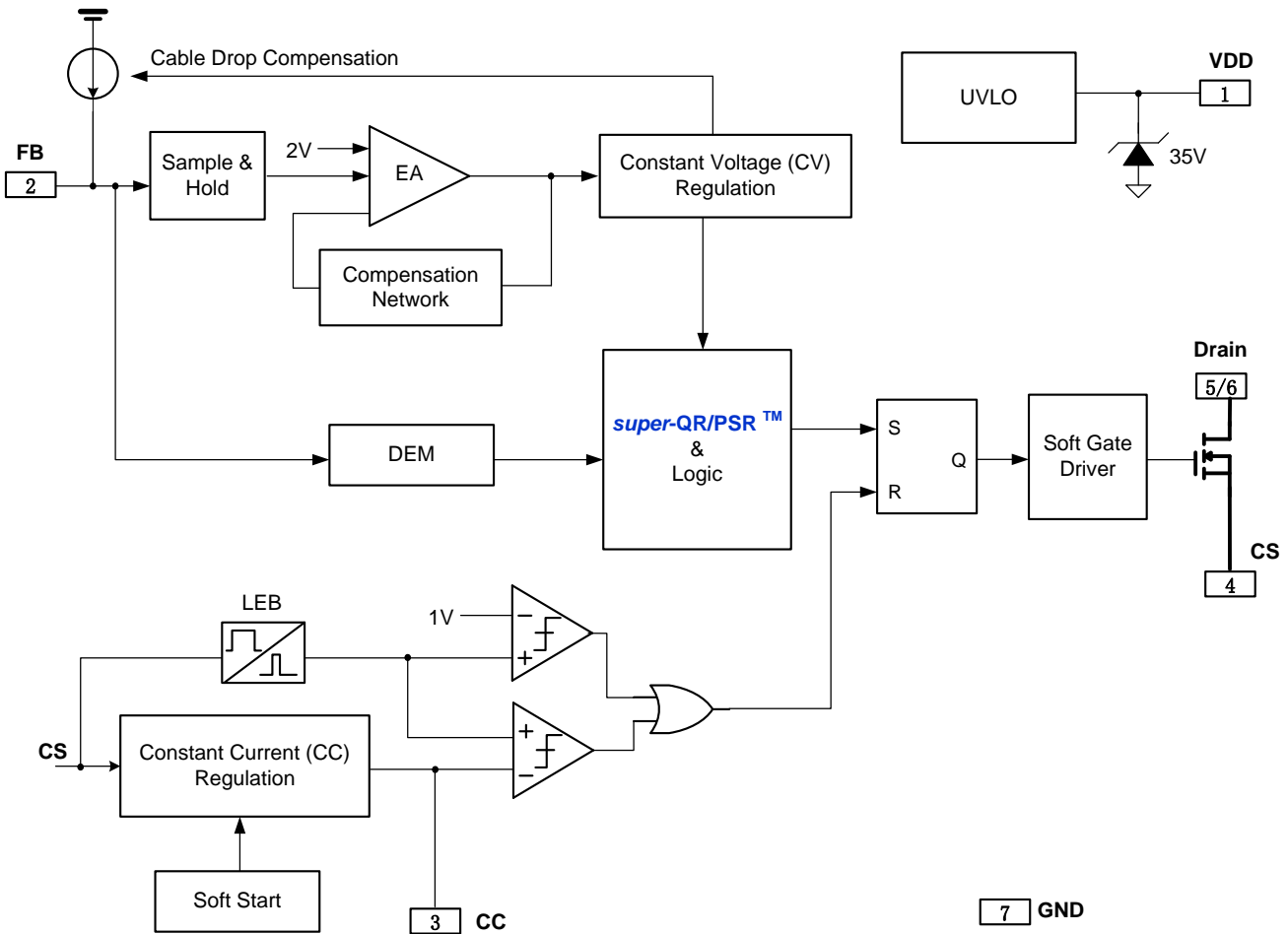
Note 1. The Max. output power is limited by junction temperature

Note 2. 230VAC or 100/115VAC with doublers

Note 3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50 °C ambient.

Marking Information


YWW: Year&Week code

Block Diagram

Pin Description

| Pin Num | Pin Name | I/O | Description |
|---------|----------|-----|---|
| 1 | VDD | P | IC power supply pin. |
| 2 | FB | I | System feedback pin. This control input regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding. |
| 3 | CC | O | Connect a capacitor between this pin and GND for CC regulation. |
| 4 | CS | I | Current sense pin. |
| 5-6 | Drain | P | High voltage power MOSFET drain connection. |
| 7 | GND | P | Ground |

Absolute Maximum Ratings (Note 1)

| Parameter | | Value | Unit |
|--|----------------|-------------|------|
| VDD DC Supply Voltage | | 35 | V |
| VDD DC Clamp Current | | 10 | mA |
| Drain pin | | -0.3 to 650 | V |
| CC, CS voltage range | | -0.3 to 7 | V |
| FB voltage range | | -0.7 to 7 | V |
| Package Thermal Resistance (SOP-7) | $\theta_{j a}$ | 150 | °C/W |
| | $\Psi_{j t}$ | 34 | |
| Maximum Junction Temperature | | 150 | °C |
| Operating Temperature Range | | -40 to 85 | °C |
| Storage Temperature Range | | -65 to 150 | °C |
| Lead Temperature (Soldering, 10sec.) | | 260 | °C |
| ESD Capability, HBM (Human Body Model) | | 3 | kV |
| ESD Capability, MM (Machine Model) | | 250 | V |

Recommended Operation Conditions (Note 2)

| Parameter | | Value | Unit |
|-------------------------------|--|-----------|------|
| Supply Voltage, VDD | | 10 to 30 | V |
| Operating Ambient Temperature | | -40 to 85 | °C |
| Maximum Switching Frequency | | 120K | Hz |

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

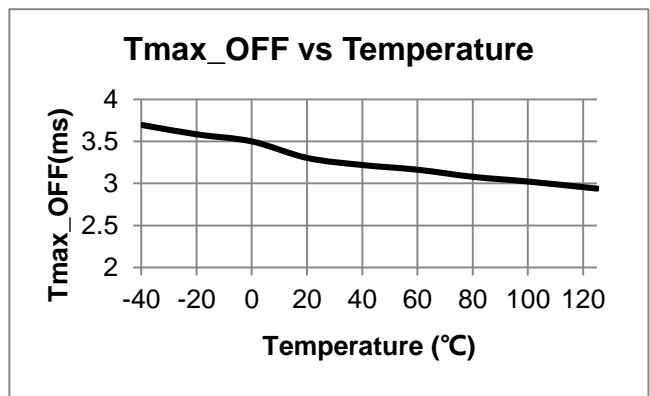
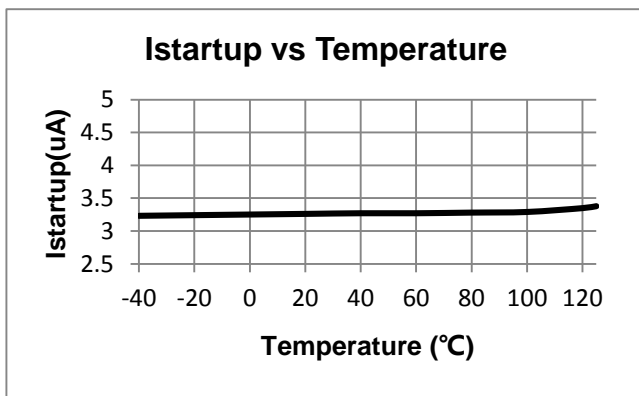
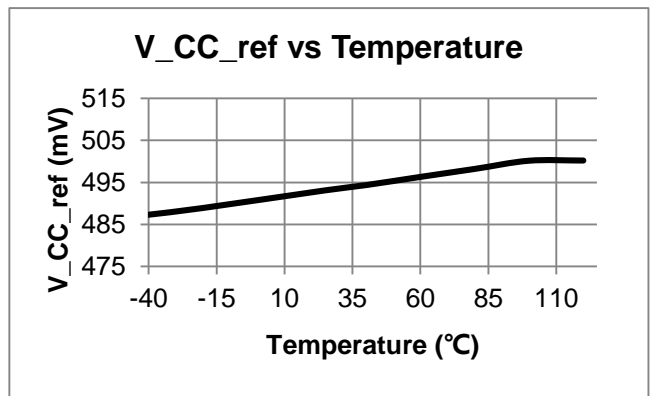
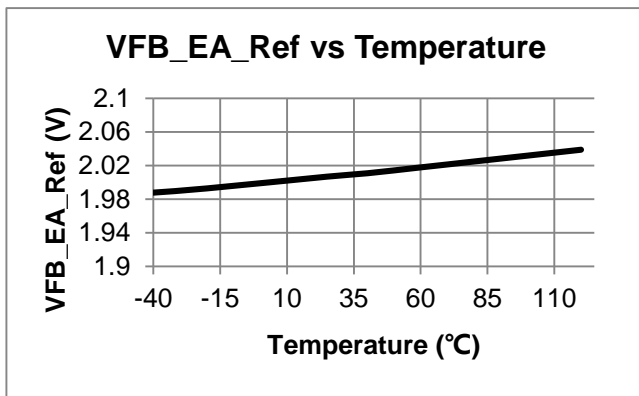
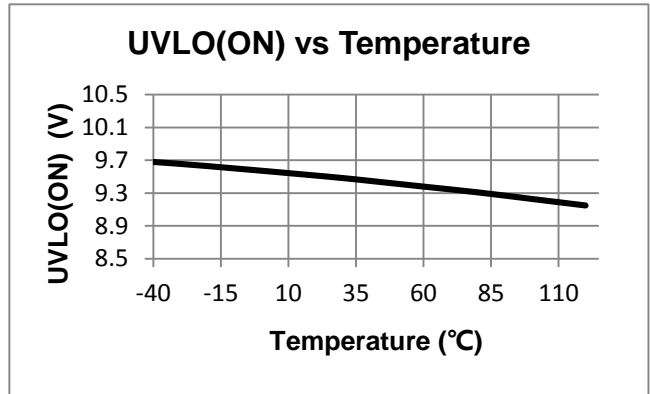
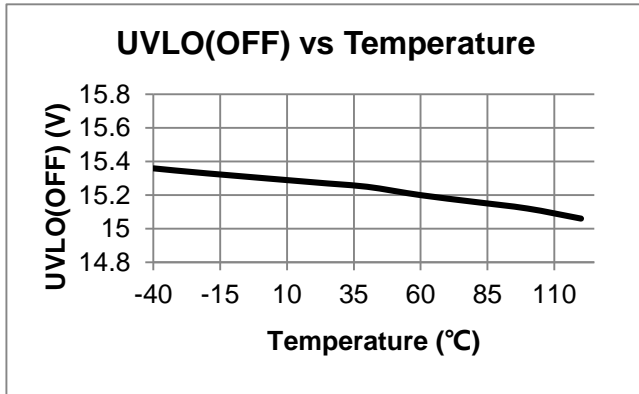
Note 2. The device is not guaranteed to function outside its operating conditions.

ELECTRICAL CHARACTERISTICS

 (T_A = 25°C, VDD=16V, if not otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|--|---------------------------------|------|------|------|------|
| Supply Voltage (VDD) Section | | | | | | |
| I_Startup | VDD Start up Current | VDD = UVLO(ON) - 1V | | 2 | 20 | uA |
| I_VDD_Op | Operation Current | V _{FB} = 1V, VDD = 20V | | 1 | 1.5 | mA |
| UVLO(OFF) | VDD Under Voltage Lockout Exit (Startup) | | 14 | 15.5 | 16.5 | V |
| UVLO(ON) | VDD Under Voltage Lockout Enter | | 8.5 | 9.5 | 10.5 | V |
| VDD_OVP | VDD Over Voltage Protection | | 31 | 33 | 35 | V |
| VDD_Clamp | VDD Zener Clamp Voltage | I(VDD) = 7 mA | 33 | 35 | 37 | V |
| Feedback Input Section (FB Pin) | | | | | | |
| V _{FB_EA_Ref} | Internal Error Amplifier(EA) reference input | | 1.97 | 2.0 | 2.03 | V |
| V _{FB_OVP} | Output over voltage protection threshold | | | 2.4 | | V |
| V _{FB_Short} | Output Short Circuit Threshold | | | 0.65 | | V |
| F _{Clamp_Short} | Output Short Circuit Frequency Clamp | | | 40 | | KHz |
| V _{FB_DEM} | Demagnetization comparator threshold | | | 75 | | mV |
| T _{min_OFF} | Minimum OFF time | (Note 3) | | 2 | | uSec |
| T _{max_OFF} | Maximum OFF time | (Note 3) | | 3 | | mSec |
| I _{Cable_max} | Max Cable compensation current | | | 40 | | uA |
| Current Sense Input Section (CS Pin) | | | | | | |
| T _{blanking} | CS Input Leading Edge Blanking Time | | | 500 | | nSec |
| T _{D_OC} | Over Current Detection and Control Delay | | | 100 | | nSec |
| V _{CS_max} | Max CS pin voltage | | | 1 | | V |
| Constant Current Section (CC Pin) | | | | | | |
| V _{CC_ref} | Internal CC reference | | 490 | 500 | 510 | mV |
| Power MOSFET Section | | | | | | |
| BV _{dss} | Power MOSFET Drain Source Breakdown Voltage | | 650 | | | V |
| R _{dson} | Static Drain-Source On Resistance | I(Drain) = 2A | | 3.8 | | Ω |
| I _{dss} | Zero Gate Voltage Drain Current | | | | 1 | uA |

Note 3. Guaranteed by design.

CHARACTERIZATION PLOTS


OPERATION DESCRIPTION

SF6772V is a high performance, multi mode controlled, highly integrated QR (Quasi Resonant) Primary Side Regulation (PSR) power switch with built-in fast dynamic response control. The built-in high precision CV/CC control with high level protection features make it very suitable for offline small power converter applications.

◆ Startup Current and Startup Control

Startup current of SF6772V is designed to be very low (typically 2uA) so that VDD could be charged up above UVLO(OFF) threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application.

◆ Operating Current

The operating current in SF6772V is as small as 1mA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement..

◆ *super-QR/PSR*TM Control

SF6772V uses a proprietary *super-QR/PSR*TM control for high efficiency and low EMI. The IC works in Quasi-Resonant (QR) mode in Constant Current (CC) and Constant Voltage (CV) mode. In this way, the efficiency is boosted and the EMI is reduced greatly. The IC can easily meet EPS level 6 standard.

◆ Constant Current (CC) Regulation

SF6772V can accurately control the output current by the internal current feedback control loop. The output mean current in constant current (CC) mode can be approximately expressed as:

$$I_{CC}(\text{mA}) = \frac{N}{2} \times \frac{500(\text{mV})}{R_{cs}(\Omega)}$$

In the equation above,

N---The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the MOSFET source to GND.

◆ Precision CV/CC Performance

In SF6772V, the parameters are trimmed to tight range, which makes the system CC/CV to have less than 5% variation.

◆ Soft Start

SF6772V features an internal soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. It reduces the stress on the secondary diode during startup. Every startup process is followed by a soft start activation.

◆ Proprietary Cable Voltage Drop Compensation in CV Mode

When it comes to cellular phone charger applications, the battery is located at the end of cable, which causes typically several percentage of voltage drop on the actual battery voltage. SF6772V has a proprietary built-in cable voltage drop compensation block which can provide a constant output voltage at the end of the cable over the entire load range in CV mode.

◆ Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the gate driver. Thus, external RC filter with a small time constant is enough for current sensing.

◆ Minimum and Maximum OFF Time

In SF6772V, a minimum OFF time (typically 2us) is implemented to suppress ringing when GATE is off. The minimum OFF time is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup. The maximum OFF time in SF6772V is typically 3ms, which provides a large range for frequency reduction. In this way, a low standby power of 70mW can be achieved.

◆ Smart Output Short Protection

The output short circuit protection of conventional PSR system is based on the coupling between auxiliary winding and secondary winding. When output is short, the auxiliary winding cannot provide enough energy to the IC any more. In this way, the system will enter into auto-recovery mode protection. However, the IC may be wrongly supplied if the leakage inductance of the primary winding is large enough.

In SF6772V, if output short circuit occurs, the IC will detect the situation and enter into auto-recovery mode protection.

◆ VDD OVP(Over Voltage Protection)

VDD OVP (Over Voltage Protection) is implemented in SF6772V and it is a protection of auto-recovery mode.

◆ Auto Recovery Mode Protection

As shown in Fig.1, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered from the auxiliary winding. When VDD falls to UVLO(on) (typical 9.5V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.1.

However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable and disable the switching until the fault condition is disappeared.

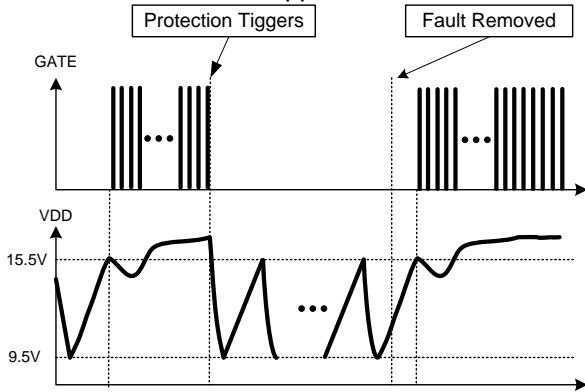


Fig.1

◆ **Pin Floating Protection**

In SF6772V, if pin floating situation occurs, the IC is designed to have no damage to system.

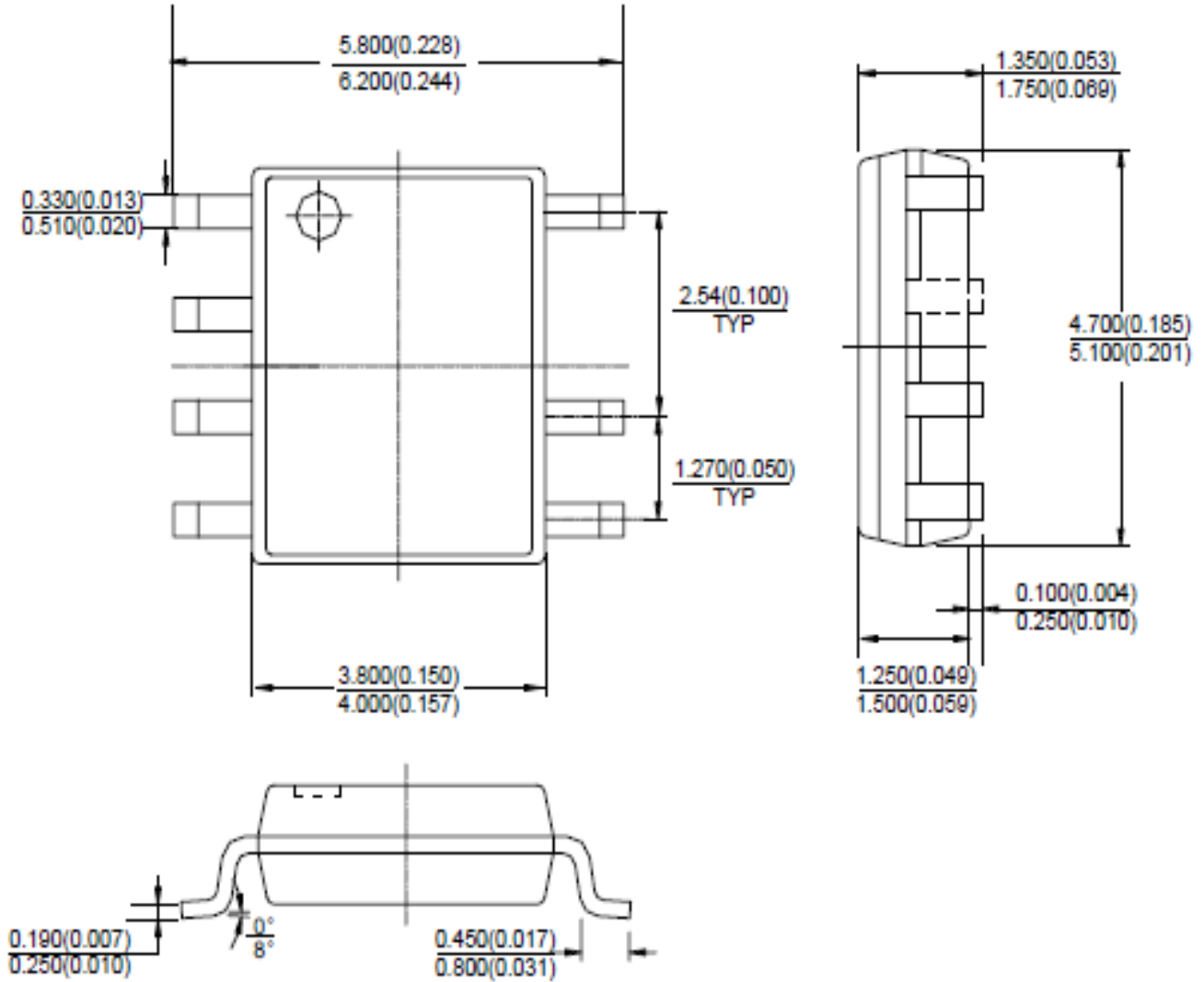
◆ **Soft Gate Drive**

SF6772V has a soft totem-pole gate driver with optimized EMI performance. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input.

PACKAGE MECHANICAL DATA

SOIC-7

Unit: mm(inch)



Note: Eject hole, oriented hole and mold mark is optional.

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