

## 178A, 40V N-CHANNEL MOSFET

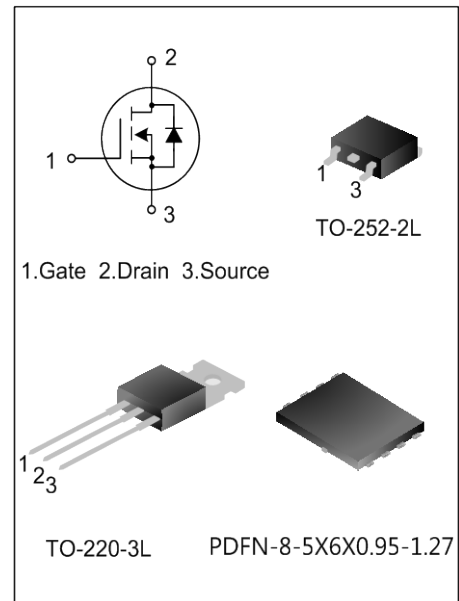
### DESCRIPTION

SVT044R5NT/D/L5 an N-channel enhancement mode power MOS field effect transistor which is produced using SILAN LVMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance.

This device is widely used in UPS, Power Management for Inverter Systems.

### FEATURES

- ◆ 178A,40V
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



### ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVT044R5NT	TO-220-3L	044R5NT	Pb free	Tube
SVT044R5NDTR	TO-252-2L	044R5ND	Halogen free	Tape&Reel
SVT044R5NL5TR	PDFN-8-5X6X0.95-1.27	044R5NL5	Halogen free	Tape&Reel

### ABSOLUTE MAXIMUM RATINGS (Unless otherwise noted, T<sub>c</sub>=25°C)

Characteristics	Symbol	Ratings			Unit
		SVT044R5NT	SVT044R5ND	SVT044R5NL5	
Drain-Source Voltage	V <sub>DS</sub>	40			V
Gate-Source Voltage	V <sub>GS</sub>	±20			V
Drain Current	T <sub>C</sub> =25°C	178			A
	T <sub>C</sub> =100°C	112			
	T <sub>C</sub> =25°C(package limited)	160	128	105	
Drain Current Pulsed	I <sub>DM</sub>	640			A
Power Dissipation(T <sub>C</sub> =25°C) -Derate above 25°C	P <sub>D</sub>	178	112	100	W
		1.42	0.90	0.8	W/°C
Single Pulsed Avalanche Energy(Note 1)	E <sub>AS</sub>	612			mJ
Operation Junction Temperature Range	T <sub>J</sub>	-55~+150			°C
Storage Temperature Range	T <sub>stg</sub>	-55~+150			°C

## THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings			Unit
		SVT044R5NT	SVT044R5ND	SVT044R5NL5	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.70	1.12	1.25	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	50	°C/W

## ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $T_c=25^\circ\text{C}$ )

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40	--	--	V
Drain-Source Leakage Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	--	--	1.0	$\mu A$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS}=\pm 25V, V_{DS}=0V$	--	--	$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	--	3.5	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=50A$ (220/252)	--	3.5	4.5	m $\Omega$
		$V_{GS}=10V, I_D=50A$ (PDFN5*6)	--	3.0	3.6	
Gate Resistance	$R_G$	$f=1\text{MHz}$		2.0		$\Omega$
Input Capacitance	$C_{iss}$	$f=1\text{MHz}, V_{GS}=0V, V_{DS}=25V$	--	5603	--	pF
Output Capacitance	$C_{oss}$		--	542	--	
Reverse Transfer Capacitance	$C_{rss}$		--	401	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, V_{GS}=10V, R_G=24\Omega,$ $I_D=160A$ (Note 2,3)	--	51	--	ns
Turn-on Rise Time	$t_r$		--	130	--	
Turn-off Delay Time	$t_{d(off)}$		--	245	--	
Turn-off Fall Time	$t_f$		--	179	--	
Total Gate Charge	$Q_g$	$V_{DD}=32V, V_{GS}=10V, I_D=80A$ (Note 2,3)	--	111	--	nC
Gate-Source Charge	$Q_{gs}$		--	30	--	
Gate-Drain Charge	$Q_{gd}$		--	32	--	

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	$I_S$	Integral Reverse P-N Junction	--	--	160	A
Pulsed Source Current	$I_{SM}$	Diode in the MOSFET	--	--	640	
Diode Forward Voltage	$V_{SD}$	$I_S=50A, V_{GS}=0V$	--	--	1.0	V
Reverse Recovery Time	$T_{rr}$	$I_S=40A, V_{GS}=0V,$	--	28	--	ns
Reverse Recovery Charge	$Q_{rr}$	$dI/dt=100A/\mu s$	--	0.02	--	$\mu C$

### Notes:

1.  $L=1\text{mH}, V_{DD}=38V, R_G=10\Omega,$  starting  $T_J=25^\circ\text{C}$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s,$  Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. Output Characteristics

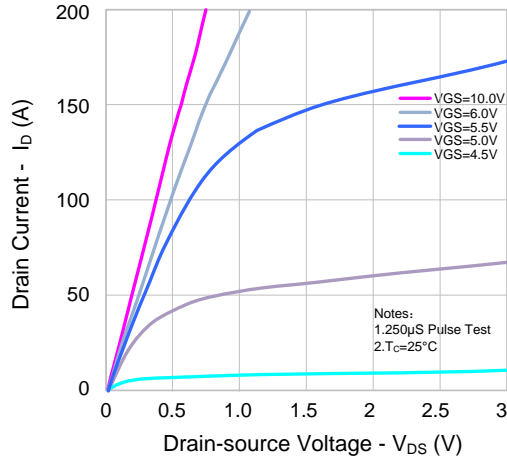


Figure 2. Transfer Characteristics

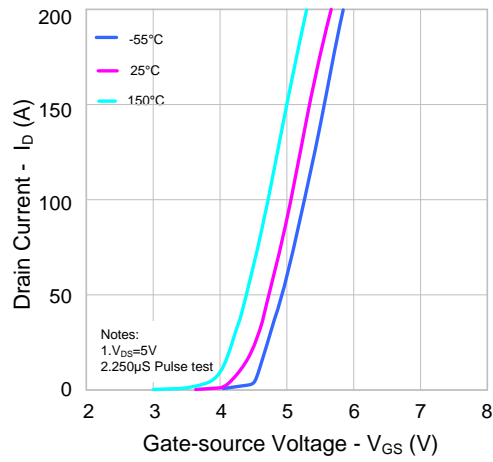


Figure 3. On-resistance vs. Drain Current

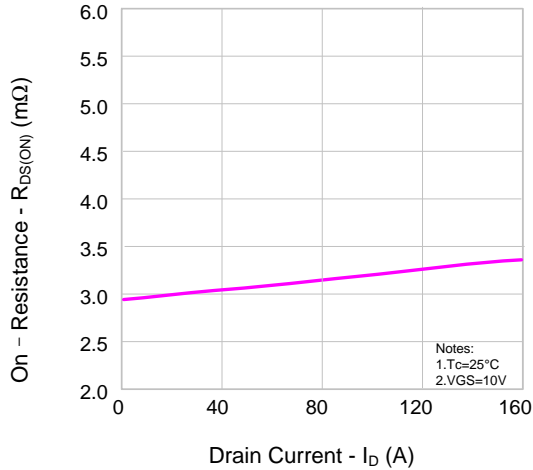


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

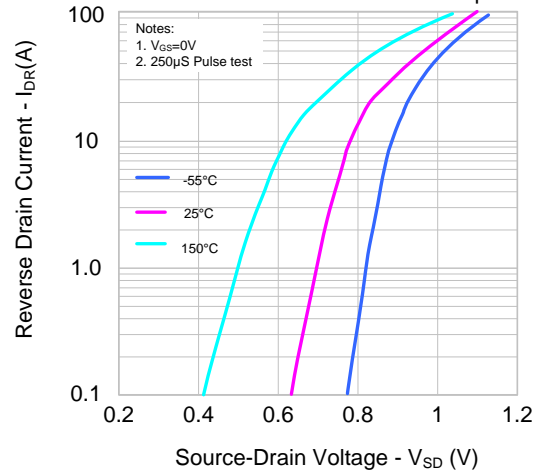


Figure 5. Capacitance Characteristics

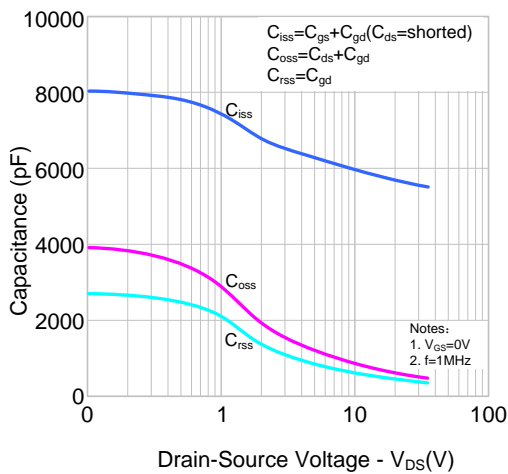
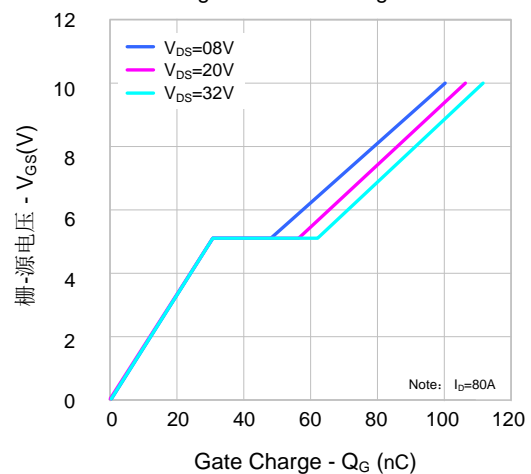
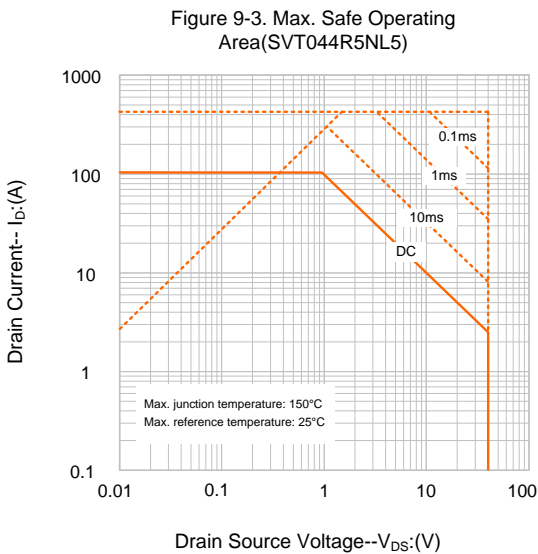
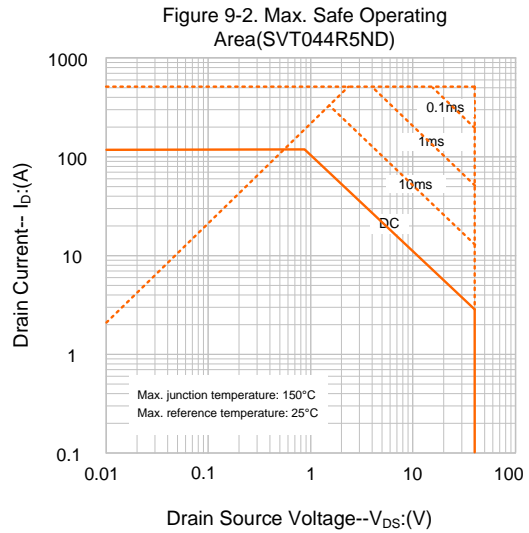
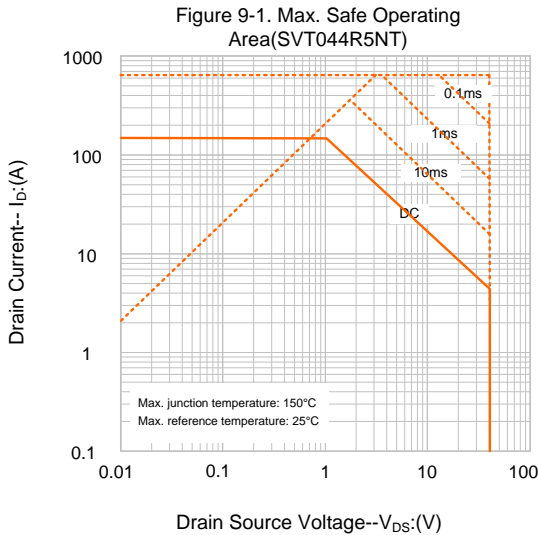
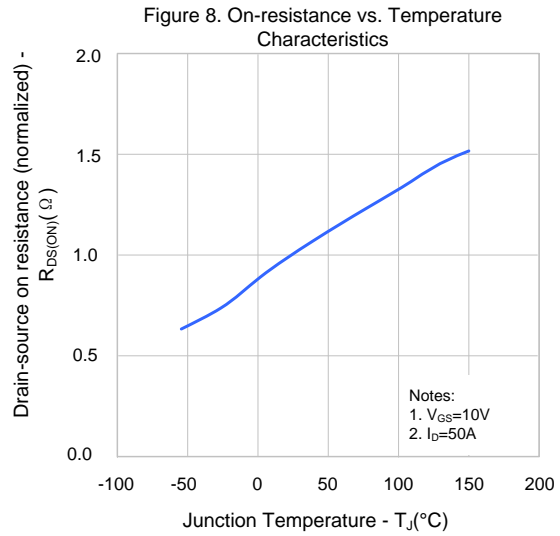
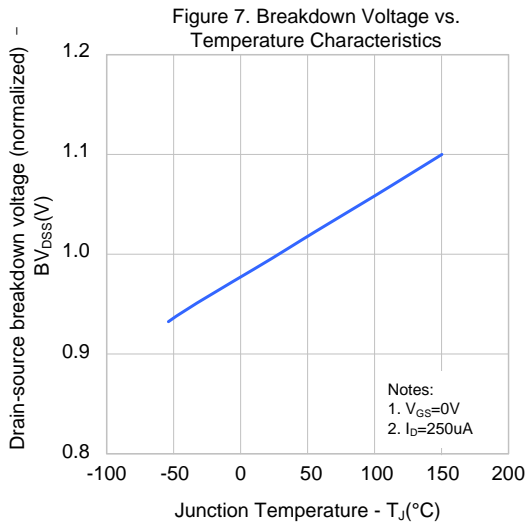


Figure 6. Gate Charge

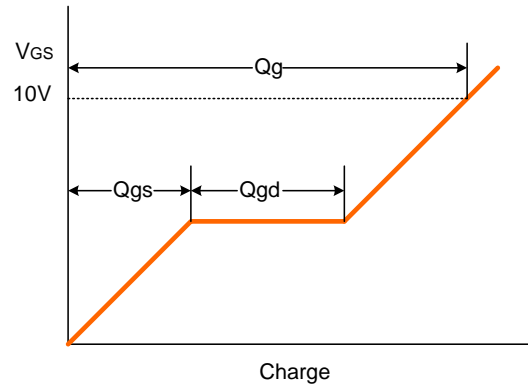
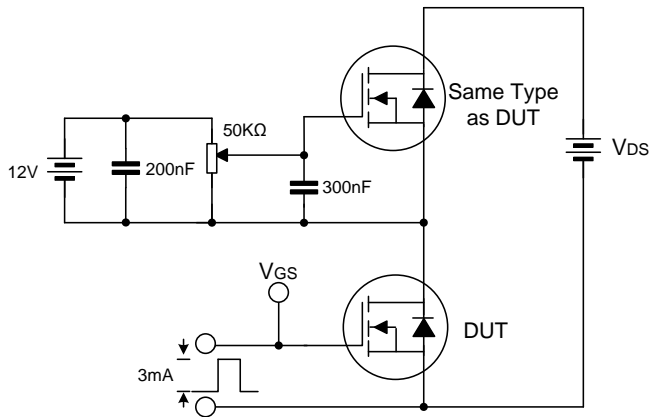


**TYPICAL CHARACTERISTICS(continued)**

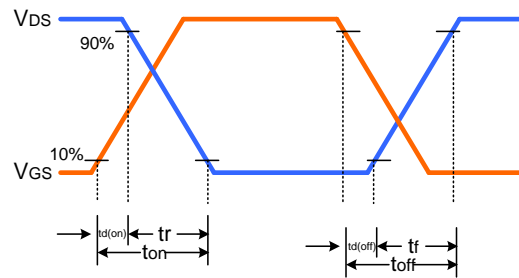
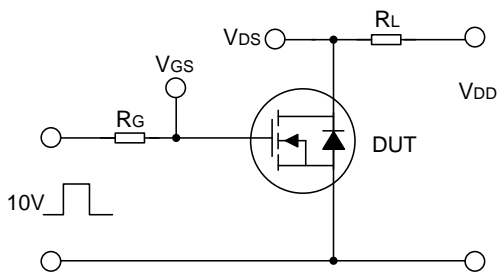


**TYPICAL TEST CIRCUIT**

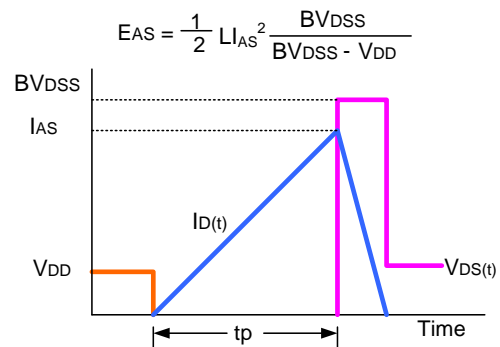
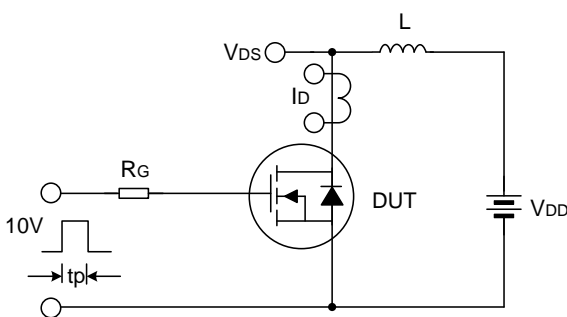
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



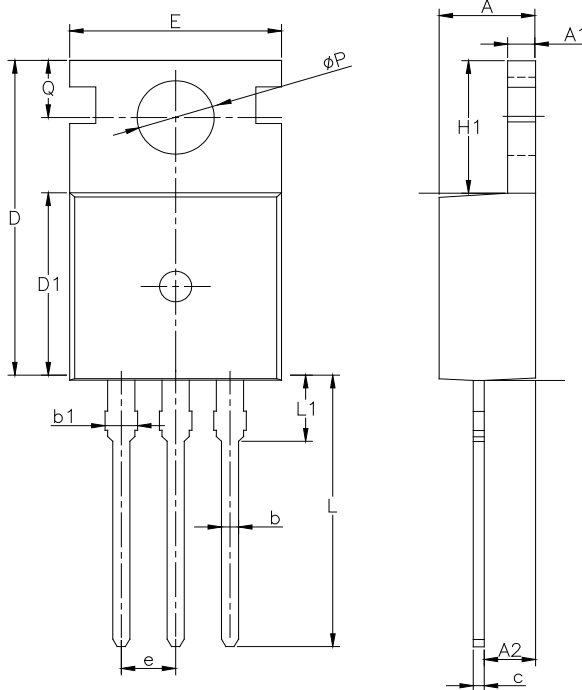
Unclamped Inductive Switching Test Circuit & Waveform



**PACKAGE OUTLINE**

**TO-220-3L**

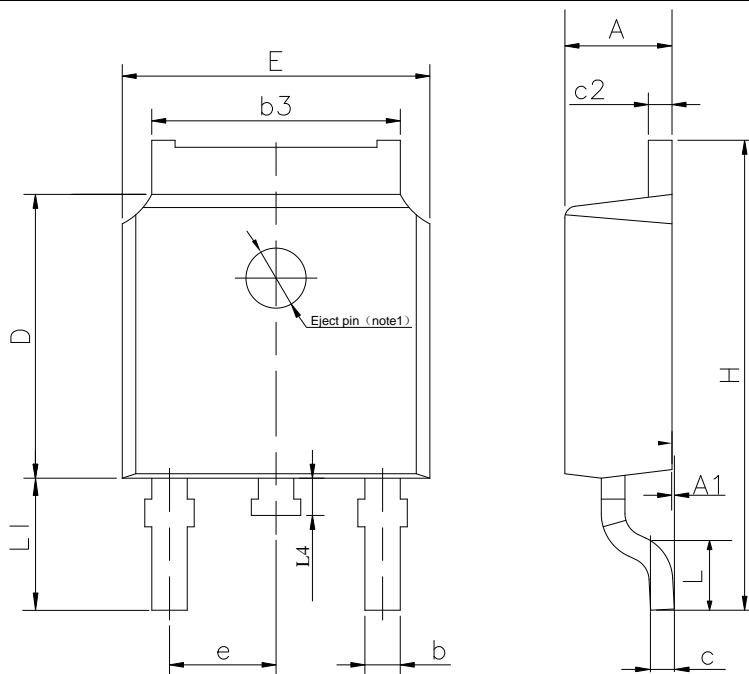
**UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
phi P	3.40	3.70	3.90
Q	2.60	—	3.20

**TO-252-2L**

**UNIT: mm**



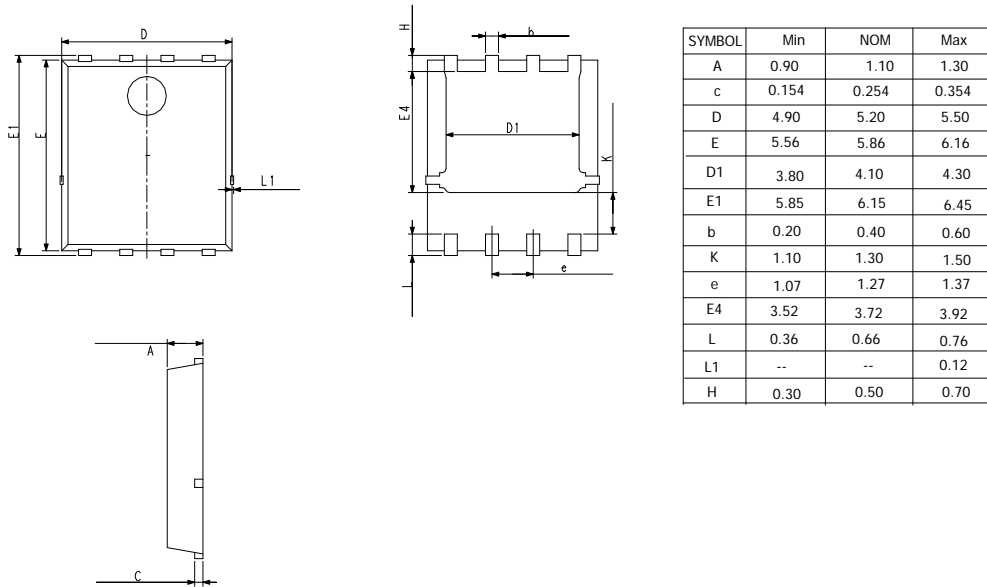
SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

## PACKAGE OUTLINE(continued)

PDFN-8-5X6X0.95-1.27

单位: 毫米



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Rev.: 1.3

Revision History:

1. Update characteristics and Fig 5 and 6
- 

Rev.: 1.2

Revision History:

1. Add PDFN-8-5X6X0.95-1.27
  2. Update the package outline of TO-220-3L
- 

Rev.: 1.1

Revision History:

1. Add TO-252-2L
- 

Rev.: 1.0

Revision History:

1. First release
-



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