Dual 4.5A Integrated Power Switch with One Channel Discharge and Reverse Blocking

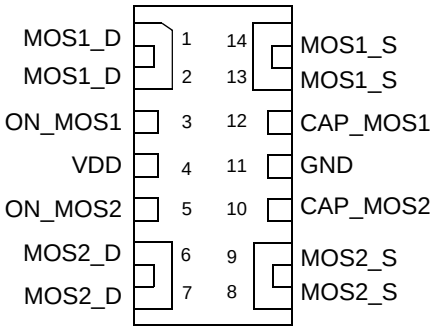
General Description

The SLG59M1612V is designed for load switching application. The part comes with two 4.5 A rated MOSFETs switched on by two ON control pins. Each MOSFETs turn on time is independently adjusted by an external capacitor. One channel discharge is active when both ON signals are inactive.

Features

- Two 4.5 A independent MOSFETs with Reverse Current Blocking
- Two Integrated VGS Charge Pumps
- Internal discharge for Channel 1. Discharge when both ON_MOS1 & ON_MOS2 = Low
- Independent Ramp Control
- Protected by thermal shutdown
- Pb-Free / RoHS Compliant
- Halogen-Free / MSL 1
- STDFN 14L, 1 x 3 x 0.55 mm

Pin Configuration

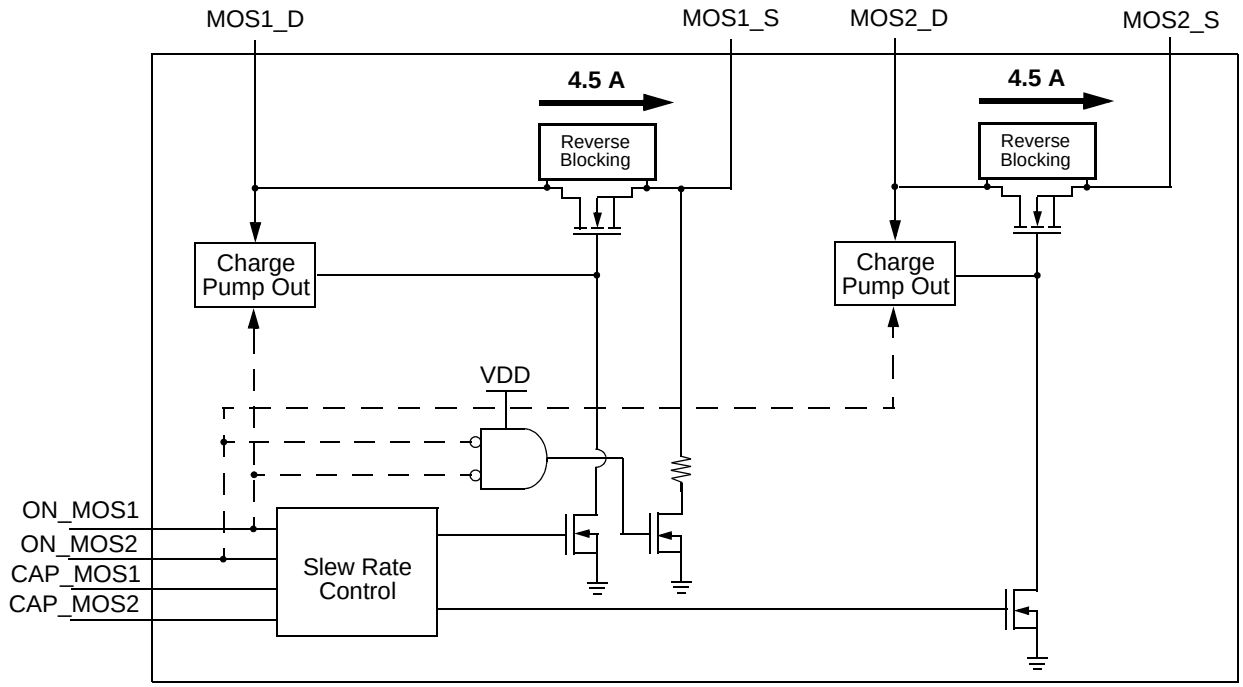


14-pin STDFN
(Top View)

Applications

- Ideal for switching ON and OFF S0 +5.0 and 3.3V power rails with associated support circuitry discharges.
- Ideal for switching ON and OFF power rails 5V or less.
- Can use either channel up to 5.5A with combined maximum current of 8.5A
- Maximum load capacitance of 1000 µF for each Channel Source terminal.

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	MOS1_D	MOSFET	Drain of MOSFET1
2	MOS1_D	MOSFET	Drain of MOSFET1 (fused with pin 1)
3	ON_MOS1	Input	Turns on MOS1 (4 MΩ pull down resistor)
4	VDD	VDD	+5VDD Power
5	ON_MOS2	Input	Turns on MOS2 (4 MΩ pull down resistor)
6	MOS2_D	MOSFET	Drain of MOSFET2
7	MOS2_D	MOSFET	Drain of MOSFET2 (fused with pin 6)
8	MOS2_S	MOSFET	Source of MOSFET2 (fused with pin 9)
9	MOS2_S	MOSFET	Source of MOSFET2
10	CAP_MOS2	Input	Sets ramp and turn on time for MOSFET2
11	GND	GND	Ground
12	CAP_MOS1	Input	Sets ramp and turn on time for MOSFET1
13	MOS1_S	MOSFET	Source of MOSFET1 (fused with pin 14)
14	MOS1_S	MOSFET	Source of MOSFET1

Discharge Logic Table

VDD	ON_MOS1	ON_MOS2	Channel 1 Discharge
No Power	X	X	Hi-Z
Power	HIGH	LOW	OFF
Power	LOW	HIGH	OFF
Power	LOW	LOW	ON

Notes:

1. Discharge on Channel 1 is only activated when both ON_MOS1 and ON_MOS2 = LOW
2. Channel 2 has no internal discharge circuitry.

Ordering Information

Part Number	Type	Production Flow
SLG59M1612V	STDFN 14L	Industrial, -40 °C to 85 °C
SLG59M1612VTR	STDFN 14L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_D	Power Supply		--	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
W_{DIS}	Package Power Dissipation		--	--	1.2	W
IDS_{MAX}	Max Operating Current				4.5	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 10 continuous seconds out of every 100 seconds	--	--	6	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

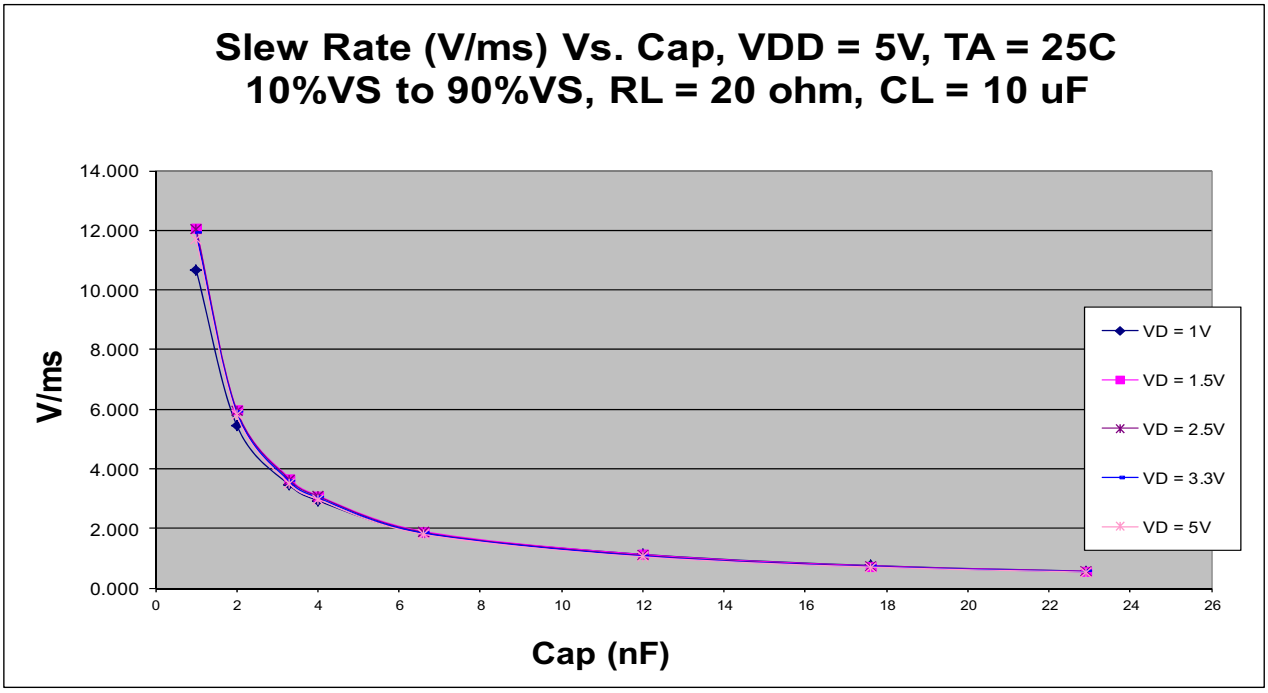
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage		2.5	--	5.5	V
I_{DD}	Power Supply Current when OFF		--	0.1	1	µA
	Power Supply Current ON_MOS_1 & ON_MOS_2 (Steady State)		--	50	100	µA
RDS_{ON}	ON Resistance	T_A 25°C MOSFET1 @100 mA	--	16.0	19.8	mΩ
		T_A 70°C MOSFET1 @100 mA	--	18.7	24.2	mΩ
		T_A 85°C MOSFET1 @100 mA		19.8	25.3	mΩ
		T_A 25°C MOSFET2 @100 mA	--	16.0	19.8	mΩ
		T_A 70°C MOSFET2 @100 mA	--	18.7	24.2	mΩ
		T_A 85°C MOSFET2 @100 mA		19.8	25.3	mΩ
MOSFET IDS	Current from Drain to Source for each MOSFET	Continuous, each channel	--	--	4.5	A
IDS_{LKG}	IDS Leakage (Reverse Blocking enabled)	V_S = 1.0 V to 5.0 V, V_{DD} = V_D = 0 V, ON_MOS = LOW, 0 to 85 °C, each channel	--	0.5	1.5	µA
		V_S = 1.0 V to 5.0 V, V_{DD} = V_D = 0 V, ON_MOS = LOW, -40 to 0 °C, each channel	--	3	5	µA
V_D	Drain Voltage		1.0	5.0	V_{DD}	V
T_{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin, R_L = 20 Ω, C_L = 10 µF	0	300	500	µs
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Configurable [1]			ms
		Example: CAP = 4 nF, V_{DD} = V_D = 5 V, Source_Cap = 10 µF, R_L = 20 Ω	--	2.0	--	ms
$T_{SLEWRATE}$	Slew Rate	10% V_S to 90% V_S	Configurable [1]			V/ms
		Example: CAP = 4 nF, V_{DD} = V_D = 5 V, Source_Cap = 10 µF, R_L = 20 Ω	--	3.0	--	V/ms
CAP_{SOURCE}	Source Cap	Source to GND	--	--	1000	µF
R_{DIS}	Discharge Resistance		100	150	300	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V

T_A = -40 °C to 85 °C (unless otherwise stated)

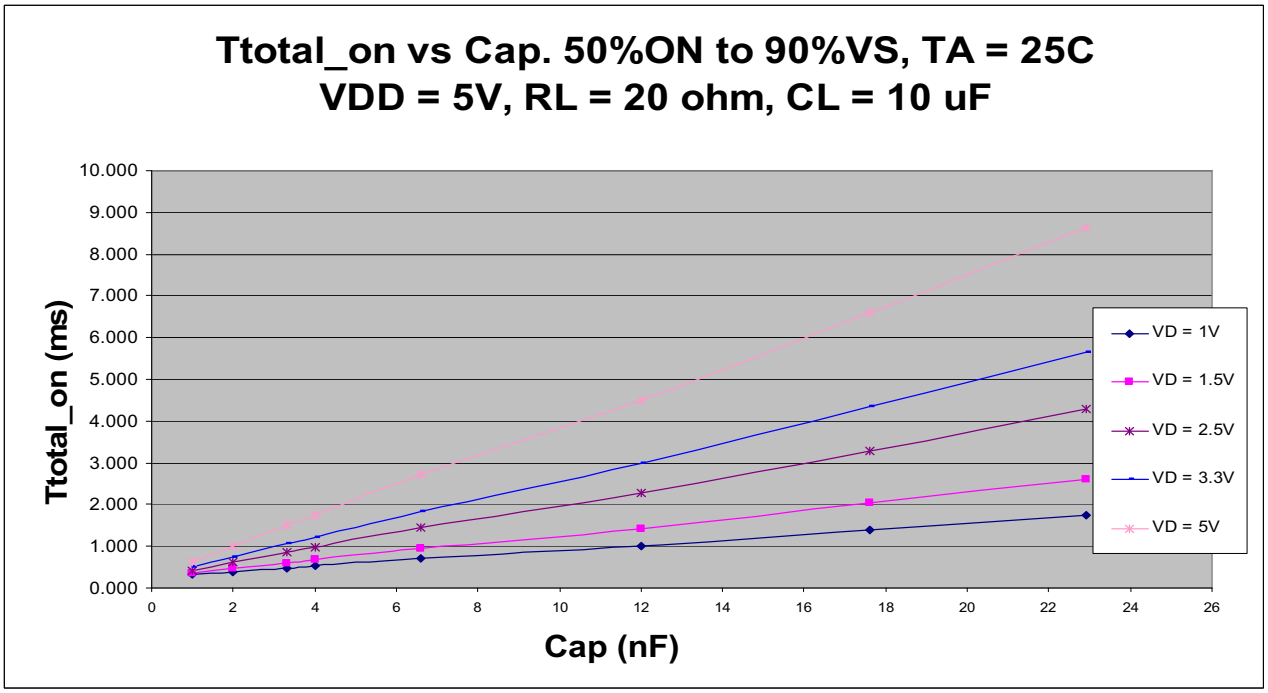
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$THERM_{ON}$[2]	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall, V_{DD} = V_D = 5 V, R_L = 20 Ω, no C_L	--	--	15	µs

Notes:
1. Refer to table for configuration details.
2. When device enters thermal shutdown, both channels will turn off.

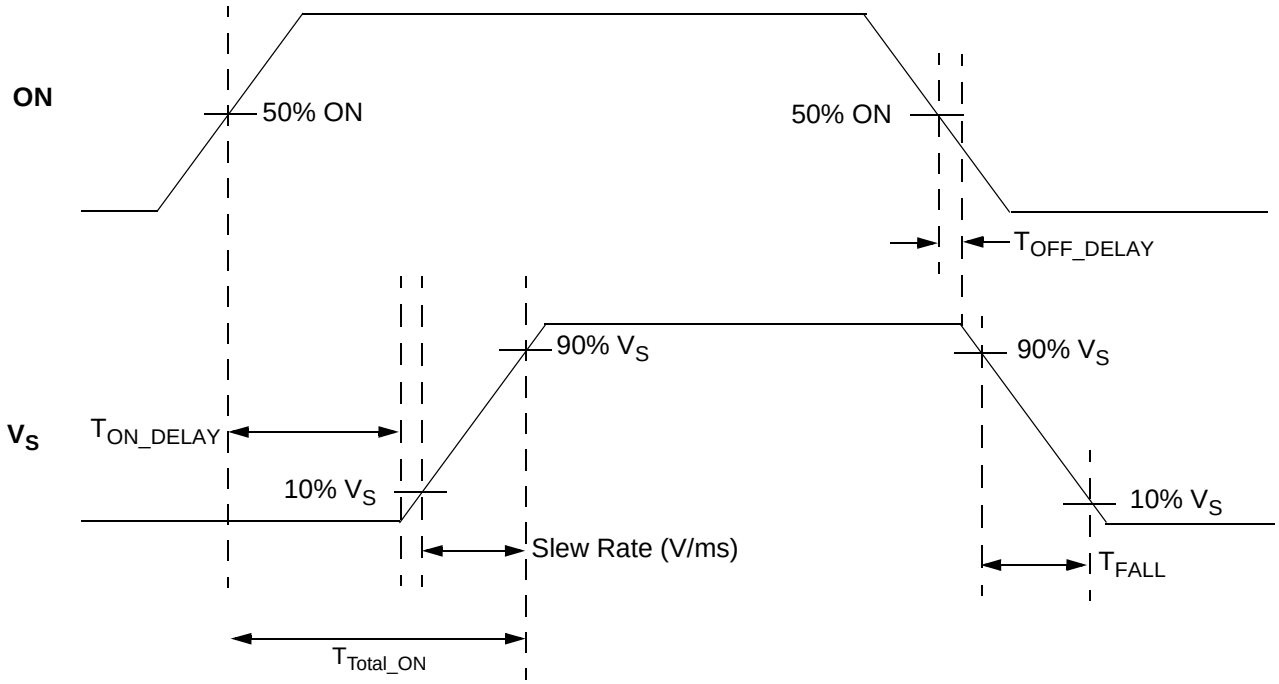
T_{SLEW} vs. CAP



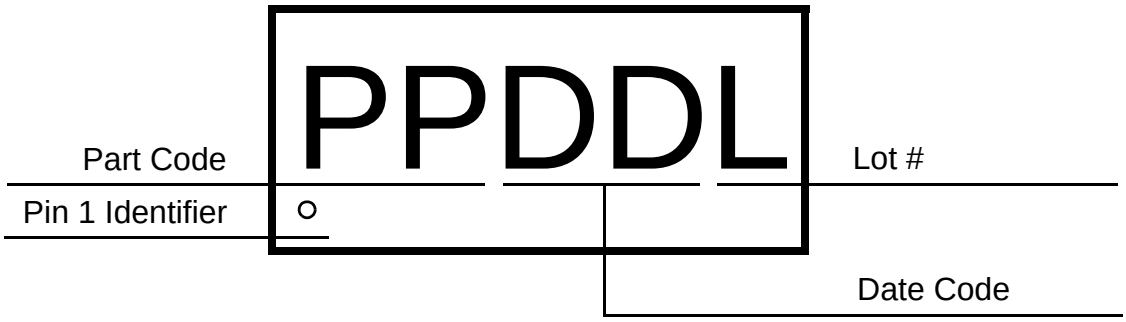
T_{TOTAL_ON} vs. CAP



T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement

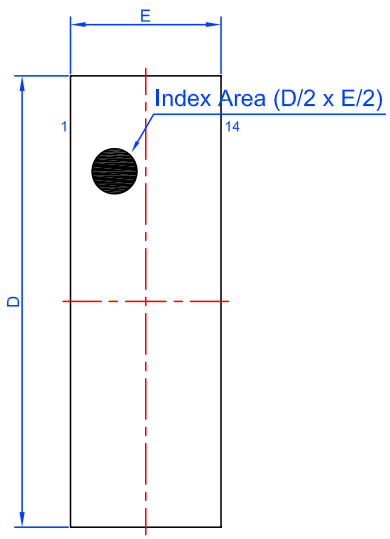


Package Top Marking System Definition

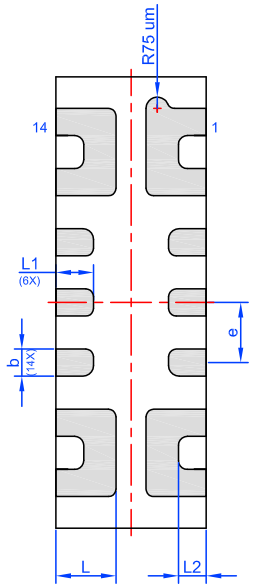


Package Drawing and Dimensions

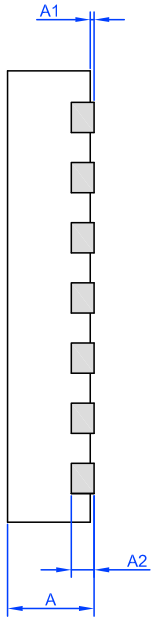
14 Lead STDFN Package 1 mm x 3 mm (Fused Lead)



Top View



BTM View



SIDE View

Unit: mm

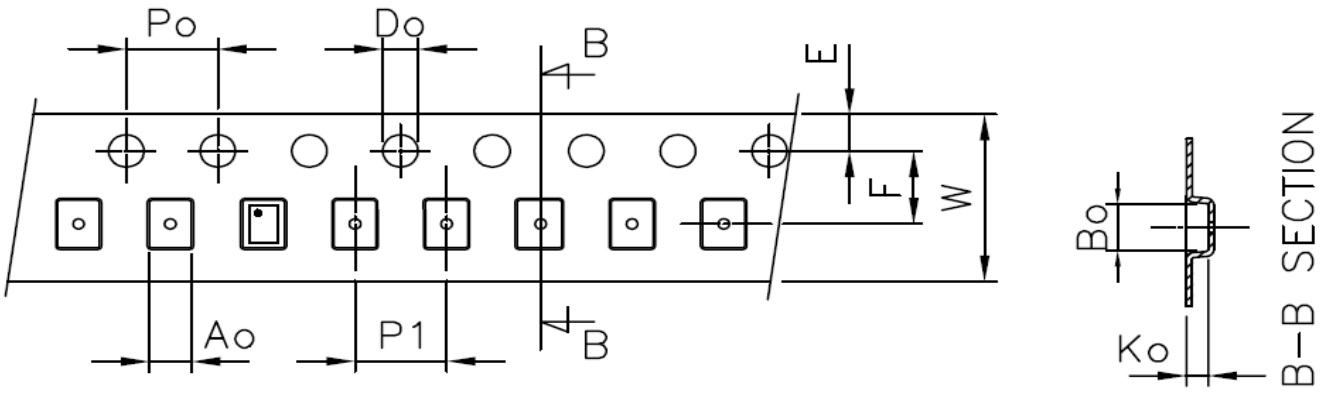
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.20	0.25	0.30
e	0.40 BSC			L2	0.06	0.11	0.16

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size	Units per Reel	Max Units per Box	Reel & Hub Size (mm)	Trailer A		Leader B		Pocket Tape (mm)	
						Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STDFN 14L	14	1x3x0.55mm	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 14L	1.15	3.15	0.7	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.65 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
9/9/2015	1.00	Production Release Updated Electrical Characteristics conditions

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