



## Ultra-small 22 mΩ 4 A Load Switch with Discharge and Reverse Current Blocking

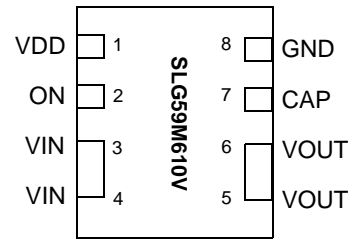
### General Description

The SLG59M610V is a 22 mΩ 4 A single-channel load switch that is able to switch 1 to 5 V power rails. The product is packaged in an ultra-small 1.5 x 2.0 mm package.

### Features

- 1.5 x 2.0 mm FC-TDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 22 mΩ RDS<sub>ON</sub> while supporting 4 A
- Two Over Current Protection Modes
  - Short Circuit Current Limit
  - Active Current Limit
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 85°C
- Operating Voltage: 2.5 V to 5.5 V

### Pin Configuration

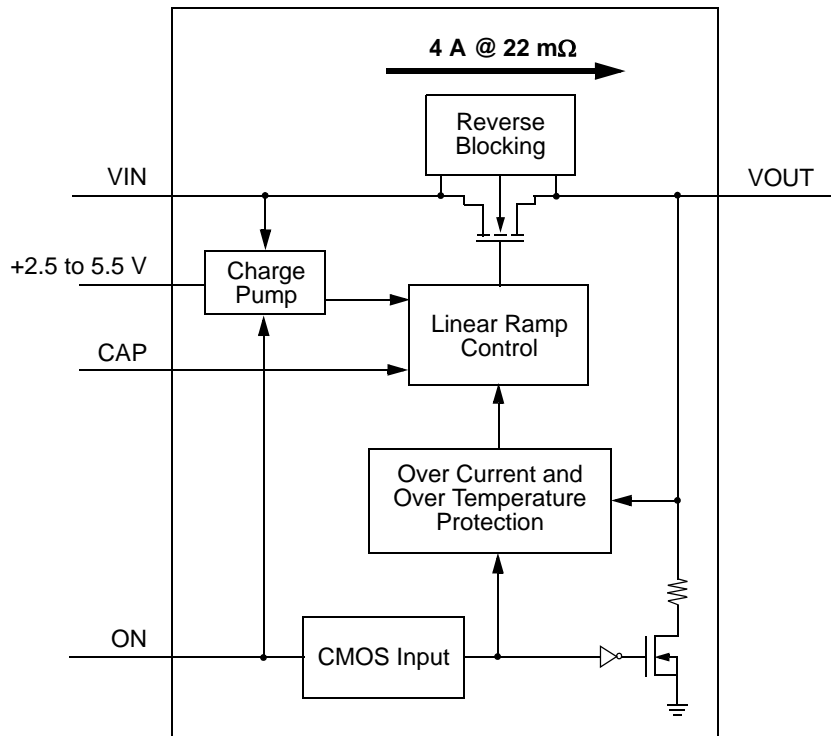


**8-pin FC-TDFN (Top View)**

### Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

### Block Diagram





### Pin Description

| Pin # | Pin Name | Type   | Pin Description  |
|-------|----------|--------|--|
| 1     | VDD      | PWR    | VDD power for load switch control (2.5 V to 5.5 V)   |
| 2     | ON       | Input  | Turns MOSFET ON (4 M $\Omega$ pull down resistor)<br>CMOS input with VIL < 0.3 V, VIH > 0.85 V |
| 3     | VIN      | MOSFET | Drain of Power MOSFET (fused with pin 4)   |
| 4     | VIN      | MOSFET | Drain of Power MOSFET (fused with pin 3)   |
| 5     | VOUT     | MOSFET | Source of Power MOSFET (fused with pin 6)  |
| 6     | VOUT     | MOSFET | Source of Power MOSFET (fused with pin 5)  |
| 7     | CAP      | Input  | Capacitor for controlling power rail ramp rate   |
| 8     | GND      | GND    | Ground   |

### Ordering Information

| Part Number  | Type                       | Production Flow             |
|--------------|----------------------------|-----------------------------|
| SLG59M610V   | FC-TDFN 8L                 | Industrial, -40 °C to 85 °C |
| SLG59M610VTR | FC-TDFN 8L (Tape and Reel) | Industrial, -40 °C to 85 °C |



## Absolute Maximum Ratings

| Parameter                            | Description                       | Conditions                               | Min. | Typ. | Max. | Unit |
|--------------------------------------|-----------------------------------|--|------|------|------|------|
| V <sub>DD</sub>                      | Power Supply                      |  | --   | --   | 7    | V    |
| T <sub>S</sub>                       | Storage Temperature               |  | -65  | --   | 150  | °C   |
| ESD <sub>HBM</sub>                   | ESD Protection                    | Human Body Model                         | 2000 | --   | --   | V    |
| W <sub>DIS</sub>                     | Package Power Dissipation         |  | --   | --   | 1    | W    |
| MOSFET I <sub>DS</sub> <sub>PK</sub> | Peak Current from Drain to Source | For no more than 1 ms with 1% duty cycle | --   | --   | 6    | A    |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

T<sub>A</sub> = -40 °C to 85 °C (unless otherwise stated)

| Parameter                         | Description                          | Conditions   | Min.                      | Typ. | Max.            | Unit |
|-----------------------------------|--------------------------------------|--|---------------------------|------|-----------------|------|
| V <sub>DD</sub>                   | Power Supply Voltage                 | -40 °C to 85 °C  | 2.5                       | --   | 5.5             | V    |
| I <sub>DD</sub>                   | Power Supply Current (PIN 1)         | when OFF   | --                        | --   | 1               | μA   |
|                                   |                                      | when ON, No load   | --                        | 70   | 100             | μA   |
| R <sub>DS</sub> <sub>ON</sub>     | Static Drain to Source ON Resistance | T <sub>A</sub> 25 °C @ 100 mA  | --                        | 22   | 28              | mΩ   |
|                                   |                                      | T <sub>A</sub> 70 °C @ 100 mA  | --                        | 25   | 30              | mΩ   |
|                                   |                                      | T <sub>A</sub> 85 °C @ 100 mA  | --                        | 27   | 31              | mΩ   |
| I <sub>DS</sub>                   | Operating Current                    | V <sub>IN</sub> = 1.0 V to 5.5 V   | --                        | --   | 4               | A    |
| V <sub>IN</sub>                   | Drain Voltage                        |  | 1.0                       | --   | V <sub>DD</sub> | V    |
| T <sub>ON</sub> <sub>Delay</sub>  | ON pin Delay Time                    | 50% ON to Ramp Begin   | 0                         | 300  | 500             | μs   |
| T <sub>Total_ON</sub>             | Total Turn On Time                   | 50% ON to 90% V <sub>OUT</sub>   | Configurable <sup>1</sup> |      |                 | ms   |
|                                   |                                      | Example: CAP (PIN 7) = 4 nF, V <sub>DD</sub> = V <sub>IN</sub> = 5 V, Source_Cap = 10 μF, I <sub>DS</sub> = 100 mA | --                        | 1.96 | --              | ms   |
| T <sub>SLEWRATE</sub>             | Slew Rate                            | 10% V <sub>S</sub> to 90% V <sub>S</sub>   | Configurable <sup>1</sup> |      |                 | V/ms |
|                                   |                                      | Example: CAP (PIN 7) = 4 nF, V <sub>DD</sub> = V <sub>IN</sub> = 5 V, Source_Cap = 10 μF, I <sub>DS</sub> = 100 mA | --                        | 3.0  | --              | V/ms |
| I <sub>REVERSE</sub>              | Reverse Blocking Current             | V <sub>OUT</sub> = 5.0, V <sub>IN</sub> = 0 V; V <sub>DD</sub> = 0 V; ON = 0 V                                     | --                        | 0.5  | 2               | μA   |
| CAP <sub>SOURCE</sub>             | Source Cap                           | Source to GND  | --                        | --   | 500             | μF   |
| R <sub>DIS</sub>                  | Discharge Resistance                 |  | 100                       | 150  | 300             | Ω    |
| ON_V <sub>IH</sub>                | High Input Voltage on ON pin         |  | 0.85                      | --   | V <sub>DD</sub> | V    |
| ON_V <sub>IL</sub>                | Low Input Voltage on ON pin          |  | -0.3                      | 0    | 0.3             | V    |
| I <sub>LIMIT</sub>                | Active Current Limit                 | MOSFET will automatically limit current when V <sub>S</sub> > 250 mV   | --                        | 6.0  | --              | A    |
|                                   | Short Circuit Current Limit          | MOSFET will automatically limit current when V <sub>S</sub> < 250 mV   | --                        | 0.5  | --              | A    |
| THERM <sub>ON</sub>               | Thermal shutoff turn-on temperature  |  | --                        | 125  | --              | °C   |
| THERM <sub>OFF</sub>              | Thermal shutoff turn-off temperature |  | --                        | 100  | --              | °C   |
| THERM <sub>TIME</sub>             | Thermal shutoff time                 |  | --                        | --   | 1               | ms   |
| T <sub>OFF</sub> <sub>Delay</sub> | OFF Delay Time                       | 50% ON to V <sub>OUT</sub> Fall, V <sub>DD</sub> = V <sub>IN</sub> = 5 V   | --                        | 7.5  | 15              | μs   |

Notes:  
1. Refer to table for configuration details.



## SLG59M610V Turn ON

The normal power on sequence is first VDD, with VD only being applied after VDD is > 1 V, and then ON after VD is at least 90% of final value. The normal power off sequence is the power on sequence in reverse.

If VDD and VD are turned on at the same time then it is possible that a voltage glitch will appear on VS before VDD achieves 1V which is the  $V_T$  of the main MOSFET. The size of the glitch is dependent on source and drain capacitance loading and the ramp rate of VDD & VD. The glitch can be eliminated with at least 10  $\mu$ F of capacitance on VS.

The VS ramp follows a linear path, not an RC limitation provided the ramp is slow enough to not be current limited by load capacitance.

## SLG59M610V Current Limiting

The SLG59M610V has two modes of current limiting, differentiated by the output (Source pin) voltage.

### 1. Standard Current Limiting Mode (with Thermal Protection)

When  $V(S) > 250$  mV, the output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics table. The current limiting circuit is very fast and responds within a few micro-seconds to sudden loads. When overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceeding the Active Current Limit.

However, if an overload condition persists, the die temperature rise due to the increased FET resistance while at maximum current can activate Thermal Protection. If the die temperature exceeds the  $THERM_{ON}$  specification, the FET is shut completely OFF, allowing the die to cool. When the die cools to the  $THERM_{OFF}$  temperature, the FET is allowed to turn back on. This process may repeat as long as the overload condition is present.

### 2. Short Circuit Current Limiting Mode (with Thermal Protection)

When  $V(S) < 250$  mV (which is the case with a hard short, such as a solder bridge on the power rail), the current is limited to approximately 500 mA. Thermal Protection is also present, but since the Short Circuit Current Limit is much lower than Standard Current Limit, activation may only occur at higher ambient temperatures.

## Reverse Current Blocking Protection Operation

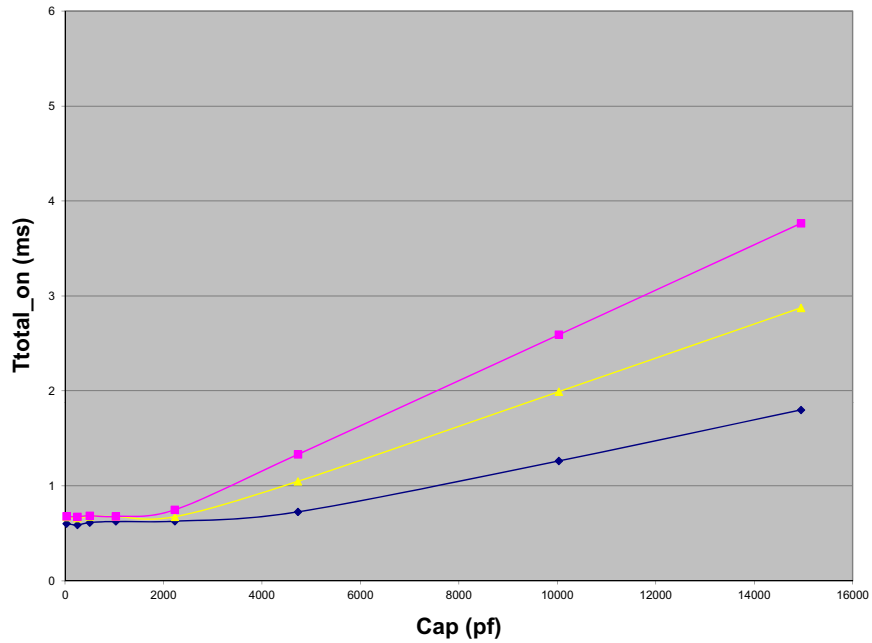
In the SLG59M610V, reverse current blocking is active only when ON = Low. Thus if ON = High, current may flow in both directions even if external  $V_{OUT} > V_{IN}$  is suddenly applied. Once ON = Low, the SLG59M610V will block reverse current from VOUT to VIN.

For more information about Reverse Current Blocking operation and other Silego GreenFET features please visit our [Application Notes](#) page at our website and see App Note "AN-1068 GreenFET3 Integrated Power Switch Basics".



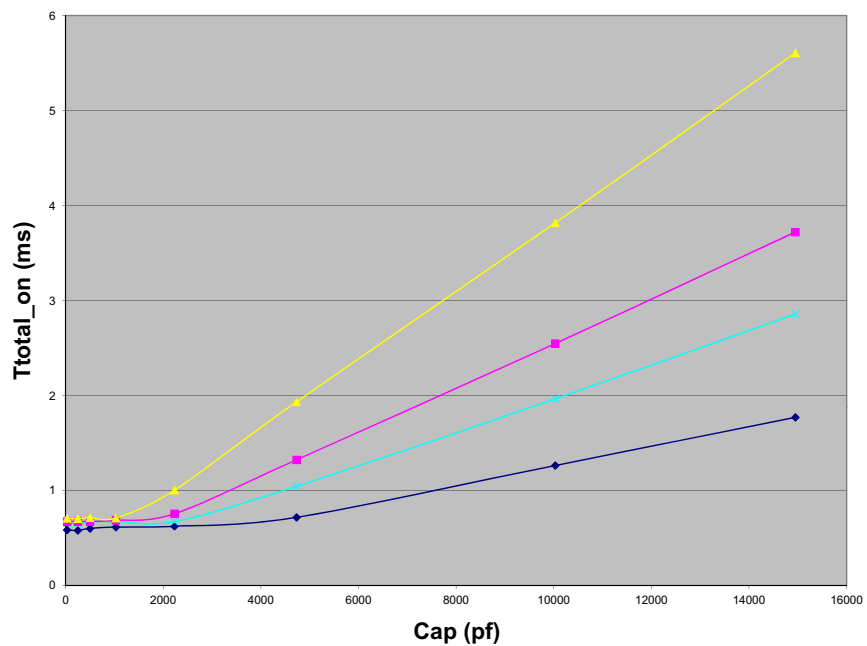
### T<sub>Total\_ON</sub> vs. CAP @ V<sub>DD</sub> = 3.3 V

SLG59M610V T<sub>Total\_ON</sub>: ON (50%) - V<sub>OUT</sub> (90%)  
V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25 °C. C<sub>L</sub> = 10 μF, I<sub>DS</sub> = 100 mA



### T<sub>Total\_ON</sub> vs. CAP @ V<sub>DD</sub> = 5.0 V

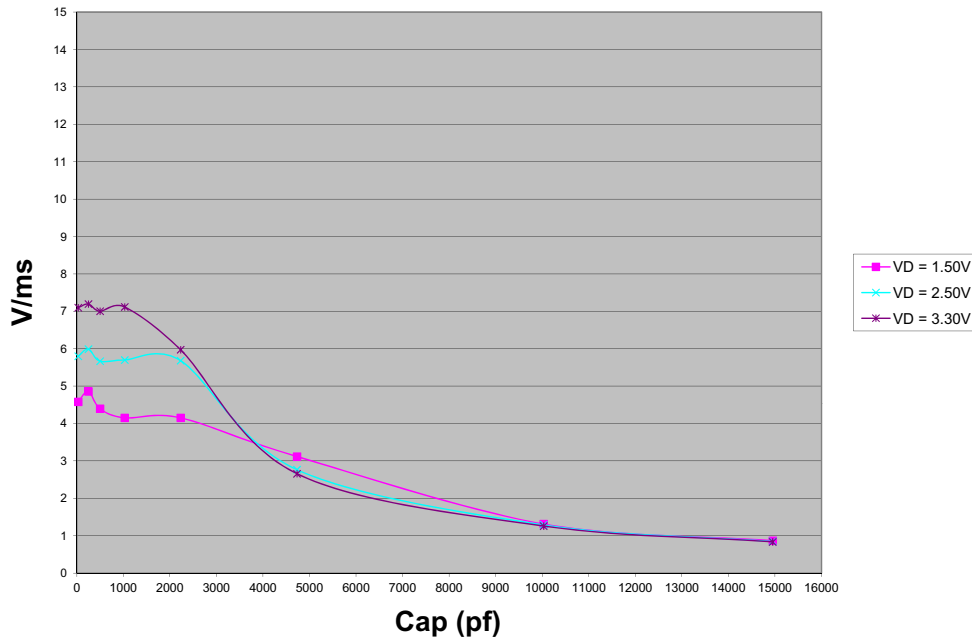
SLG59M610V T<sub>Total\_ON</sub>: ON (50%) - V<sub>OUT</sub> (90%)  
V<sub>DD</sub> = 5.0 V, T<sub>A</sub> = 25 °C. C<sub>L</sub> = 10 μF, I<sub>DS</sub> = 100 mA





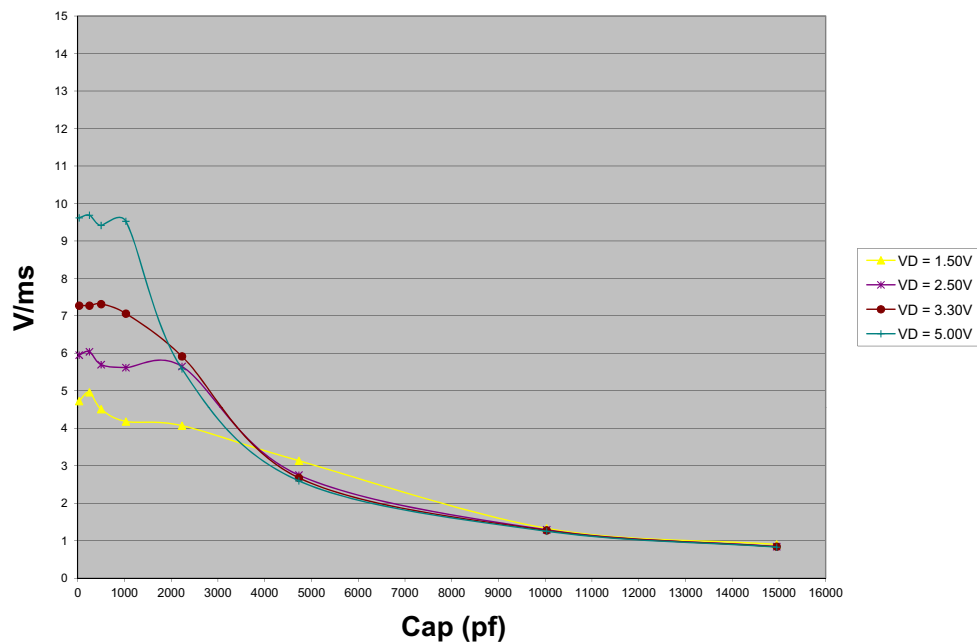
### $T_{SLEW}$ vs. CAP @ $V_{DD} = 3.3\text{ V}$

SLG59M610V  $T_{SLEW}$ :  $V_{OUT}(10\%) - V_{OUT}(90\%)$   
 $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $C_L = 10\text{ }\mu\text{F}$ ,  $I_{DS} = 100\text{ mA}$



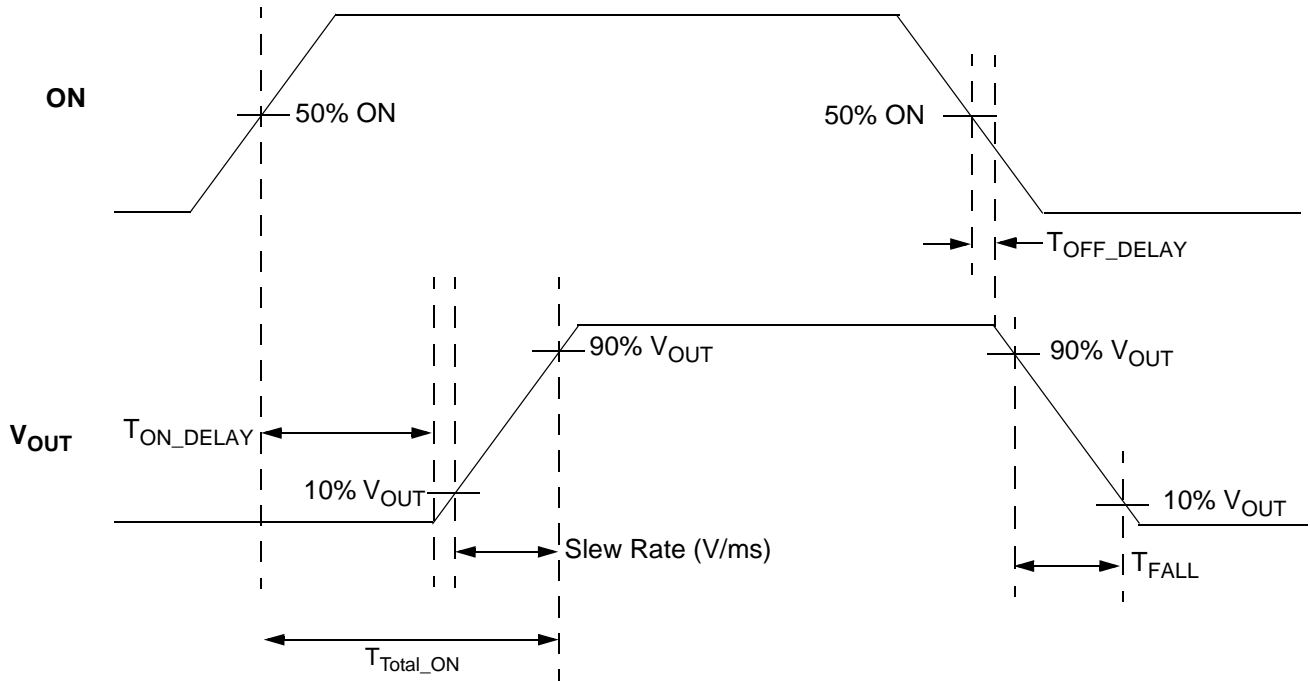
### $T_{SLEW}$ vs. CAP @ $V_{DD} = 5.0\text{ V}$

SLG59M610V  $T_{SLEW}$ :  $V_{OUT}(10\%) - V_{OUT}(90\%)$   
 $V_{DD} = 5.0\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $C_L = 10\text{ }\mu\text{F}$ ,  $I_{DS} = 100\text{ mA}$





$T_{Total\_ON}$ ,  $T_{ON\_Delay}$  and Slew Rate Measurement





Package Top Marking System Definition

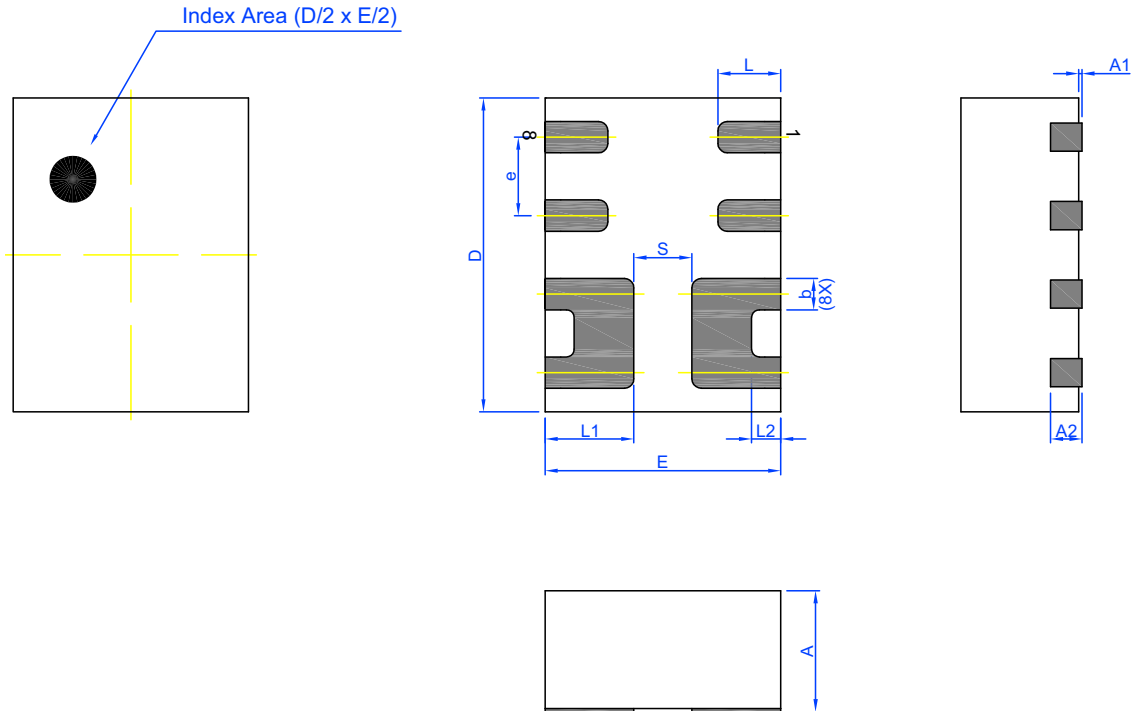






## Package Drawing and Dimensions

8 Lead TDFN Package 1.5 x 2.0 mm (Fused Lead)  
JEDEC MO-252, Variation W2015D



Unit: mm

| Symbol | Min   | Nom. | Max   | Symbol | Min      | Nom.  | Max   |
|--------|-------|------|-------|--------|----------|-------|-------|
| A      | 0.70  | 0.75 | 0.80  | L      | 0.35     | 0.40  | 0.45  |
| A1     | 0.005 | -    | 0.060 | L1     | 0.515    | 0.565 | 0.615 |
| A2     | 0.15  | 0.20 | 0.25  | L2     | 0.135    | 0.185 | 0.235 |
| b      | 0.15  | 0.20 | 0.25  | e      | 0.50 BSC |       |       |
| D      | 1.95  | 2.00 | 2.05  | S      | 0.37 REF |       |       |
| E      | 1.45  | 1.50 | 1.55  |        |          |       |       |



**Tape and Reel Specifications**

| Package Type     | # of Pins | Nominal Package Size [mm] | Max Units |         | Reel & Hub Size [mm] | Leader (min) |             | Trailer (min) |             | Tape Width [mm] | Part Pitch [mm] |
|------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
|                  |           |                           | per Reel  | per Box |                      | Pockets      | Length [mm] | Pockets       | Length [mm] |                 |                 |
| TDFN 8L FC Green | 8         | 1.5 x 2.0 x 0.75          | 3000      | 3000    | 178 / 60             | 100          | 400         | 100           | 400         | 8               | 4               |

**Carrier Tape Drawing and Dimensions**

| Package Type     | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
|                  | A0                | B0               | K0           | P0               | P1           | D0                  | E                       | F                           | W          |
| TDFN 8L FC Green | 1.68              | 2.18             | 0.9          | 4                | 4            | 1.5                 | 1.75                    | 3.5                         | 8          |



Refer to EIA-481 specification

**Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.25 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).



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**Revision History**

| Date      | Version | Change   |
|-----------|---------|--|
| 4/28/2016 | 1.03    | Added Reverse Current Blocking Description and clarified Current Limit Modes description |
| 3/9/2016  | 1.02    | Updated Ireverse   |

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