



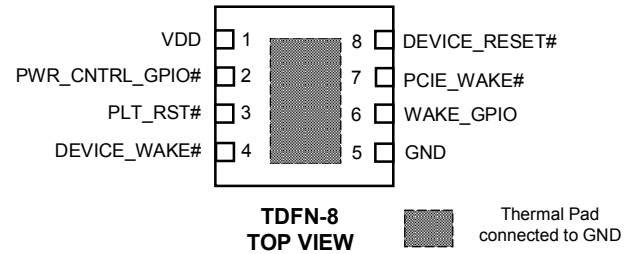
General Description

Silego GreenPAK SLG7NT4131 is a low power and small form device. The SoC is housed in a 2mm x 2mm TDFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- 3.3V Supply
- Pb-Free / RoHS Compliant
- Halogen-Free
- TDFN-8 Package

Pin Configuration

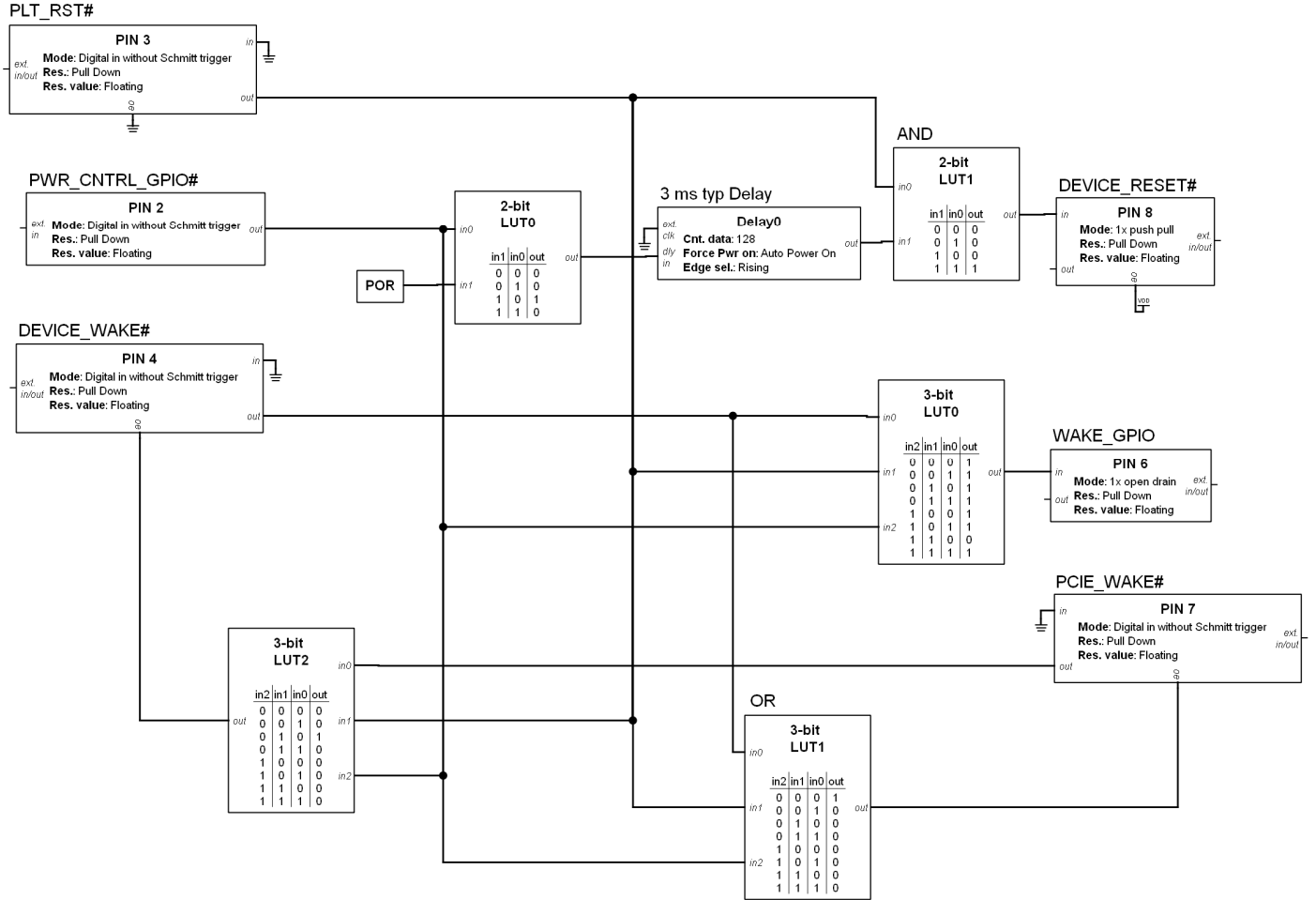


Output Summary

- 1 Output – Open Drain
- 1 Output – Push-Pull
- 1 Output – 3-State



Block Diagram





Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	3.3V Supply Voltage
2	PWR_CNTRL_GPIO#	Input	Digital Input
3	PLT_RST#	Input	Digital Input
4	DEVICE_WAKE#	Input/Output	3-State
5	GND	GND	Ground
6	WAKE_GPIO	Output	Open Drain
7	PCIE_WAKE#	Input/Output	3-State
8	DEVICE_RESET#	Output	Push-Pull
Exposed Bottom Pad	GND	GND	Ground

Ordering Options & Configuration

Part Number	Package Type
SLG7NT4131V	V = TDFN-8
SLG7NT4131VTR	VTR = TDFN-8 – Tape and Reel (3k units)



Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
V _{DD} to GND	-0.3	4.6	V
Voltage at input pins	-0.3	4.6	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

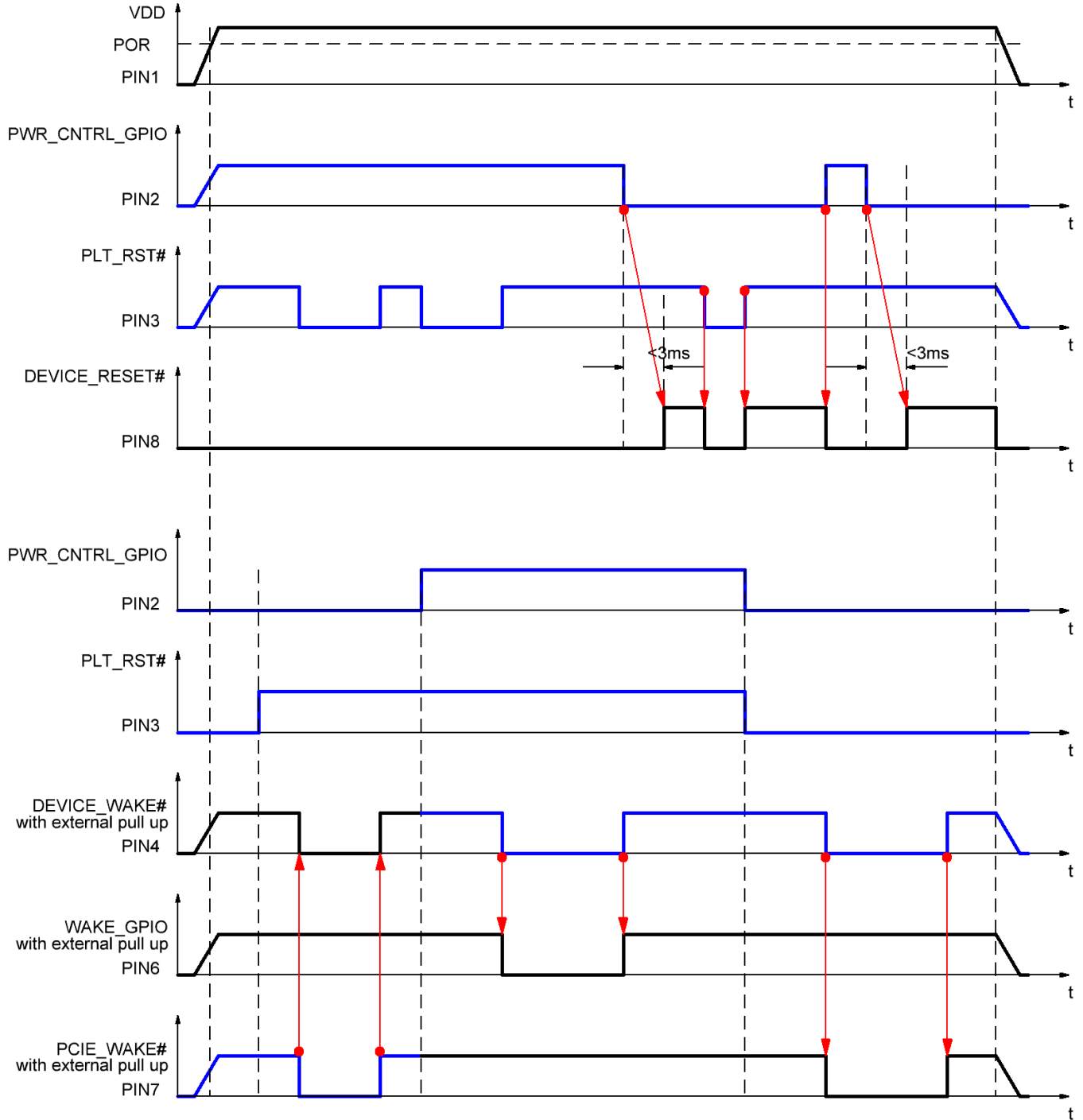
Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage		3.0	3.3	3.6	V
I _Q	Quiescent Current	Static inputs and outputs	--	0.5	--	µA
T _A	Operating Temperature		-40	25	85	°C
V _{IH}	HIGH-Level Input Voltage	Logic Input	1.7	--	--	V
V _{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.95	V
I _{IH}	HIGH-Level Input Leakage Current	Logic Input Pins; V _{IN} =3.3V	-100	--	100	nA
I _{IL}	LOW-Level Input Leakage Current	Logic Input Pins; V _{IN} =0V	-100	--	100	nA
T _{DLY0}	Delay0 Time		2.1	3	3.9	ms
V _{OH}	HIGH-Level Output Voltage	Push Pull/3-State OE=1 Output Logic High Output Level, I _{OH} =8mA	2.4	--	--	V
V _{OL}	Output Voltage Low	Push Pull/3-State OE=1 Output Logic Low Output Level, I _{OL} =8mA	--	--	0.4	V
		Open Drain, I _{OL} = 20mA	--	--	0.4	
V _O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I _{OH}	HIGH-Level Output Current	Push Pull/3-State OE=1 Output Current, V _{OH} =2.4V	--	--	8	mA
I _{OL}	LOW-Level Output Current	Push Pull/3-State OE=1 Output Current, V _{OL} =0.4V	8	--	--	mA
		Open Drain, V _{OL} = 0.4V	20	--	--	
T _{StUp}	Start Up Time	After VDD reaches 1.4V level	--	7	--	ms



Timing diagram





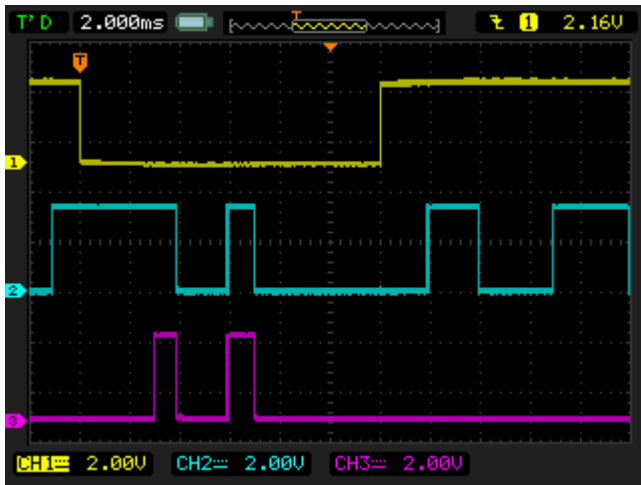
SLG7NT4131 Functionality Waveform

Channel 1 (yellow/top line) – PIN2 (PWR_CNTRL_GPIO#)

Channel 2 (blue/2nd line) – PIN3 (PLT_RST#)

Channel 3 (magenta / bottom line) – PIN8 (DEVICE_RESET#)

1. DEVICE_RESET# operation



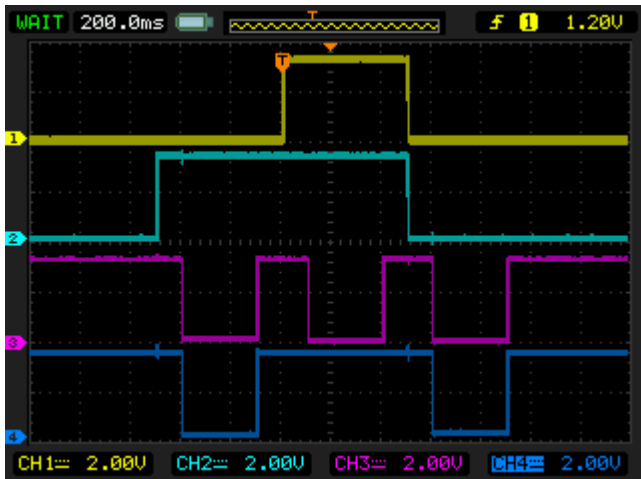
Channel 1 (yellow/top line) – PIN2 (PWR_CNTRL_GPIO#)

Channel 2 (light blue /2nd line) – PIN3 (PLT_RST#)

Channel 3 (magenta/3rd line) – PIN4 (DEVICE_WAKE#) with external 10kΩ pull up resistors

Channel 3 (blue/bottom line) – PIN3 (PCIE_WAKE#) with external 10kΩ pull up resistors

2. Bi-Directional function





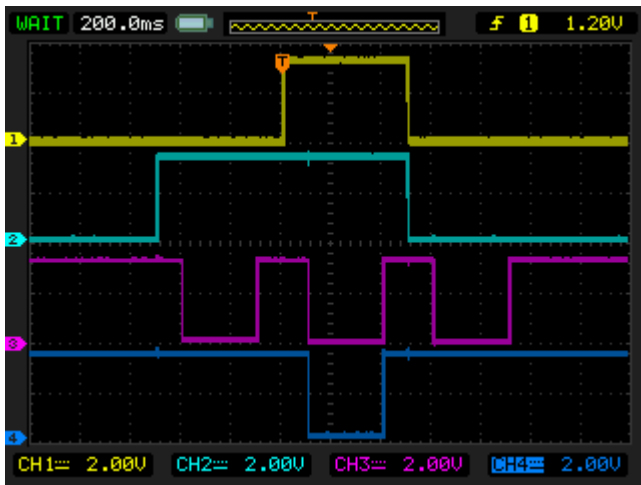
Channel 1 (yellow/top line) – PIN2 (PWR_CNTRL_GPIO#)

Channel 2 (light blue /2nd line) – PIN3 (PLT_RST#)

Channel 3 (magenta/3rd line) – PIN4 (DEVICE_WAKE#) with external 10kΩ pull up resistors

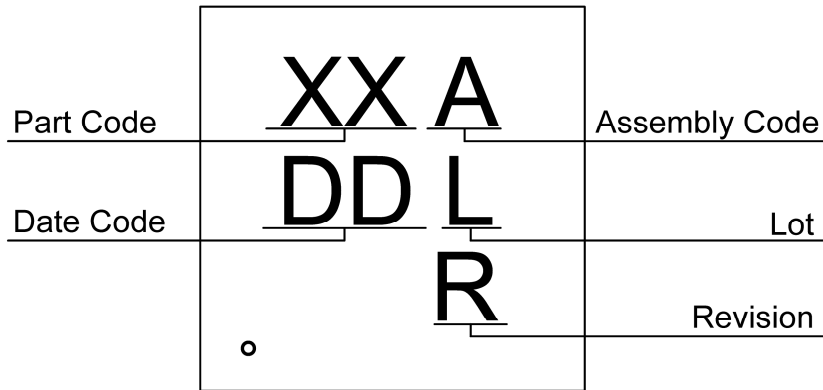
Channel 3 (blue/bottom line) – PIN9 (WAKE_GPIO) with external 10kΩ pull up resistors

3. MUX function





Package Top Marking



- XX – Part Code Field: identifies the specific device configuration
- A – Assembly Code Field: Assembly Location of the device.
- DD – Date Code Field: Coded date of manufacture
- L – Lot Code: Designates Lot #
- R – Revision Code: Device Revision

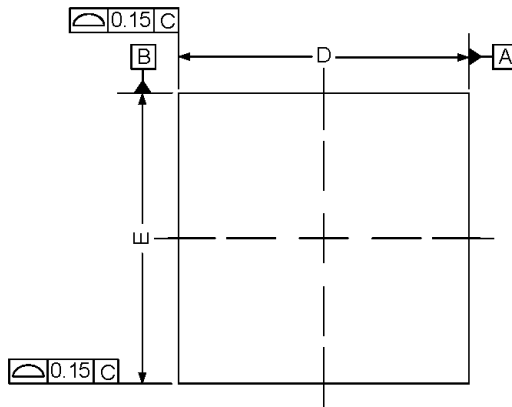
Datasheet Revision	Programming Code Number	Part Code	Revision	Date
0.20	03			11/26/2012



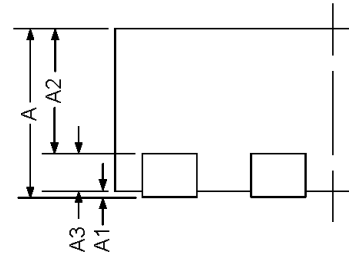
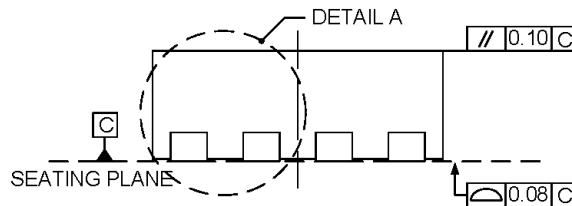
Package Drawing and Dimensions

TDFN-8 Package

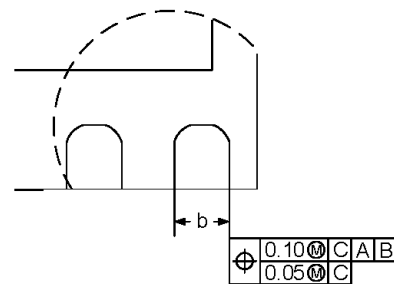
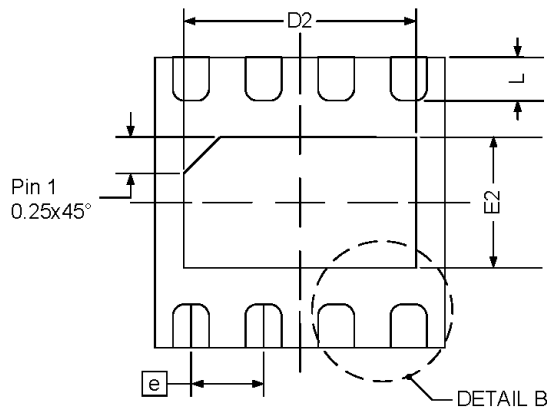
JEDEC MO-229, Variation WCCD



Symbol	Min (mm)	NOM (mm)	Max (mm)
A	0.70	0.75	0.80
A1	0.00	--	0.05
A2	--	0.55	--
A3	--	0.20	--
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.50 BSC		
L	0.20	0.30	0.40



DETAIL A



DETAIL B

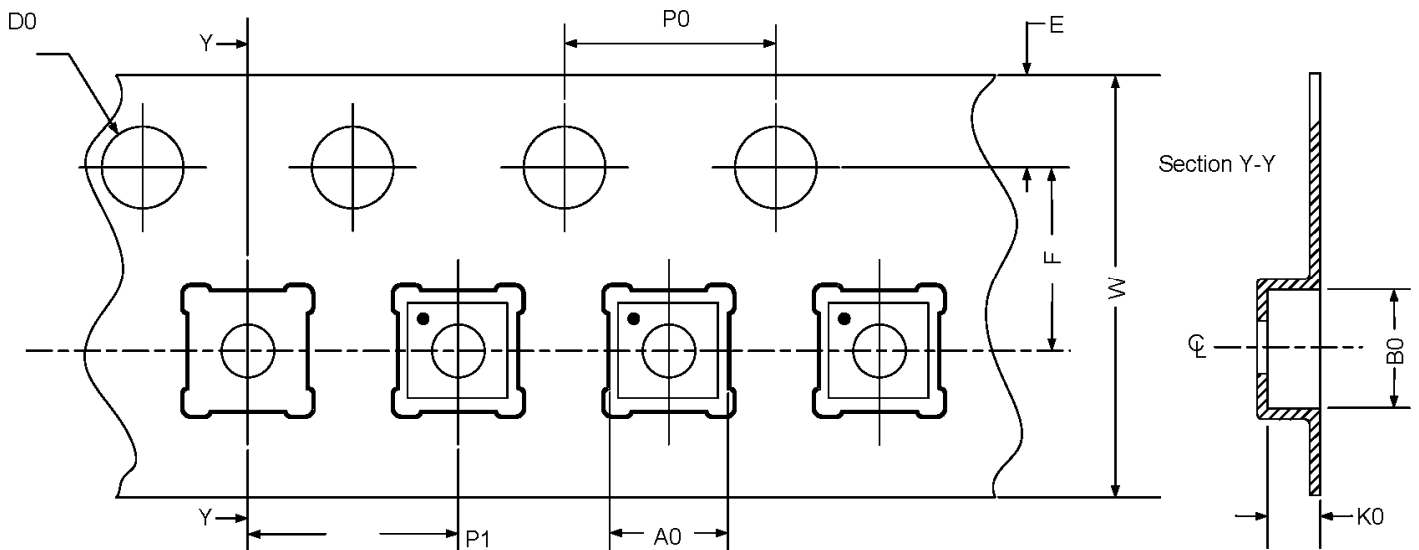


Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 8L 2x2mm Green	8	2x2x0.75	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 8L 2x2mm Green	2.3	2.3	1.05	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 mm³ (nominal). More information can be found at www.jedec.org.



Datasheet Revision History

Date	Version	Change
11/08/2012	0.1	New design
11/22/2012	0.11	Changed input PINs type to Digital Input
11/26/2012	0.20	Changed DEVICE_WAKE# and PCIE_WAKE# functionality to bi-directional



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For more information regarding Silego Green products, please visit:

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