Application Note: SM80592E

High Efficiency, 1.5MHz, 2A Synchronous Step Down Regulator

Advanced Design Specification

General Description

The SM80592E is a high efficiency 1.5MHz synchronous step down DC/DC regulator capable of delivering up to 2A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1.5MHz switching frequency.

Ordering Information

SM80592 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SM80592EIHD	DFN1.3×0.9-6	--

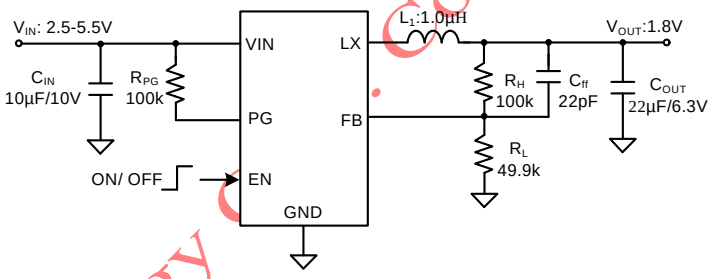
Features

- 2.5V to 5.5V Input Voltage Range
- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom) 125mΩ /75mΩ
- High Switching Frequency 1.5MHz Minimizes the External Components
- Internal Soft-start Limits the Inrush Current
- 100% Dropout Operation
- Forced PWM Operation
- Power Good Indicator
- Hic-cup for Short Circuit Protection
- Output Auto Discharge Function
- RoHS Compliant and Halogen Free
- Compact Package: DFN1.3×0.9-6

Applications

- Set Top Box
- USB Dongle
- Media Player
- Smart Phone

Typical Applications



Inductor and C_{OUT} Selection Table

V_{OUT}[V]	L [μH]	C_{OUT} [μF] 4.7	10	22	22×2
1.2	1.0		√	☆	√
	1.5		√	√	√
1.8/3.3	1.0			☆	√
	1.5			√	√

Note: '☆' means recommended for most applications.

Figure1. Schematic Diagram

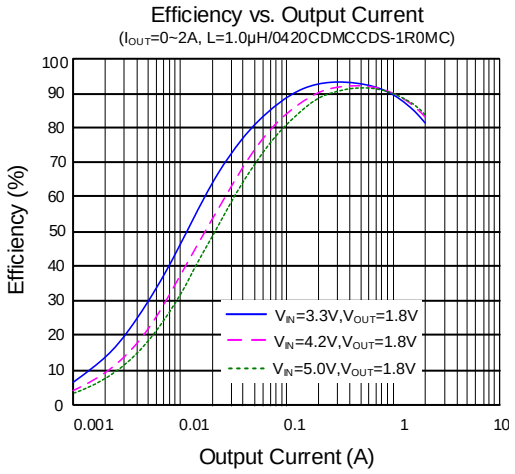
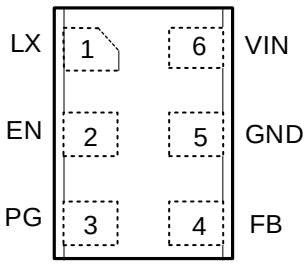


Figure2. Efficiency vs. Output Current

Pinout (Top View)



(DFN1.3×0.9-6)

Top Mark: **N2*xyz*** (device code: N2, ***x=year code, y=week code, z= lot number code)***

Pin Name	Pin Number	Pin Description
LX	1	Inductor pin. Connect this pin to the switching node of the inductor.
EN	2	Enable control. Pull high to turn on. Do not leave it floating.
PG	3	Power good indicator. Power good indicator (open drain output). Low if the output < 90% or the output >120% of regulation voltage; High otherwise. Connect a pull-up resistor to the input.
FB	4	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: $V_{OUT}=0.6\times(1+R_H/R_L)$.
GND	5	Ground pin.
VIN	6	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.

Function Block

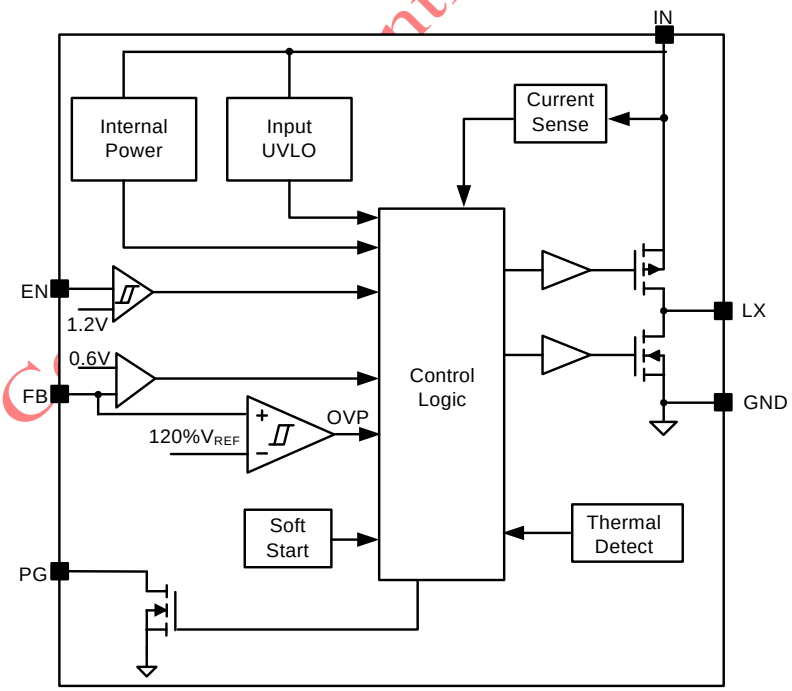


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- -0.3V to 6.0V
FB, EN, PG Voltage---------- -0.3V to V_{IN}+0.6V
LX Voltage---------- -0.3V(*1) to 6.0V(*2)
Power Dissipation, P_D @ T_A = 25℃ ---------- 1.1W
Package Thermal Resistance (Note 2)
θ_{JA} ----------90℃/W
θ_{JC} ----------20℃/W
Junction Temperature Range ---------- -40°C to 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃

(*1) LX Voltage Tested Down to -3V<40ns
(*2) LX Voltage Tested Up to +7V<40ns

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 2.5V to 5.5V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0μH, C_{OUT} = 22μF, T_A = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.5		5.5	V
Input UVLO Threshold	V_{UVLO}			2.45	2.5	V
Input UVLO Hysteresis	V_{YST}			150		mV
Shutdown Current	I_{SHDN}	V_{EN}=0V		0.1	1	μA
Feedback Reference Voltage	V_{REF}	I_{OUT}=0A, CCM	0.591	0.6	0.609	V
LX Node Discharge Resistance	R_{DIS}			50		Ω
Top FET R_{ON}	$R_{DS(ON)1}$			125		mΩ
Bottom FET R_{ON}	$R_{DS(ON)2}$			75		mΩ
EN Input Voltage High	$V_{EN,H}$		1.2			V
EN Input Voltage Low	$V_{EN,L}$				0.4	V
PG Threshold for Under Voltage Detection	$V_{PG,UVP}$			90		%
PG Low Delay Time for Under Voltage Detection	$t_{UVP,DLY}$			15		μs
PG Threshold for Over Voltage Detection	$V_{PG,OVP}$			120		%
PG Low Delay Time for Over Voltage Detection	$t_{OVP,DLY}$			15		μs
Min ON Time	$t_{ON,MIN}$			50		ns
Maximum Duty Cycle	D_{MAX}		100			%
Turn On Delay Time	$t_{ON,DLY}$	from EN high to LX start switching		0.25		ms
Soft-start Time	t_{SS}	V_{OUT} from 0% to 100%		0.75		ms
Switching Frequency	f_{SW}	I_{OUT}=0A, CCM		1.5		MHz
Top FET Current Limit	$I_{LMT,TOP}$		3			A
Bottom FET Reverse Current Limit	$I_{LMT,RVS}$		0.55		1.2	A
Output Under Voltage Protection Threshold	V_{UVP}			50		$\%V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$			10		μs
UVP Hiccup ON Time	$t_{UVP,ON}$			1.45		ms
UVP Hiccup OFF Time	$t_{UVP,OFF}$			1.45		ms
Thermal Shutdown Temperature	T_{SD}			160		℃
Thermal Shutdown Hysteresis	T_{HYS}			20		℃

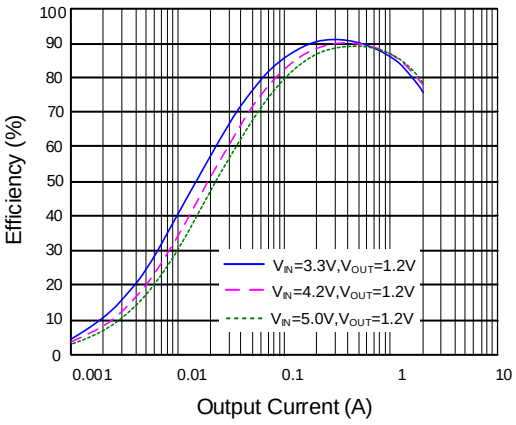
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} of SM80592E is measured in the natural convection at T_A = 25°C on a 2-oz two-layer Silergy evaluation board. Pin 1 is the case position for θ_{JC} measurement.

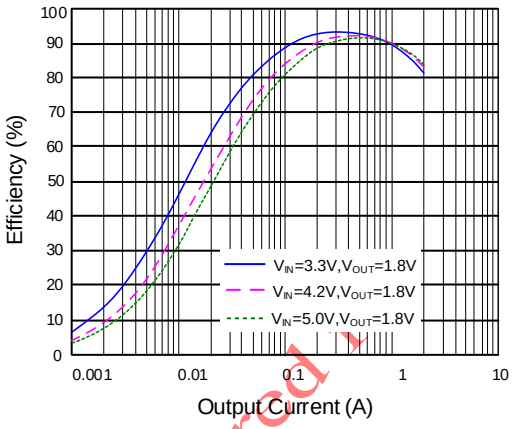
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

Efficiency vs. Output Current
(I_{OUT}=0~2A, L=1.0μH/0420CDMCCDS-1R0MC)



Efficiency vs. Output Current
(I_{OUT}=0~2A, L=1.0μH/0420CDMCCDS-1R0MC)



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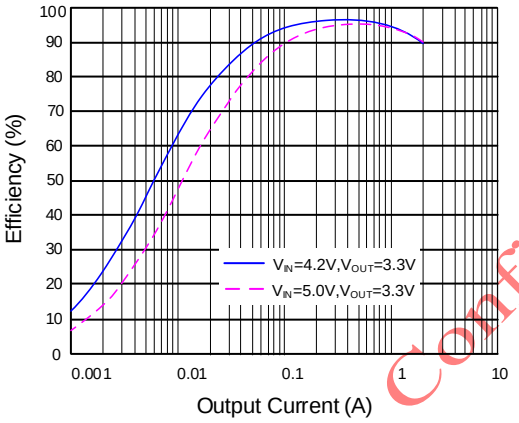
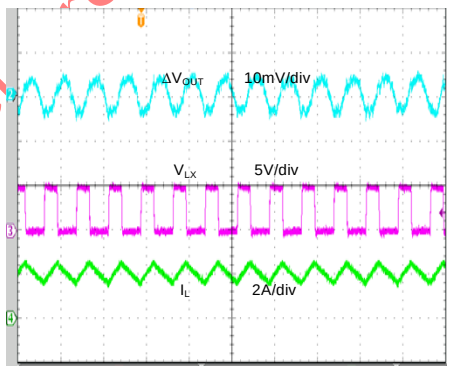
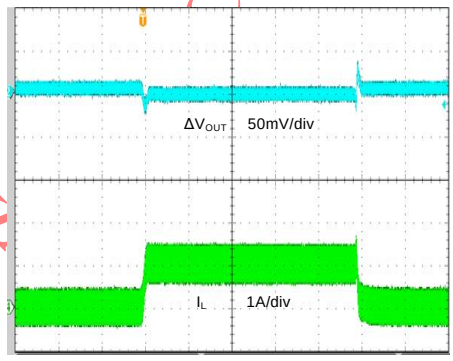


Output Ripple
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=2.0A)



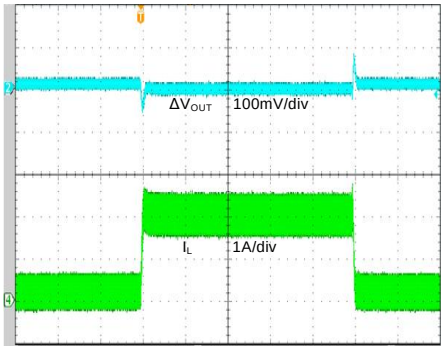
Time (1μs/div)

Load Transient
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ 1A)



Time (100μs/div)

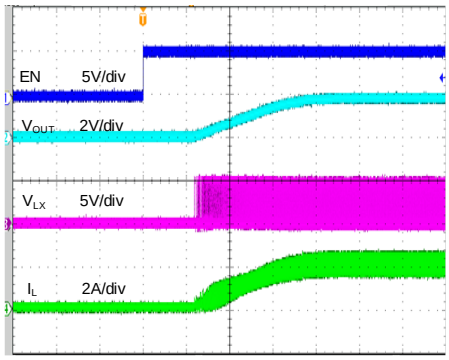
Load Transient
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0.2A ~ 2A)



Time (100μs/div)

Startup from Enable

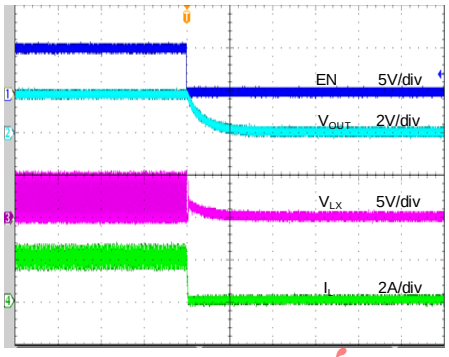
(V_{IN}=5.0V, V_{OUT}=1.8V, R_{LOAD}=0.9Ω)



Time (200μs/div)

Shutdown from Enable

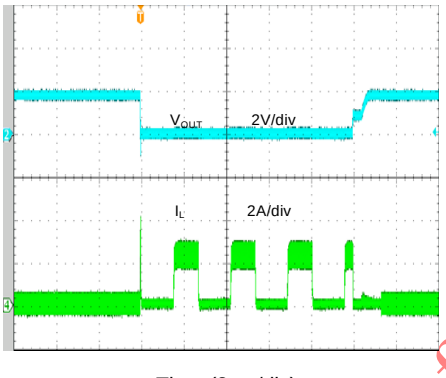
(V_{IN}=5.0V, V_{OUT}=1.8V,R_{LOAD}=0.9Ω)



Time (40μs/div)

Short Circuit Protection

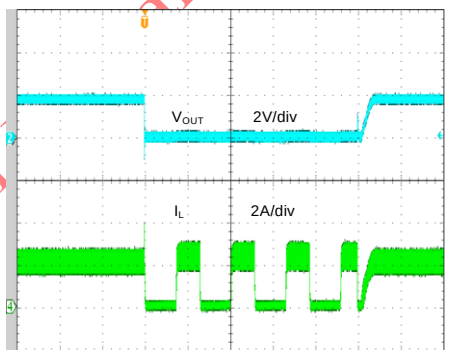
(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=0A ~ Short)



Time (2ms/div)

Short Circuit Protection

(V_{IN}=5.0V, V_{OUT}=1.8V, I_O=2A ~ Short)



Time (2ms/div)

Operation

The SM80592E is a high efficiency 1.5MHz synchronous step down DC/DC regulator capable of delivering up to 2A output current. It can operate over a wide input voltage range from 2.5V to 5.5V and integrate main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The low output voltage ripple, the small external inductor and the capacitor sizes are achieved with 1.5MHz switching frequency.

Applications Information

Because of the high integration in the SM80592E, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_H and R_L) need to be selected for the targeted application specifications.

Feedback Resistor Dividers R_H and R_L

Choose R_H and R_L to program the proper output voltage. A value of between 1kΩ and 1MΩ is recommended for both resistors. If R_L =120kΩ is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{OUT} - 0.6\,V) \times R_L}{0.6V}$$

Input Capacitor C_{IN}

A typical X5R or better grade ceramic capacitor with 6.3V rating and greater than 10μF capacitance is recommended. To minimize the potential noise problem, this ceramic capacitor should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} and the IN/GND pins.

Output Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

2) For FCCM mode converter, in order to avoid the reverse current limit (0.55A min) being triggered at open load condition, when choosing the inductance, the 1/2 inductor ripple current (ΔI) should be smaller than the reverse current limit threshold. Otherwise the output voltage will be charged to higher value. The 1/2 inductor ripple current is calculated as:

$$\frac{1}{2}\Delta I = \frac{V_{OUT}(V_{IN}-V_{OUT})}{2 \times L \times f_{SW} \times V_{IN}} \le 0.55$$

Where fsw is the switching frequency and 0.55 is the bottom FET reverse current limit. So the inductance can be calculated as:

$$L \ge \frac{V_{OUT}(V_{IN}-V_{OUT})}{1.1 \times V_{IN} \times f_{SW}}$$

3) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

4) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

Load Transient Considerations

The SM80592E regulator integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic capacitor in parallel with R_H may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.

Layout Design

The layout design of the SM80592E is relatively simple. For the best efficiency and to minimize noise problems, the following components should be placed close to the IC: C_{IN}, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable paths are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) C_{IN} must be close to pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.
3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.
4) The components R_H and R_L and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

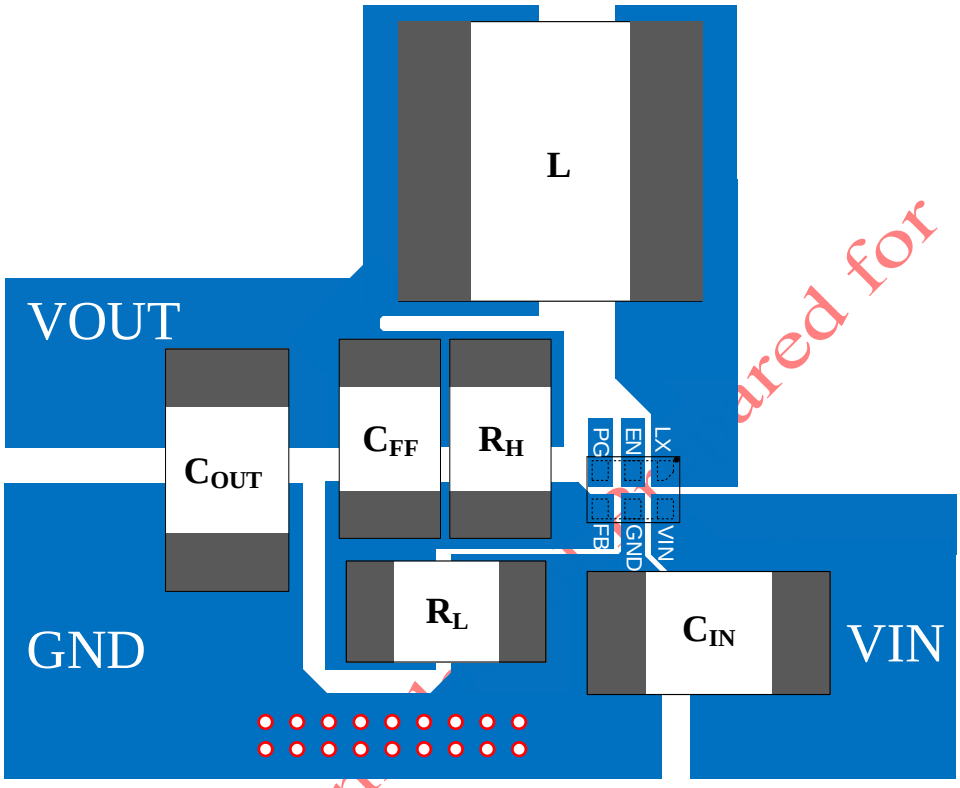
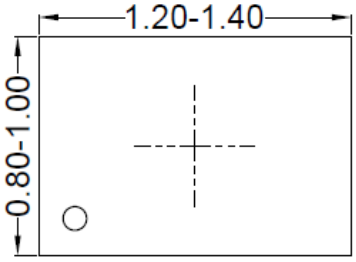
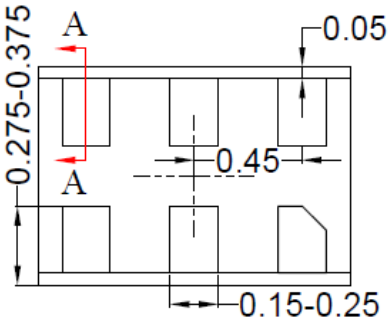


Figure4. PCB Layout Suggestion

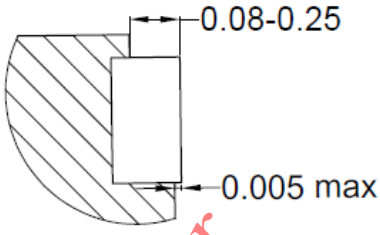
DFN1.3×0.9-6 Package Outline Drawing



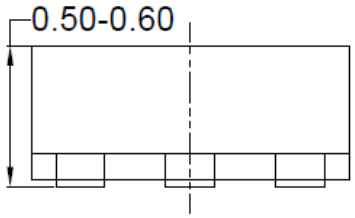
Top View



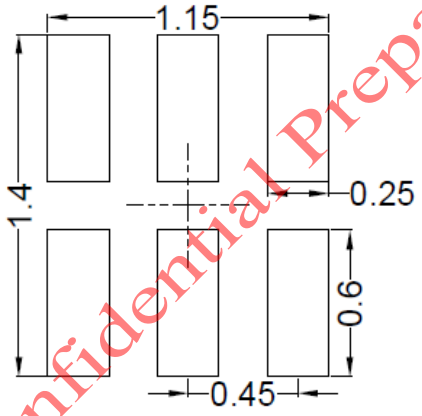
Bottom View



A-A



Front View



Recommended PCB layout
(Reference only)

Notes: 1, All dimension in millimeter and exclude mold flash & metal burr
2, center line refers chip body center

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