Application Note: SQ33065

6V to 75V Synchronous Buck Controller With Wide Duty Cycle Range

Preliminary Specification

General Description

The SQ33065 is 75V synchronous buck controller with type Ⅲ voltage mode control and feedforward. Minimum tens of nanosecond on-time facilitates large step-down ratios. The SQ33065 continues to operate when input voltage decreases to as low as 6V.
VIN over voltage protection is achieved by directly detecting VIN pin voltage to prevent output inverse charging. Cycle-by-cycle over current protection is accomplished by measuring the voltage across the low-side MOSFET or current sense resistor. Forced-PWM (FPWM) eliminates frequency variation and a selectable diode emulation lowers power consumption at light-load conditions. The switching frequency as high as 1 MHz can be set or synchronized to an external clock.

Ordering Information

SQ33065 □(□□□)

Package Code

Optional Spec Code

Ordering Number	Package type	Note
SQ33065WAQ	QFN3.5x4.5-20	

Features

- 6V to 75V Input Voltage Range
- Switching Frequency: 100kHz~1MHz
  - SYNC In/Out Capability
- Soft-Start or Voltage Tracking
- 0.8V ±1% Reference Voltage
- Minimum On-Time: 60ns typical
- Minimum Off-Time: 200ns typical
- Type Ⅲ Voltage-Mode Control With Feedforward
- High Gain-Bandwidth Error Amplifier
- Open-Drain Power Good Indicator
- Protection Features
  - Cycle-by-cycle Over current Protection
  - VIN Over voltage Protection
  - Input UVLO with Hysteresis
  - VCC and Gate UVLO Protection
  - Thermal Shutdown Protection with Hysteresis
- Compact Package: QFN3.5x4.5-20

Applications

- Telecom Power Application
- RF Power Application
- Commercial Drone Application
- DSP Power Application

Typical Application

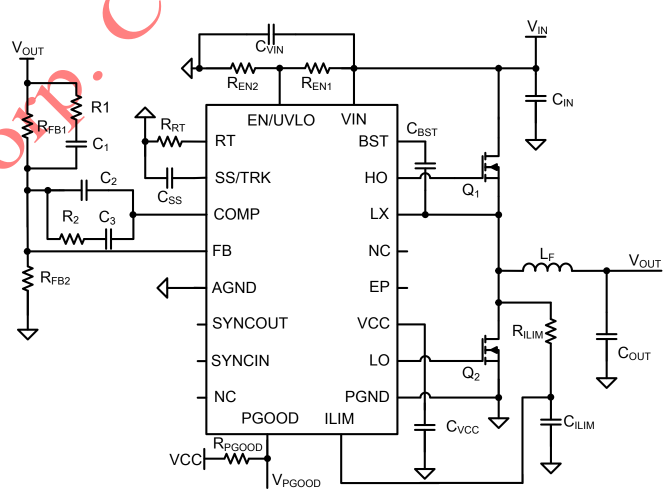
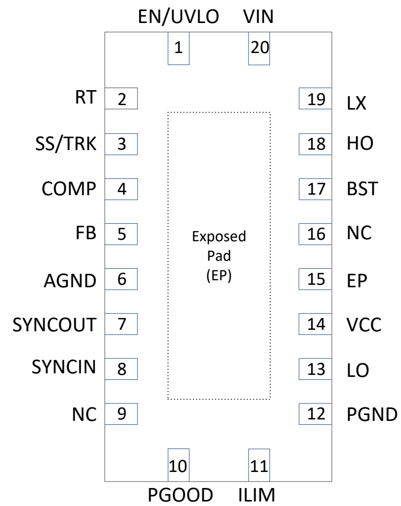


Figure 1. Typical Application

Pinout (Top View)



Top mark: **DXY*xyz*** (Device code: **DXY**, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
EN/UVLO	1	Enable and UVLO pin
RT	2	Switching frequency set pin. A resistor is connected to RT pin and set the operation frequency.
SS/TRK	3	Soft-start and voltage tracking pin. A capacitor is connected to set soft-start time.
COMP	4	Output of the internal error amplifier.
FB	5	Output Feedback Pin.
AGND	6	Analog ground.
SYNCOUT	7	Synchronization output. Logic output that provides a clock signal that is 180 °out-of phase with the high-side FET gate drive.
SYNCIN	8	Synchronization input pin.
NC	9	No electrical connection.
PGOOD	10	Power Good indicator.
ILIM	11	Current limit set and protection pin.
PGND	12	Power ground.
LO	13	Low side MOSFET gate driver pin.
VCC	14	Power supply pin.
EP	15	Exposed pad of the package.
NC	16	No electrical connection.
BST	17	Bootstrap supply for the high-side gate driver.
HO	18	High side MOSFET gate driver pin.
LX	19	Inductor pin. Connect this pin to the switching node of inductor.
VIN	20	Voltage supply for VCC LDO regulator and VIN protection pin.
EP	-	Exposed pad of the package.

Block Diagram

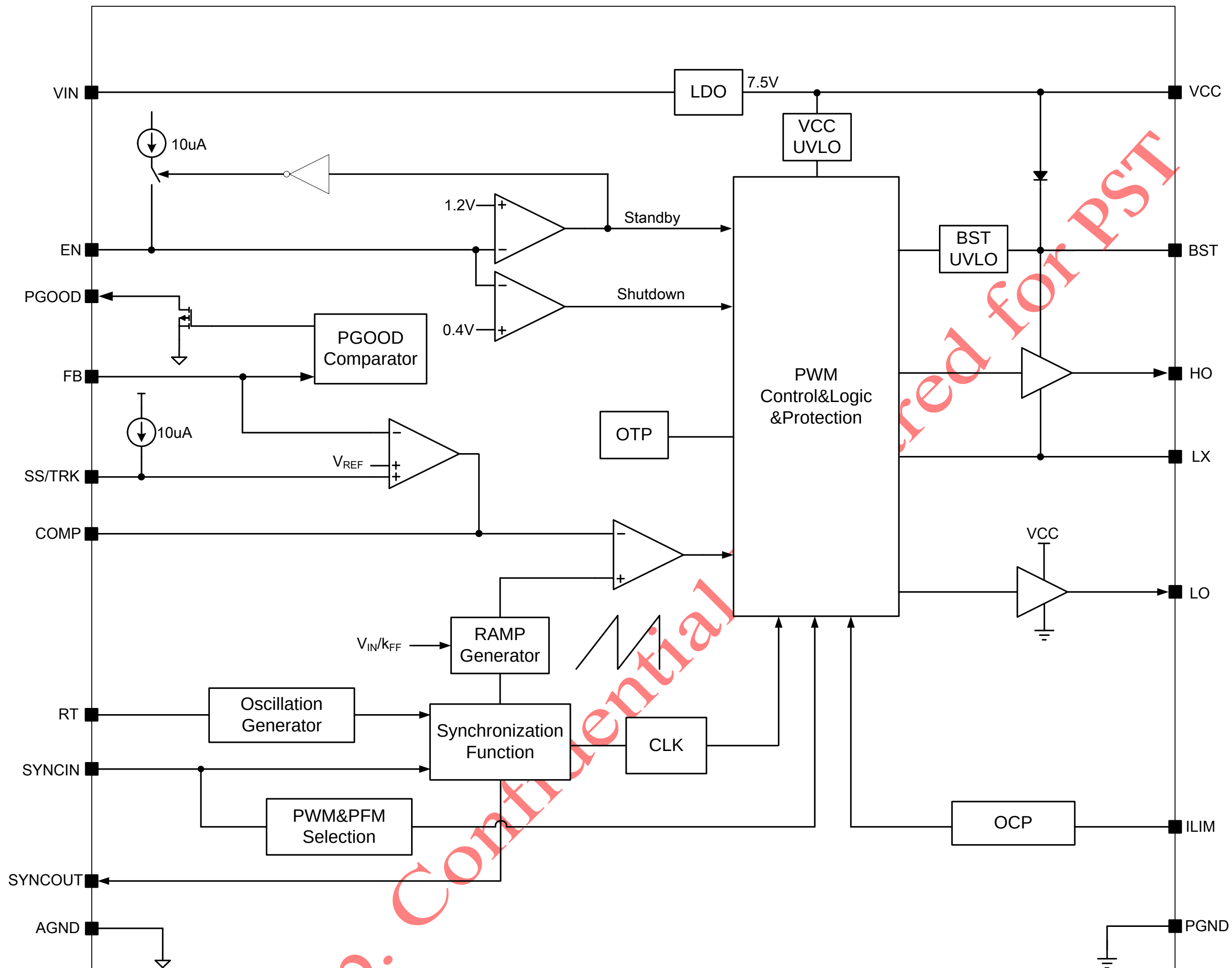


Fig 2. Simplified Block Diagram

Absolute Maximum Ratings

Absolute Maximum Voltage (Note 1)
VIN, EN/UVLO, PGOOD-- -0.3V to 95V
LX-- -1V to 95V
ILIM-- -0.3V to 95V
VCC, SYNCIN-- -0.3V to 14V
BST to LX-- -0.3V to 14V
FB, COMP, SS/TRK, RT-- -0.3V to 6V
BST -- -0.3V to 105V
Package Thermal Resistance (Note 2)
Power Dissipation max, @ TA=25 ℃ QFN3.5x4.5-20 -- 3.3W
Θ_{JA} -- 38 ℃/W
$\Theta_{JC(top)}$ -- 21 ℃/W
Junction Temperature Range -- 150 ℃
Lead Temperature (Soldering, 10 sec.) -- 260 ℃
Storage Temperature Range -- -65 ℃ to 150 ℃

Recommended Operating Conditions (Note 3)

VIN -- 6V to 75V
VCC-- 8V to 13V
Junction Temperature Range -- -40 ℃ to 125 ℃

Electrical Characteristics

(V_{IN}=48V, $V_{EN/UVLO}$=1.5V, R_{RT}=25kΩ, Tj=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Vin Input Supply& Vin Protection(OVP)						
VIN Voltage Range	V_{IN}		6		75	V
Operating Input Current, not Switching	I_{Q-RUN}	$V_{EN/UVLO}$ = 1.5V, $V_{SS/TRK}$ = 0V		1		mA
Standby Input Current	I_{Q-STBY}	$V_{EN/UVLO}$ = 1V		0.4		mA
Shutdown Input Current	I_{Q-SDN}	$V_{EN/UVLO}$ = 0V, V_{VCC}< 1V		10		µA
VIN OVP	V_{IN_OVP}			88		V
VIN OVP Hysteresis	$V_{IN\_OVP\_hys}$			6		V
VCC Regulator						
VCC Regulation Voltage	V_{VCC}	$V_{SS/TRK}$ = 0V, 9V ≤ V_{VIN} ≤ 75V,0mA < I_{VCC} ≤ 20mA		7.5		V
VIN to VCC Dropout Voltage	$V_{VCC-LDO}$	V_{IN} = 6 V, $V_{SS/TRK}$ = 0 V, I_{VCC} = 20 mA		0.25		V
VCC Short-circuit Current	I_{SC-LDO}	$V_{SS/TRK}$ = 0V, VCC = 6V		50		mA
VCC UVLO Threshold	V_{UVLO_H}	VCC rising		4.75		V
VCC UVLO Hysteresis	V_{UVLO_HYS}	Rising threshold – falling threshold		250		mV
Minimum External Bias Supply Voltage	$V_{VCC-EXT}$	Voltage required to disable VCC regulator	8			V
External VCC Input Current, not Switching	I_{VCC}	$V_{SS/TRK}$ = 0V, V_{VCC} = 13V		1		mA
Enable And Input UVLO						
Shutdown to Standby Threshold	V_{SDN}	$V_{EN/UVLO}$ rising		375		mV

Shutdown Threshold Hysteresis	$V_{SDN-HYS}$	EN/UVLO rising – falling threshold		35		mV
Standby to Operating Threshold	V_{EN}	$V_{EN/UVLO}$ rising		1.2		V
Standby to Operating Hysteresis Current	I_{EN-HYS}	$V_{EN/UVLO}$ = 1.5V		10		uA
Error Amplifier						
FB Reference Voltage	V_{REF}	FB connected to COMP		800		mV
FB Input Bias Current	$I_{FB-BIAS}$	V_{FB} = 0.8V		0		uA
COMP Output High Voltage	$V_{COMP-OH}$	V_{FB} = 0V, COMP sourcing 0.5mA		4.2		V
COMP Output Low Voltage	$V_{COMP-OL}$	COMP sinking 0.6mA		0.45		V
DC Gain	AVOL			100		dB
Unity Gain Bandwidth	GBW			6.6		MHz
Soft Start and Voltage Tracking						
SS/TRK Capacitor Charging Current	I_{SS}	$V_{SS/TRK}$ = 0V		10		uA
SS/TRK Discharge FET Resistance	R_{SS}	$V_{EN/UVLO}$ = 1V, $V_{SS/TRK}$ = 0.1V		28		Ω
SS/TRK to FB Offset	V_{SS-FB}			0		mV
SS/TRK Clamp Voltage	$V_{SS-CLAMP}$	$V_{SS/TRK}$–V_{FB}, V_{FB} = 0.8V		120		mV
POWER GOOD INDICATOR						
FB Upper Threshold for PGOOD High to Low	PG_{UTH}	% of V_{REF}, V_{FB} rising		108.00%		
FB Lower Threshold for PGOOD High to Low	PG_{LTH}	% of V_{REF}, V_{FB} falling		92.00%		
PGOOD Upper Threshold Hysteresis	PG_{HYS_U}	% of V_{REF}		3.00%		
PGOOD Lower Threshold Hysteresis	PG_{HYS_L}	% of V_{REF}		2.00%		
PGOOD Rising Filter	$T_{PG-RISE}$	FB to PGOOD rising edge		33		µs
PGOOD Falling Filter	$T_{PG-FALL}$	FB to PGOOD falling edge		33		µs
PGOOD Low State Output Voltage	V_{PG-OL}	V_{FB} = 0.9 V, I_{PGOOD} = 2 mA		170		mV
PGOOD High State Leakage Current	I_{PG-OH}	V_{FB} = 0.8V, V_{PGOOD} = 13V		50		nA
Switching Frequency						
Oscillator Frequency – 1	F_{SW1}	R_{RT} = 100kΩ		100		kHz
Oscillator Frequency – 2	F_{SW2}	R_{RT} = 25kΩ		400		kHz
Oscillator Frequency – 3	F_{SW3}	R_{RT} = 12.5kΩ		740		kHz
Synchronization Input and Output						
SYNCIN External Clock Frequency Range	F_{SYNC}	% of nominal frequency set by R_{RT}	-20%		50%	
Minimum SYNCIN Input Logic High	$V_{SYNC-IH}$		2			V
Maximum SYNCIN Input Logic Low	$V_{SYNC-IL}$				0.8	V
SYNCIN Input Resistance	R_{SYNCIN}	V_{SYNCIN} = 3 V		23		kΩ
SYNCIN Input Minimum Pulse Width	$T_{SYNCI-PW}$	Minimum high state or low state duration	50			ns
SYNCOUT High State Output Voltage	$V_{SYNCO-OH}$	$I_{SYNCOUT}$ = –1 mA (sourcing)	3			V
SYNCOUT Low State Output Voltage	$V_{SYNCO-OL}$	$I_{SYNCOUT}$ = 0.4 mA (sinking)			0.4	V
Delay from HO Rising to SYNCOUT Leading Edge	$T_{SYNCOUT}$	V_{SYNCIN} = 0 V, T_S = 1/F_{SW},F_{SW} set by R_{RT}		T_S/2 – 200		ns

Delay from SYNCIN Leading Edge to HO Rising	T_{SYNCIN}	50% to 50%		200		ns
Bootstrap Diode and Under Voltage Threshold						
Diode Forward Voltage, VCC to BST	$V_{BST-FWD}$	VCC to BST, BST pin sourcing 20 mA		0.8		V
BST to LX Quiescent Current, not Switching	I_{Q-BST}	$V_{SS/TRK}$ = 0V, V_{LX} = 48V, V_{BST} = 54V		40		uA
BST to LX under Voltage Detection	V_{BST-UV}	$V_{BST} - V_{LX}$ falling		3.2		V
BST to LX under Voltage Hysteresis	$V_{BST-HYS}$	$V_{BST} - V_{LX}$ rising		0.36		V
PWM CONTROL						
Minimum Controllable on-time	$T_{ON(MIN)}$	$V_{BST} - V_{LX}$ = 7 V, HO 50% to 50%		60		ns
Minimum off-time	$T_{OFF(MIN)}$	$V_{BST} - V_{LX}$ = 7 V, HO 50% to 50%		200		ns
Maximum Duty Cycle	DC_{100kHz}	F_{SW} = 100 kHz, 6 V $\leq V_{VIN} \leq$ 60 V		97%		
	DC_{400kHz}	F_{SW} = 400 kHz, 6 V $\leq V_{VIN} \leq$ 60 V		90%		
Ramp Valley Voltage (COMP at 0%duty cycle)	$V_{RAMP(min)}$			300		mV
PWM Feedforward Gain (VIN / VRAMP)	k_{FF}	6 V $\leq V_{VIN} \leq$ 75 V		15		V/V
OVERCURRENT PROTECT (OCP) – VALLEY CURRENT LIMITING						
ILIM Source Current, RSENSE Mode	I_{RS}	Low voltage detected at ILIM		100		uA
ILIM Source Current, RDS(on) Mode	I_{RDSON}	LX voltage detected at ILIM, T_J = 25 ℃		200		uA
ILIM Current Tempco	I_{RSTC}	R_{DS-ON} mode		4500		ppm/ ℃
ILIM Current Tempco	$I_{RDSONTC}$	R_{SENSE} mode		0		ppm/ ℃
ILIM Comparator Threshold at ILIM	$V_{ILIM-TH}$			0		mV
SHORT-CIRCUIT PROTECT (SCP) – DUTY CYCLE CLAMP						
Clamp Offset voltage – no current Limiting	$V_{CLAMP-OS}$	CLAMP to COMP steady state offset voltage 0		0.2+VIN/75		V
Minimum Clamp Voltage	$V_{CLAMP-MIN}$	CLAMP voltage with continuous current limiting 0.3 + V_{VIN}/150		0.3+VIN/150		V
HICCUP MODE FAULT PROTECTION						
Hiccup Mode Activation Delay	$C_{HICC-DEL}$	Clock cycles with current limiting before hiccup off-time activated		128		cycles
Hiccup Mode off-time after Activation	C_{HICCUP}	Clock cycles with no switching followed by SS/TRK release		8192		cycles
DIODE EMULATION						
Zero-cross Detect (ZCD) Soft-start Ramp	V_{ZCD-SS}	ZCD threshold measured at LX pin 50 clock cycles after first HO pulse		0		mV
Zero-cross Detect Disable Threshold(CCM)	$V_{ZCD-DIS}$	ZCD threshold measured at LX pin 1000 clock cycles after first HO pulse		200		mV
Diode Emulation Zero-cross Threshold	V_{DEM-TH}	Measured at LX with V_{LX} rising		0		mV

Gate Driver						
HO High-state Resistance, HO to BST	$R_{HO\text{-}UP}$	$V_{BST} – V_{LX}$ = 7 V, I_{HO} = –100 mA		1.8		Ω
HO Low-state Resistance, HO to LX	$R_{HO\text{-}DOWN}$	$V_{BST} – V_{LX}$ = 7 V, I_{HO} = 100 mA		0.7		Ω
LO High-state Resistance, LO to VCC	$R_{LO\text{-}UP}$	$V_{BST} – V_{LX}$ = 7 V, I_{LO} = –100 mA		1.8		Ω
LO Low-state Resistance, LO to PGND	$R_{LO\text{-}DOWN}$	$V_{BST} – V_{LX}$ = 7 V, I_{LO} = 100 mA		0.7		Ω
HO, LO Source Current	I_{HOH}, I_{LOH}	$V_{BST} – V_{LX}$ = 7 V, HO = LX, LO = AGND		2.3		A
HO, LO Sink Current	I_{HOL}, I_{LOL}	$V_{BST} – V_{LX}$ = 7 V, HO = BST, LO = VCC		3.9		A
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SD}	T_J rising		160		˚C
Thermal Shutdown Hysteresis	$T_{SD\text{-}HYS}$			18		˚C
Switching Characteristics						
HO, LO Rise Times	$T_{HO\text{-}TR}$_$T_{LO\text{-}TR}$	$V_{BST} – V_{LX}$ = 7 V, C_{LOAD} = 1 nF, 20% to 80%		7		ns
HO, LO Fall Times	$T_{HO\text{-}TF}$_$T_{LO\text{-}TF}$	$V_{BST} – V_{LX}$ = 7 V, C_{LOAD} = 1 nF, 80% to 20%		4		ns
HO Turn on Dead Time	$T_{HO\text{-}DT}$	$V_{BST} – V_{LX}$ = 7 V, LO off to HO on, 50% to 50%		25		ns
LO Turn on Dead Time	$T_{LO\text{-}DT}$	$V_{BST} – V_{LX}$ = 7 V, HO off to LO on, 50% to 50%		25		ns

Note 1: Stresses beyond the listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may remain possibility to affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A=25 ℃ on a high effective four layer PCB with thermal via according with JESD 51-2, -5, -7 measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

Operation Principles

Input Voltage

SQ33065 adopts wide range input voltage, varying from 6V to 75V. It also samples V_{in} value to realize V_{in}-feedforward to remove V_{in} impact on voltage loop compensation.

A resistor R_{VIN} (2.2Ω) and a capacitor C_{VIN} (100pF) is recommended to added on Vin pin to filter the noise, as shown in Fig 3.

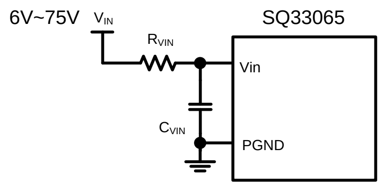


Fig 3. V_{in} Pin Connection

Power Supply VCC

In SQ33065, a LDO is connected to V_{in} to generate VCC voltage, providing internal logic power and gate driver power. If V_{in}>7.5V, output of LDO (VCC) is 7.5V. If V_{in}<7.5V, VCC will follow Vin with a small voltage drop. The maximum LDO (VCC) current ability is 50mA and it can support high power application.
Usually a 2.2uF capacitor is needed to connect VCC and PGND.

There is large power loss, (V_{in}-7.5)*I_{VCC}, on LDO if V_{in} is larger than VCC (7.5V) too much. Thus, VCC can be connected to output voltage or auxiliary voltage (8V~13V), using a diode to decrease power loss on SQ33065, as shown in Fig 4. If SQ33065 detects VCC is higher than 8V, it will turn off internal LDO to decrease power loss on it. Under this condition, a diode is also needed to avoid reverse current if V_{in}<V_{AUX} or V_{out}.

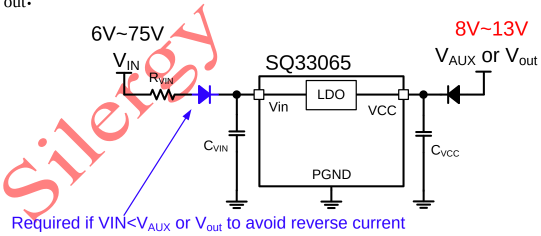


Fig 4. External VCC Supply

EN Resistor Setting

SQ33065 can set programmable EN/UVLO voltage with user-defined hysteresis.

When EN pin is higher than 0.4V and lower than 1.2V, SQ33065 enters standby mode. Under standby mode, internal LDO is working and SS/TRK pin is pull down to zero with no switching. When EN pin is higher than V_{EN_on}=1.2V, SQ33065 is in normal operation mode and a I_{EN_HYS}=10uA current flows out of EN pin to generate Hysteresis off voltage.

R_{EN1}&R_{EN2} are used to set EN/UVLO voltage. V_{in_on} is SQ33065 working V_{in} pin voltage and V_{in_off} is stopping working voltage. Use equation:

$$R_{EN1}=(V_{in\_on}-V_{in\_off})/I_{EN\_HYS}$$

$$R_{EN2}=R_{EN1}V_{EN\_on}/(V_{in\_on}-V_{EN\_on})$$

R_{EN1}&R_{EN2} can be calculated.

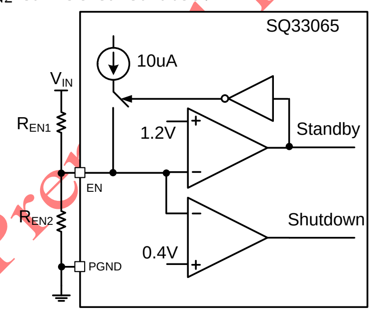


Fig 5. Programmable EN Set

In some application, a remote signal is used to control SQ33065. In this application, a resistor R_1(100Ω) is recommended to added on EN pin to avoid voltage spike caused by L_{line}.

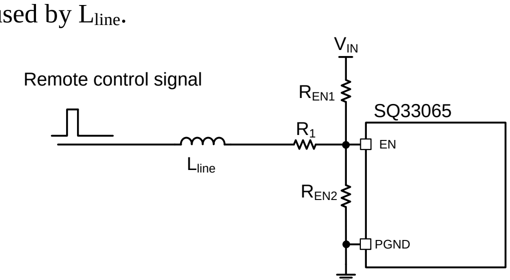


Fig 6. Remote Control Circuit

Frequency setting

A resistor is must needed on RT pin to set internal basic operation frequency, f_{RT}, as shown in Fig 7. The switching frequency range is from 100 kHz to 1 MHz.

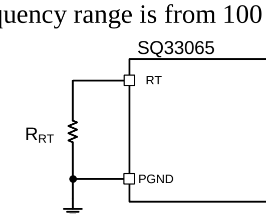


Fig 7. Frequency Set

The switching frequency, f_s, can be calculated by equation below:

$$f_s(\text{kHz}) = f_{RT}(\text{kHz}) = \frac{10^3}{0.093R_{RT}(\text{k}\Omega) + 0.14}$$

Synchronization and DCM&CCM Selection

SQ33065 can implement synchronization by SYNCIN pin. The external clock signal added on SYNCIN pin should satisfy requirements below:

Frequency range: 100 kHz~1MHz,

–20% f_{RT} ~ +50%f_{RT}

Maximum voltage amplitude: 13V

Minimum pulse width: 50ns

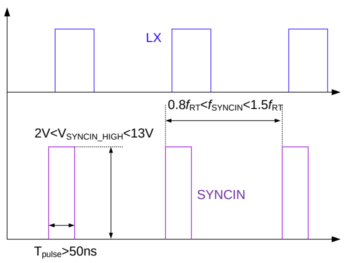


Fig 8. Synchronization Function Waveform

SYNCIN pin can also be used to select DCM (discontinuous conduction mode) & CCM (continuous conduction mode).

If SYNCIN is higher than 2V, it operates under CCM. The IC also operates under CCM if synchronization is used. Take internal resistor R_{SYNCIN} into consideration to make sure high level voltage of SYNCIN is larger than 2V if divided resistor is used here.

If SYNCIN is connected to GND, SQ33065 operates under DCM. The floating SYNCIN pin is not recommended.

When SQ33065 operates under DCM, LX will use zero crossing detection to determine if LO should be turn off. Under light load or no load condition, the power loss will decrease if SQ33065 works under DCM, however the light load transient will be slower.

DCM is also applied during start-up to prevent reverse current, whatever SYNCIN is high or low voltage. Finally, DCM changes to CCM gradually if SYNCIN is high level or it operates under synchronization.

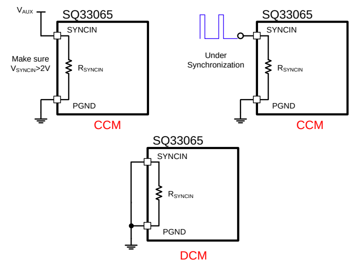


Fig 9. CCM&DCM Selection

Soft Start&Tracking Function

When EN pin is above 1.2V, a 10uA current flows out of SS/TRK pin to charge external capacitor. This can control amplifier's reference voltage to program soft start time. The C_{SS} can be set by using the equation:

$$C_{SS} = \frac{t_{SS} I_{SS}}{V_{REF}}$$

t_{SS} is set soft start time, I_{SS}=10uA, V_{REF}=0.8V. Minimum C_{SS} capacitance is 2.2nF.

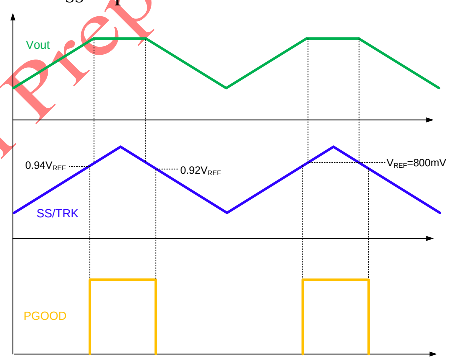


Fig 10. Tracking and PGOOD Function Waveform

Customers can also connect a signal to SS/TRK pin to let output voltage track the added control signal. The typical waveform of V_{out}, SS/TRK, PGOOD is shown in Fig 10.

The control signal can be divided output voltage of master or a voltage source. The circuit of two tracking configurations following a master is shown in Fig 11.

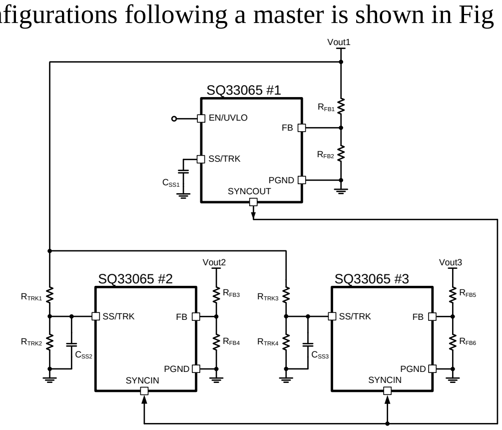


Fig 11. Tracking Function Circuit

PGOOD Indicator

PGOOD pin is used to reflect output voltage state, by detecting FB voltage as shown in Fig 10. When the FB voltage exceeds 94% V_{REF}, with 2% hysteresis, the switch S_{PGOOD} turns off and when the FB voltage exceeds 108% V_{REF}, the switch S_{PGOOD} turns on, pulling PGOOD low, with 3% hysteresis. The switch S_{PGOOD} turn on or turn off delay time is 25 µs.

PGOOD pin can be used as shown in Fig 12. PGOOD pin should be connected to a resistor, 10kΩ~100kΩ, and pull up to a DC voltage, usually VCC pin. When PGOOD is pull up to the DC voltage, it means output has been established. Then, PGOOD can be connected to next system to indicator if V_{out} has been established.

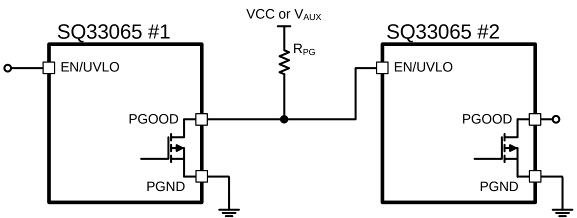


Fig 12. PGOOD Controlling EN/UVLO

Type-III Voltage Mode Control (COMP&FB)

SQ33065 adopts voltage-mode control, Type-III circuit, compensation with feed-forward, k_{FF}=15V/V. It has two zeros and three poles to compensate zeros and poles caused by the systems. COMP pin is output of error amplifier, of which gain and bandwidth are both extremely large. FB pin is output voltage feed back pin, connected to negative input of the amplifier. The positive input of the amplifier is precise 800mV reference voltage. The detailed design method will be presented later.

Gate Driver

SQ33065 has at least 2A source current and 3A sink current, so it can be used in large current application, where Q_g is large or even two MOSFETs are used in parallel. The large current ability means fast turn on&turn off speed and switching loss can be reduced.

The maximum voltage of LO is VCC voltage and VCC supplies the LO power. VCC also charges a external 0.1uF BST_LX capacitor, through integrated bootstrap diode, which supplies HO power. Thus, the maximum voltage of HO is VCC minus $V_{BST\text{-}FWD}$ and $V_{BST\text{-}FWD}$ is bootstrap diode voltage drop.

Adaptive dead time is used in switching interval to avoid shoot through.

Programmable OCP

SQ33065 can set programmable OCP as circuit below. In Fig 13(a), voltage drop on R_{dson} is sampled, without any extra power loss, while in Fig 13(b), a sampling resistor is needed and voltage across it is sampled. SQ33065 compares the ILIM pin voltage with internal reference each duty cycle to determine if I_L exceeds set OCP threshold.

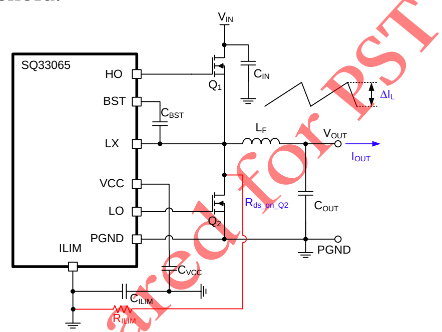


Fig 13(a). Programmable OCP Rds_on Mode

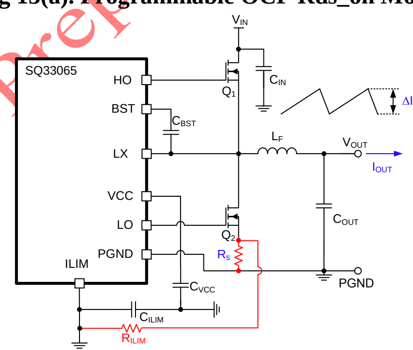


Fig 13(b). Programmable OCP Rsense Mode

Under different implementations, OCP current I_{ILIM} through ILIM pin is different. $I_{LIM\_Rds\_on}$=200uA @25℃, which incorporates a TC of +4500 ppm/℃, in Fig 13(a) R_{ds_on} mode and I_{LIM_RS}=100uA and it will not change @-25℃~125℃ in Fig 13(b) R_{sense} mode. A resistor R_{ILIM} is connected between ILIM pin and sampling point. The R_{ILIM} can be set as equation below:

$$R_{ILIM} = \begin{cases} \dfrac{(I_{OUT} - \Delta I_L / 2) R_{ds\_on\_Q2}}{I_{LIM\_Rds\_on}}, & R_{ds\_on} \text{ mode} \\[2ex] \dfrac{(I_{OUT} - \Delta I_L / 2) R_S}{I_{LIM\_RS}}, & R_{sense} \text{ mode} \end{cases}$$

In order to avoid voltage ring impact, a capacitor C_{ILIM} connected between ILIM to PGND is essential. Approximately 6 ns of $R_{ILIM} \cdot C_{ILIM}$ is recommended.

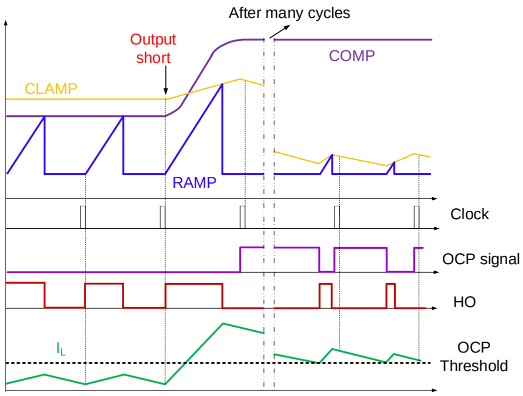


Fig 14. OCP Logic

Fig 14 shows the OCP logic, CLAMP is internal signal which is used to limit large inductor current when output shorts, RAMP is PWM waveform. If the over current condition that OCP signal is high level when SQ33065 detects inductor current, lasts for 128 continuous clock cycles, OCP is triggered and SS is pulled low for 8192 clock cycles. Then SQ33065 enters auto recovery state.

Thermal Shutdown

SQ33065 monitors die temperature under normal operating mode. Once die temperature rises above internal OTP threshold, IC will stop switching. If die temperature is lower than hysteresis temperature, SQ33065 enters auto recovery state.

Power Stage Design Guide

Inductor calculation

Choose the inductance to provide the desired ripple current ΔI_L, between 30% and 40% of the maximum DC output current at nominal input voltage. The inductance is calculated as:

$$L_F = \frac{(V_{in} - V_{out})V_{out}}{\Delta I_L f_s V_{in}}$$

The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency. When SQ33065 operates under maximum or large duty, voltage drop on DCR of the inductor should be considered. Check the datasheet of the inductor whether its saturation current is higher than inductor peak current under OCP.

Output Capacitors

Output capacitor C_{OUT} filters the inductor ripple current and stores the energy supplying to the load. Therefore, both steady state ripple and transient requirements must be taken into consideration when select the capacitor. Capacitance is selected as equation below:

$$C_{out} \geq \frac{\Delta I_L}{8 f_s \sqrt{\Delta V_{out}^2 - (R_{ESR}\Delta I_L)^2}}$$

$$C_{out} \geq \frac{L_F \Delta I_{out}^2}{(V_{out} + \Delta V_{overshoot})^2 - V_{out}^2}$$

Tantalum and electrolytic capacitors supply a large bulk capacitance to store energy while ceramic capacitors are usually added due to its low ESR to reduce the output voltage ripple.

Input Capacitors

Input capacitor C_{in} is necessary to reduce input voltage ripple. X5R or X7R ceramic capacitors are recommended to provide low input impedance. The input capacitance is calculated as below:

$$C_{in} > \frac{D(1-D)I_{out}}{f_s(\Delta V_{in} - R_{ESR} I_{out})}$$

Power MOSFET

MOSFET selection is important in DCDC converter design. The low R_{dson} of MOSFET can bring low conduction loss to achieve high efficiency. While low R_{dson} MOSFET has large Q_g, which leads to more switching loss. It is a trade-off to select suitable R_{dson} and Q_g. Low thermal resistance is also needed and it can make power loss result in low temperature. Besides, maximum current and voltage should be satisfied.

MOSFET power losses are calculated below, where suffixes 1 and 2 represent high-side and low-side MOSFET parameters, respectively.

1. Conduction loss

$$P_{cond}=D(I_{out}^2+\Delta I_L^2/12)R_{dson1}+(1-D)(I_{out}^2+\Delta I_L^2/12)R_{dson2}$$

2. Switching loss

$$P_{sw}=V_{in} f_s (I_{Lmin}t_r+I_{Lmax}t_f)$$

t_r and t_f are LX rising and falling time. Only high-side MOSFET switching loss is calculated and low-side MOSFET switching loss is negligible.

3. Gate driver loss

$$P_{gate}=V_{CC} f_s (Q_{g1}+Q_{g2})$$

The approximate calculation of gate driver loss is based on the MOSFET internal gate resistance, the added series gate resistance and the SQ33065 internal driver resistance.

4. Output charge loss

$$P_{coss}=f_s(V_{in}Q_{oss2}+E_{oss1}-E_{oss2})$$

E_{oss1} is the energy stored in C_{oss1} and dissipated at turn on, but this is offset by the stored energy E_{oss2} on C_{oss2}.

5. Body diode conduction loss

$$P_{diode\_cond}=V_{F2} f_s (I_{Lmin}t_{dt1}+I_{Lmax}t_{dt2})$$

V_{F2} is body diode conduction voltage. Only low-side MOSFET body diode conduction loss is calculated.

6. Body diode reverse recovery loss

$$P_{RR}=V_{in}f_sQ_{RR2}$$

Q_{RR2} is low-side MOSFET body diode reverse recovery charge.

Voltage Loop Design Guide

Control Loop Compensation Design

SQ33065 use voltage-mode control, Type-III circuit, with V_{in} feedback forward, where two zeros and three poles are used in compensation. The control circuit is shown below.

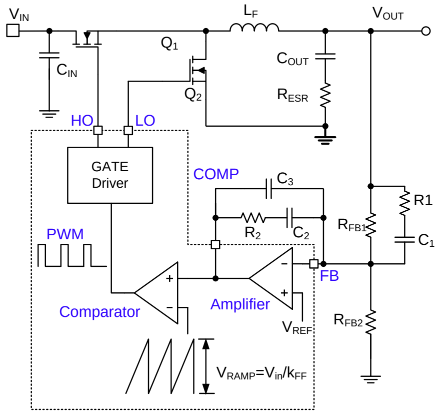


Fig 15. Control Loop Circuit

One pole is located at the origin to achieve high DC gain. The second pole is added on $1/2f_s$ to suppress high frequency noise. The last pole is usually located at f_{ESR}, which is caused by ESR of output capacitor.

The two zeros are used to compensate LC resonance poles. The added poles and zeros are shown in picture below.

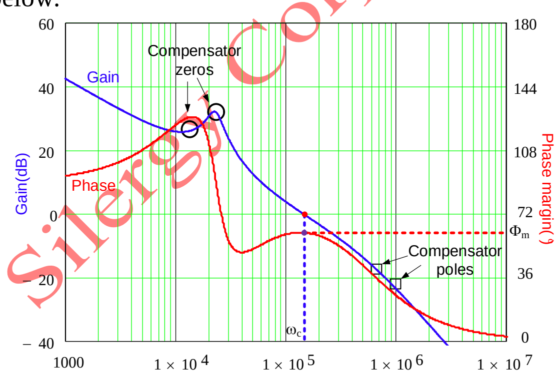


Fig 16. Open Loop Gain and Phase Margin

In Buck converter, the normal mathematic transfer function of power stage is shown below.

$$G_{vd}(s)=\frac{V_{in}(1+\frac{s}{\omega_{ESR}})}{1+\frac{s}{Q_0\omega_0}+\frac{s^2}{\omega_0^2}}$$

Where

$$\omega_0=\frac{1}{\sqrt{L_FC_{out}}}$$

$$\omega_0=\frac{1}{R_{ESR}C_{out}}$$

$$Q_0=\frac{R_o}{\sqrt{L_F/C_{out}}}$$

Following compensation in control loop circuit, there is a PWM comparator. The amplitude of the PWM is V_{in}/k_{FF} , V_{in} feed forward, and finally, the stability has nothing with V_{in}. The transfer function of PWM comparator is shown below:

$$G_M(s)=\frac{1}{V_{RAMP}}=\frac{k_{FF}}{V_{in}}$$

The compensator transfer function is shown below:

$$G_c(s)=K_{mid}\frac{(1+\frac{\omega_{z1}}{s})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}$$

The small signal open loop response of buck converter is the product of power stage, compensator and PWM comparator transfer functions:

$$T_{vd}(s)=G_{vd}(s)G_M(s)G_c(s)$$

$$=K_{mid}\frac{(1+\frac{\omega_{z1}}{s})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})}\frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q_0\omega_0}+\frac{s^2}{\omega_0^2}}k_{FF}$$

In Fig 15, R_{FB1}&R_{FB2} are divider resistor and they determine the desired V_{out}.

Here provides a simplified compensator parameters design method:

1. R_{FB2}&R_{FB2} calculation:

RFB1 is selected for 1kΩ~5kΩ and R_{FB1} can be calculated:

$$R_{FB1}=R_{FB2}(V_{out}/V_{REF}-1)$$

2. Select ω_c and K_{mid} calculation

ω_c is crossing radian frequency and usually:

$$\omega_c=1/10\sim1/5\,\omega_s$$

K_{mid} (mid-frequency gain) can be calculated approximatively:

$$K_{mid}=\omega_c/(\omega_0k_{FF})$$

k_{FF}=15 is SQ33065 feedforward parameter.

R_2 can be calculated:

$$R_2=K_{mid}R_{FB1}$$

3. ω_{z1}&ω_{z2} calculation

These zeros are needed to cancel the LC oscillation peak and their value can be selected as below:

$$\omega_{z1}=0.5\omega_0,\ \omega_{z2}=\omega_0$$

Usually output capacitor has serial parasitic resistor and a zero is located at $R_{ESR}C_{out}$. A pole is needed here to reduce ESR impact. Final pole is usually located at $\omega_s/2(\omega_s=2\pi f_s)$ to restrain switching frequency influence:

$$\omega_{p1}=\omega_{ESR},\ \omega_{p2}=\omega_s/2$$

4. Compensator resistor and capacitor calculation

Once poles and zeros' value are determined, in compensator, these poles and zeros are fabricated by the resistor and capacitors and can be calculated as below:

$$C_2=1/\omega_{z1}R_2,\ C_3=1/\omega_{p2}R_2$$

$$C_1=1/\omega_{z2}R_{FB1},\ R_1=1/\omega_{p1}C_1$$

Referring to Fig 15, the phase margin, Φ_M, is the difference between the loop phase at ω_c and –180°. Usually, 50° to 70° Φ_M in design is considered ideal.

EMI Filter Design Guide

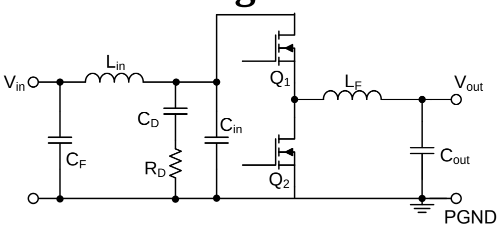


Fig 17. Buck EMI Filter

The EMI filter design steps are as follows:

1. Calculate the required attenuation of the EMI filter at the switching frequency

$$Attn = 20\log\left(\frac{I_{peak}}{\pi^2 f_s C_{in}} \cdot 1\mu V\right)\sin(\pi D_{max}) - V_{max}$$

Vmax is the allowed dBμV noise level for the applicable EMI standard.

2. Input filter inductor L_{IN} is usually selected between 1 ~10 μH. It can be lower to reduce losses in a high current design;

3. Calculate input filter capacitor C_F

$$C_F = \frac{1}{L_{IN}}\left(\frac{10^{\frac{|Attn|}{40}}}{2\pi f_s}\right)^2$$

The output impedance of the EMI filter must be extremely small and the EMI filter does not affect the loop gain of the buck converter. The resonant frequency of the EMI filter is:

$$f_{res\_filter} = \frac{1}{2\pi\sqrt{L_{IN}C_F}}$$

R_D is used to reduce the peak output impedance at f_{res_filter} to reduce EMI filter impact on loop gain of the buck converter. C_D blocks the DC component of the input voltage to avoid power loss in R_D. C_D should have lower impedance than R_D at f_{res_filter} with a capacitance value greater than that of the input capacitor C_{IN}:

$$C_D \geq 4C_{IN}$$

Select the damping resistor R_D:

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}}$$

Layout Considerations

A proper PCB design must follow the below guidelines:

(a) To achieve a good EMI performance and to reduce the switching frequency voltage ripples, the output of the EMI rectifier should be connected to the C_{IN} capacitor first, then to the switching circuit.

(b) The inductor should be connected to the C_{OUT} capacitor first, and then to the load for a small output voltage ripples.

(c) The LX switching node being short, wide and small is benefit to EMI. The parasitic inductor here should be as small as possible to decrease LX peak ringing amplitude, which may be exceed maximum voltage stress of MOSFET. If the LX peak ringing amplitude is excessive, the snubber between LX and GND is needed

(d) Input capacitors, output capacitors, inductors and MOSFETs are placed on the top side of the PCB for a good cooling environment.

(e) The circuit loop of all switching circuit should be kept as small as possible to decrease disturbance as shown in Fig. 18: High-side&Low-side power loop, High-side&Low-side driver circuit loop.

(f) C_{BST} and C_{VCC} should be as close as possible to the IC to minimize the loop. High-side&Low-side driver circuit loops are also should be small. Placing a 2Ω to 10Ω resistor in series with CBST to slows down high-side MOSFET turn on speed can reduce the LX peak ringing amplitude.

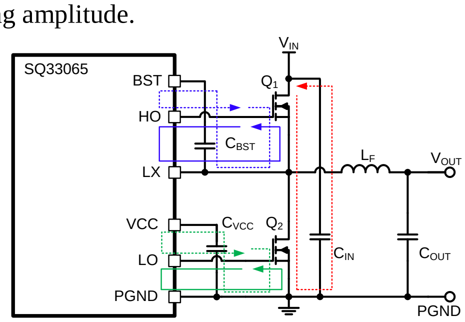


Fig 18. Switching Loop in Buck

(g) Small signal ground should be different part with power ground to avoid noise from power stage. COMP, FB, RT, ILIM, SS/TRK, SYNCIN pin should be away from LX, BST, HO, LO pin to avoid disturbances. Use internal layer as ground plane if possible.

(h) The distance between LX and ILIM pin where ILIM resistor is set should be as close as possible.

(i) Connect the PGND pin to the system ground plane using an array of vias under the exposed pad. Connect the PGND directly to the input and output capacitors. \

IC Layout Reference

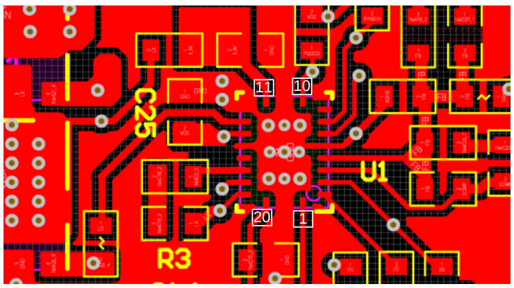
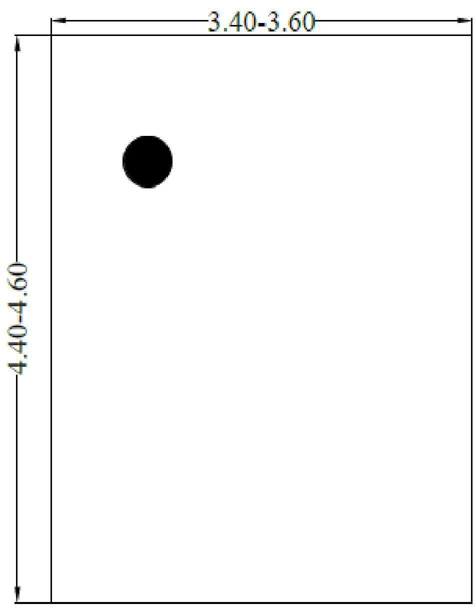
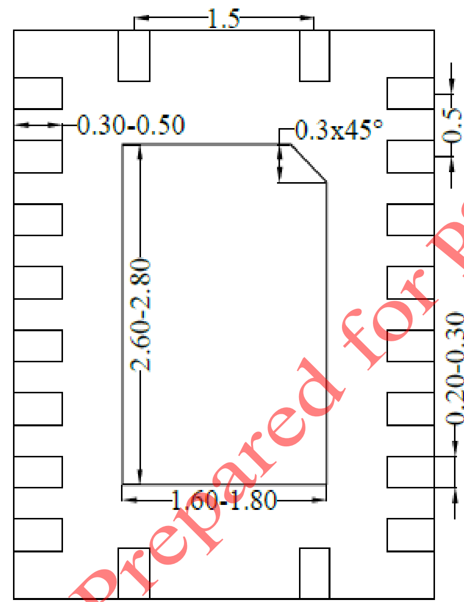


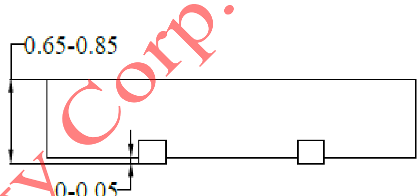
Fig 19. SQ33065 Layout Reference

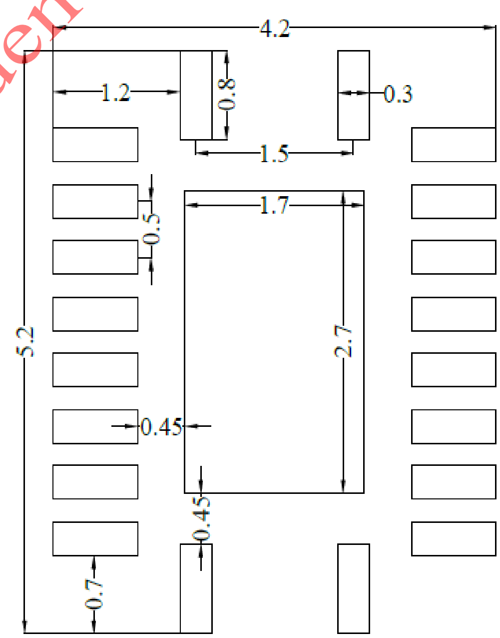
QFN3.5×4.5 -20 Package Outline & PCB Layout Design





Top View **Bottom View**



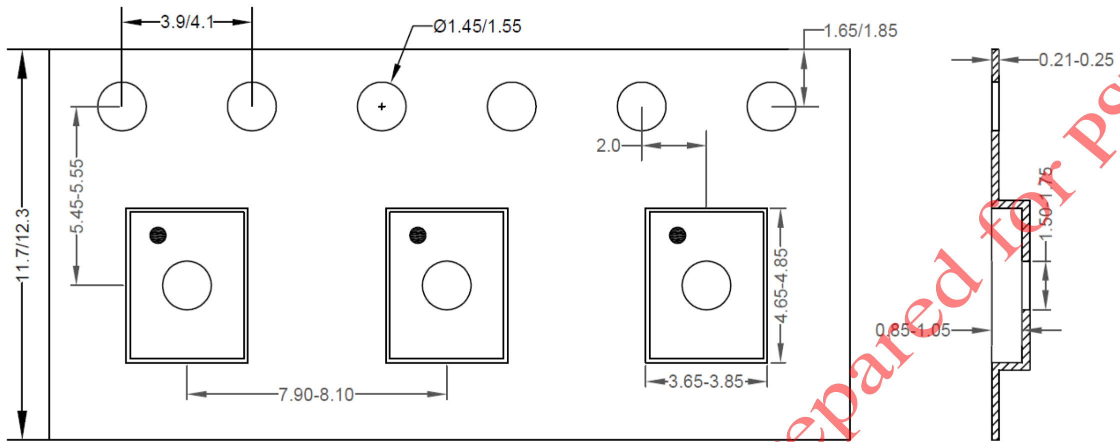


Side View **Recommended Pad Layout**

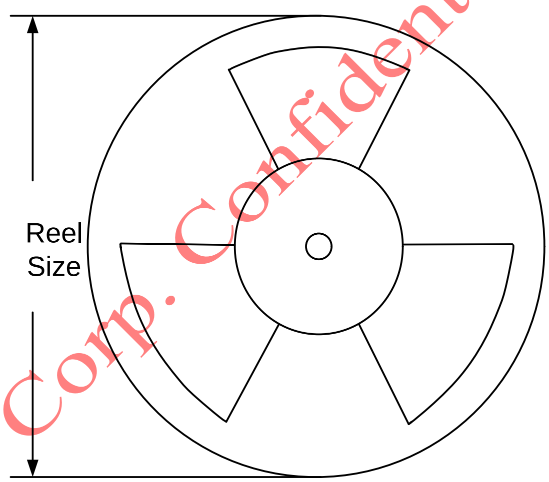
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN3.5×4.5-20 taping orientation



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3.5×4.5	12	8	13"	400	400	5000

3. Others: NA

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