

### General Description

SY205204SLC is a single-line transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection in consumer applications. The SY205204SLC is designed to provide ESD protection against over-current transient events. It complies with IEC 61000-4-2 (ESD) ( $\pm 30\text{kV}$  air,  $\pm 30\text{kV}$  contact discharge), IEC 61000-4-5 (surge) 240A (8/20 $\mu\text{s}$ ).

SY205204SLC provides protection for a single uni-directional line. It has an operating voltage of 4.5V from Pin1 to Pin2 and 0.7V in the opposite direction (Pin2 to Pin1). The part can be used to protect individual control or power lines.

The SY205204SLC is available in a compact DFN1.6x1.0-2 package.

### Features

- Transient Protection for a Single Line
  - IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air)  $\pm 30\text{kV}$  (contact)
  - IEC 61000-4-5 (surge) 240A (8/20 $\mu\text{s}$ )
- For Operating Voltage of 4.5V and Below
- Protects One Control or Power Line
- Capacitance: 1100pF (typical)
- Low Leakage Current: 0.1 $\mu\text{A}$  @  $V_{\text{RWM}}$  (max)
- Low Clamping Voltage

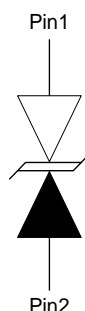
### Applications

- Power Supply Protection
- Power Management
- Battery Protection
- Portable Instrumentation
- Digital Cameras

### Mechanical Characteristics

- DFN1.6x1.0-2 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

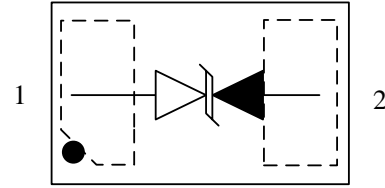
### Circuit Diagram



## Ordering Information

Part Number	Package Type	Top Mark
SY205204SLC	DFN1.6×1.0-2 RoHS Compliant and Halogen Free	MYWA

## Pinout (Top View)



## Marking Codes



**Note 1:** “M” is device code, fixed.

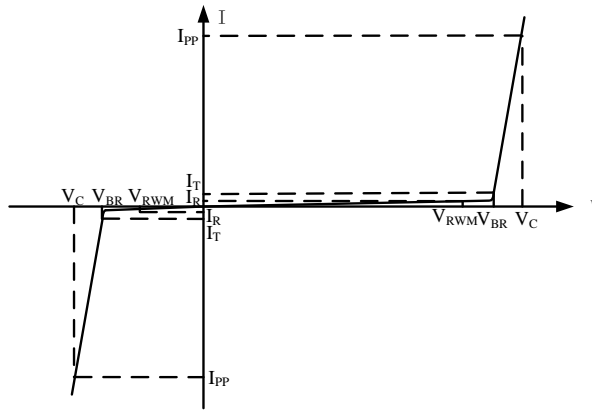
**Note 2:** “YWA” is date code.

Absolute Maximum Rating			
Parameter	Symbol	Value	Units
Maximum Peak Pulse Current (8/20μs)	$I_{PP}$	240	A
Maximum Peak Pulse Power (8/20μs)	$P_{PK}$	3100	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	$V_{ESD}$	±30 ±30	kV
Operating Temperature	$T_{OPT}$	-40/+125	°C
Storage Temperature	$T_{STG}$	-55/+150	°C

Electrical Characteristics ( $T_A = 25^\circ\text{C}$ )						
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Reverse Working Voltage	$V_{RWM}$	Pin1 to Pin2			4.5	V
Nominal Reverse Working Voltage	$V_{RWM}$	Pin2 to Pin1			0.7	V
Reverse Leakage Current @ $V_{RWM}$	$I_R$	$V_{RWM} = 4.5\text{V}$ , $T = 25^\circ\text{C}$ Pin1 to Pin2		0.01	0.1	μA
Reverse Breakdown Voltage @ $I_T$	$V_{BR}$	$I_T = 1\text{mA}$ Pin1 to Pin2	4.6	5.5	6.5	V
Reverse Breakdown Voltage @ $I_T$	$V_{BR}$	$I_T = 1\text{mA}$ Pin2 to Pin1	2.5		4.5	V
Clamping Voltage @ $I_{PP}$	$V_C^1$	$I_{PP} = 10\text{A}$ , $t_p = 8/20\mu\text{s}$		6		V
Clamping Voltage @ $I_{PP}$	$V_C^1$	$I_{PP} = 240\text{A}$ , $t_p = 8/20\mu\text{s}$		13		V
Dynamic Resistance	$R_{DYN}^{1,2}$	$t_p = 10/100\text{ns}$ From Pin1 to Pin2		0.01		Ω
Parasitic Capacitance	$C_{ESD}^1$	$V_R = 0\text{V}$ , $f = 1\text{MHz}$		1100		pF

**Note 1:** Guaranteed by design and not subject to production test.

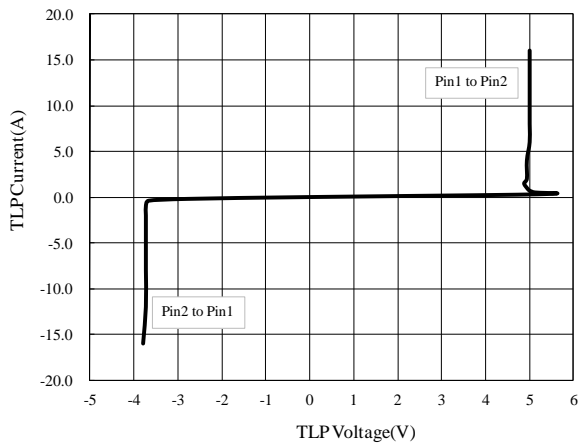
**Note 2:**  $R_{DYN}$  calculated based on  $I_{PP}=8\text{A}$  to  $I_{PP}=16\text{A}$ ,  $t_p = 10/100\text{ns}$ .



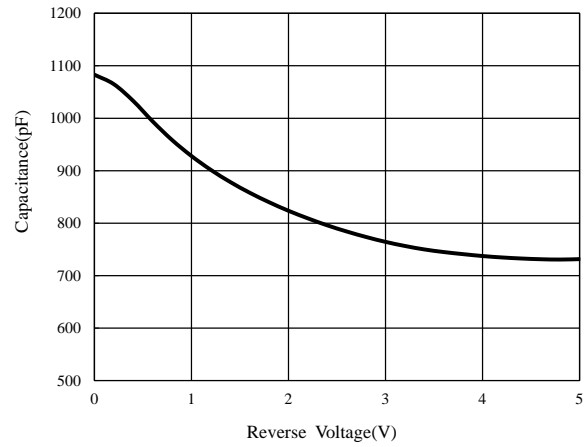
**Figure 1. Uni-Directional TVS**

## Typical Characteristics

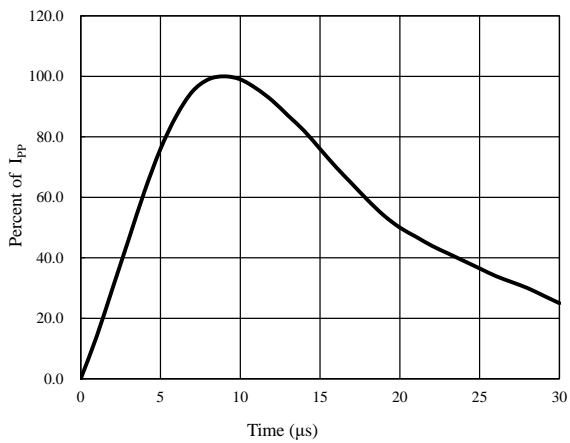
### TLP Testing of I/O to GND



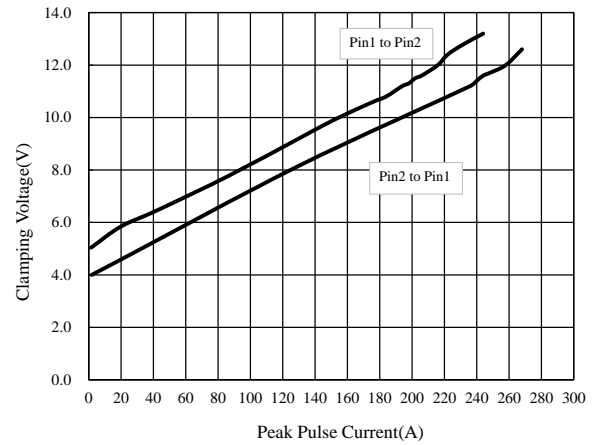
### Capacitance vs. Voltage (f = 1MHz)



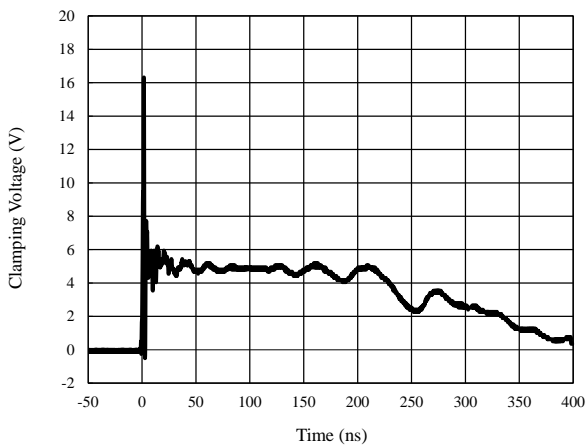
### Pulse Waveform



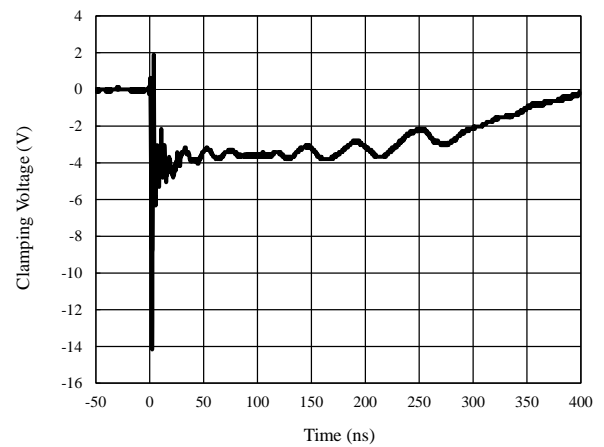
### Clamping Voltage vs. Peak Pulse Current (8/20µs)



### ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



### ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



## Application Information

SY205204SLC is designed to protect one uni-directional line and can be used for control or power lines.

The SY205204SLC pin connections are shown in Figure 2. The control or power line is connected to Pin1. Pin2 is connected to the GND, which should connect to a ground plane on the board. The connection traces should be as short as possible to minimize the parasitic inductance.

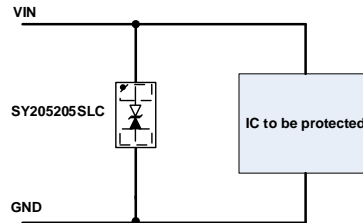


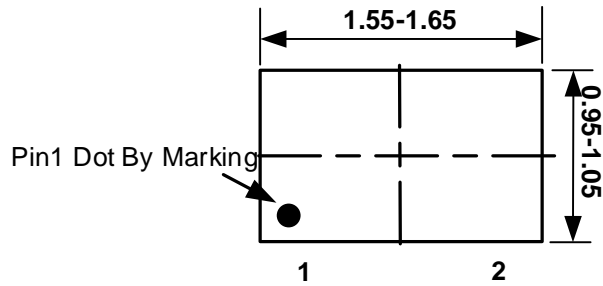
Figure 2. SY205204SLC Pin Connection in PCB

## PCB Layout Guidelines

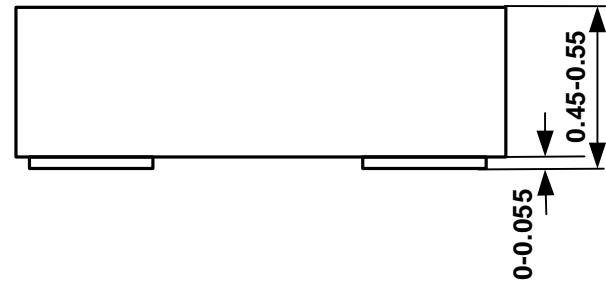
For optimum ESD protection and circuit performance, the following PCB layout guidelines are recommended:

- Place SY205204SLC as close to the connector port as possible.
- Use a large via to connect the SY205204SLC pin to the ground (GND).
- The distance between SY205204SLC Pin2 and the GND reference path should be as short as possible.

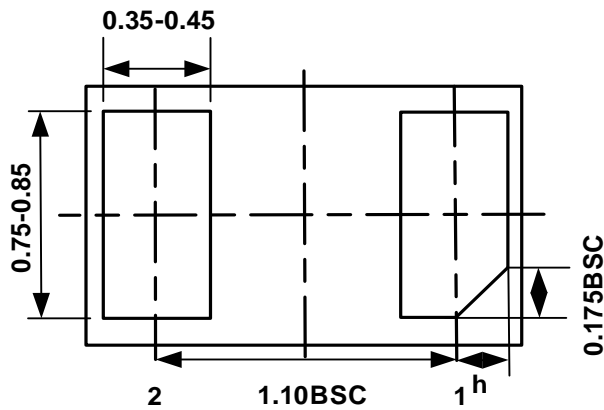
## DFN1.6x1.0-2 Package Outline



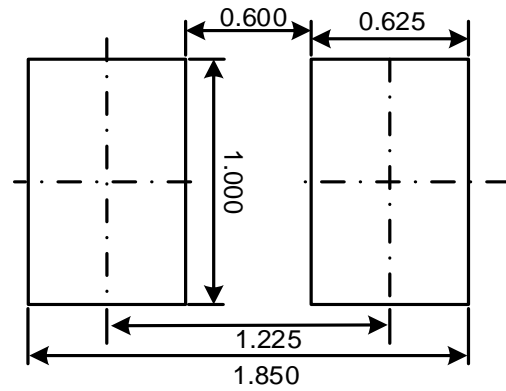
**Top View**



**Side View**



**Bottom View**

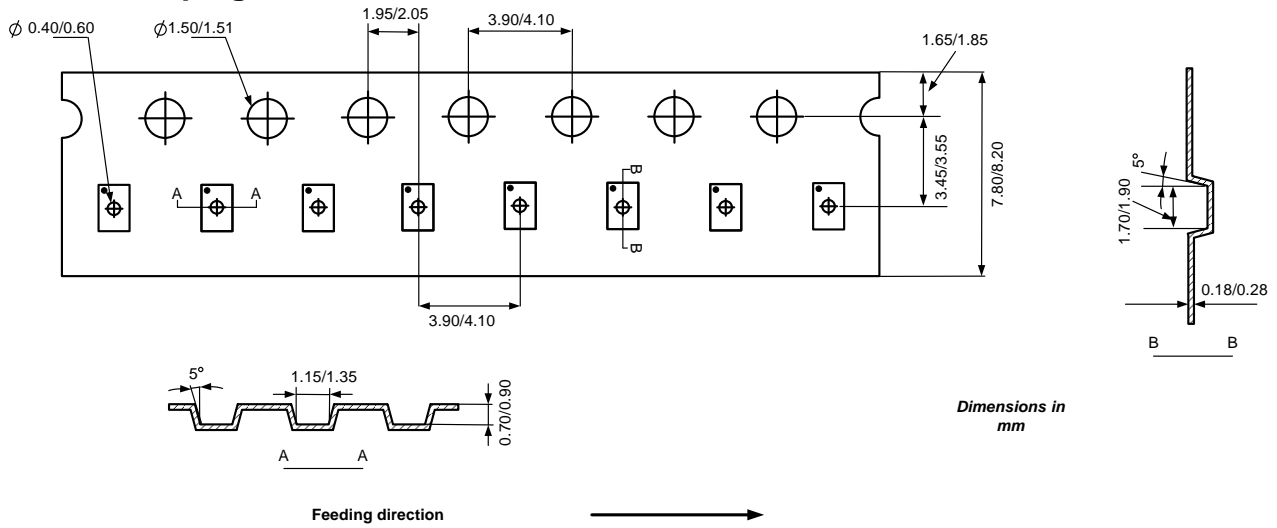


**Recommended PCB Layout  
(Reference only)**

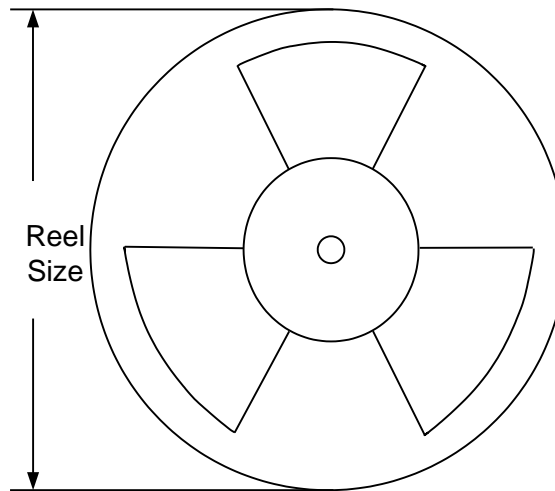
**Note:** All dimensions are in millimeters and exclude mold flash and metal burr.

## Tape and Reel Specification

### DFN1.6x1.0-2 Taping Orientation



### Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN1.6x1.0-2	8	4	7"	3000



## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	06/20/2019	Initial Release	
1.0	06/20/2020	Production Release	



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