

### General Description

SY205212SLC is a single line transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection for the USB VBUS line. The SY205212SLC is designed to protect against ESD and other over-current transient events. It complies with IEC 61000-4-2 (ESD) ( $\pm 30\text{kV}$  air,  $\pm 30\text{kV}$  contact discharge), IEC 61000-4-5 (surge) 25A (8/20 $\mu\text{s}$ ).

The SY205212SLC can protect one uni-directional line. The SY205212SLC is available in a DFN1.6x1.0-2 package with a working voltage of 20V.

### Features

- Transient Protection for Single Line
  - IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (Air)  $\pm 30\text{kV}$  (Contact)
  - IEC 61000-4-5 (Surge) 25A (8/20 $\mu\text{s}$ )
- For Operating Voltage of 20V and Below
- Protects One Control or Power Line
- Capacitance: 210pF (Typical)
- Low Leakage Current: 0.1 $\mu\text{A}$  @  $V_{\text{RWM}}$  (Max)
- Low Clamping Voltage

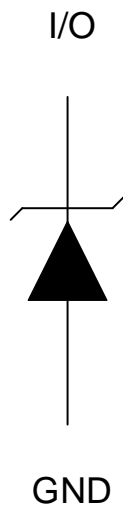
### Applications

- USB VBUS Protection
- Power Supply Protection
- Desktops, Servers and Notebooks
- Mobile Phones
- Portable Instrumentation
- Digital Cameras

### Mechanical Characteristics

- DFN1.6x1.0-2 Package
- Marking: Device code, Date Code
- Packaging: Tape and Reel

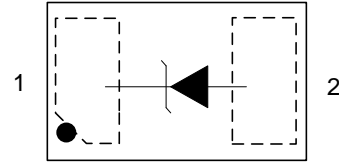
### Circuit Diagram



## Ordering Information

Part Number	Package Type	Top Mark
SY205212SLC	DFN1.6x1.0-2	PYWA

## Pinout (Top View)



## Marking Codes



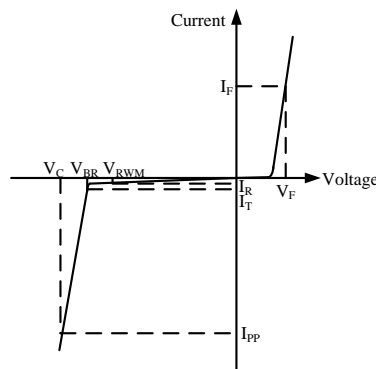
**Note 1:** “P” is device code, fixed.

**Note 2:** “YWA” is date code.

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Maximum Peak Pulse Current (8/20μs)	$I_{PP}$		25	A
Maximum Peak Pulse Power (8/20μs)	$P_{PK}$		850	W
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	$V_{ESD}$	-30	30	kV
Operating Temperature	$T_{OPT}$	-40	+125	°C
Storage Temperature	$T_{STG}$	-55	+150	°C

Electrical Characteristics $T_A = 25^\circ\text{C}$						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal Reverse Working Voltage	$V_{RWM}$				20	V
Reverse Leakage Current @ $V_{RWM}$	$I_R$	$V_{RWM} = 20\text{V}, T_A = 25^\circ\text{C}$ Pin1 to Pin2		0.01	0.1	μA
Reverse Breakdown Voltage @ $I_T$	$V_t$	$I_T = 1\text{mA}$ Pin1 to Pin2	22.2	24.5	27	V
Forward Voltage @ $I_F$	$V_F$	$I_T = 1\text{mA}$ Pin2 to Pin1	0.4		1.2	V
Clamping Voltage @ $I_{PP}$	$V_C (1)$	$I_{PP} = 10\text{A}, t_p = 8/20\mu\text{s}$ Pin1 to Pin2		28		V
Clamping Voltage @ $I_{PP}$	$V_C (1)$	$I_{PP} = 25\text{A}, t_p = 8/20\mu\text{s}$ Pin1 to Pin2		32		V
Parasitic Capacitance	$C_{ESD} (1)$	$V_R = 0\text{V}, f = 1\text{MHz}$ Pin1 to Pin2		210		pF

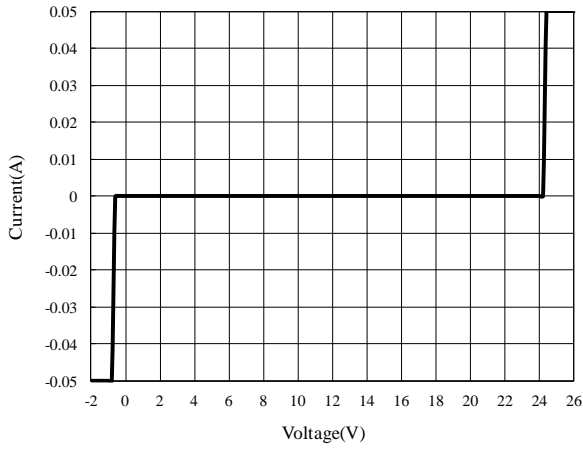
**Note:** The device is not guaranteed to function outside its operating conditions.



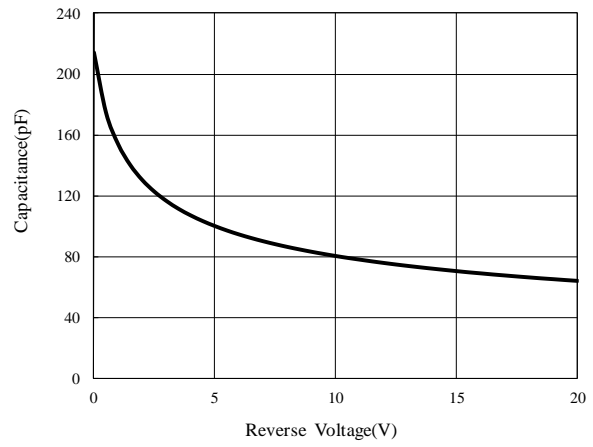
**Figure 1. Uni-Directional TVS**

## Typical Characteristics

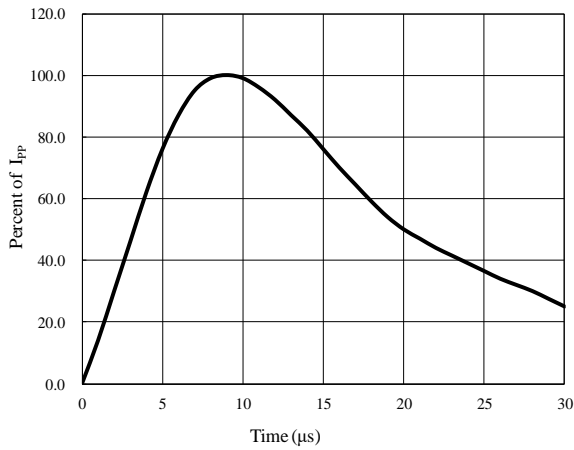
### Voltage Sweeping



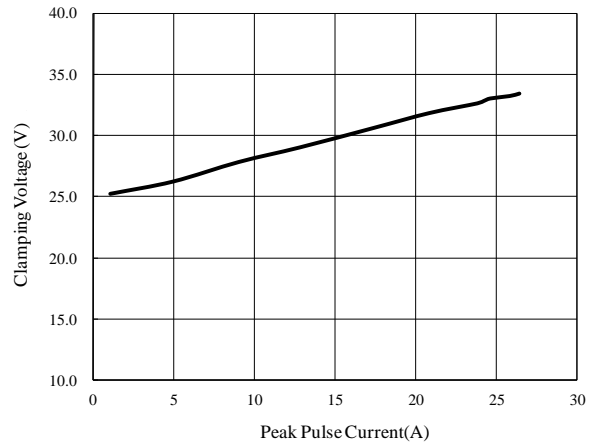
### Capacitance vs. Voltage



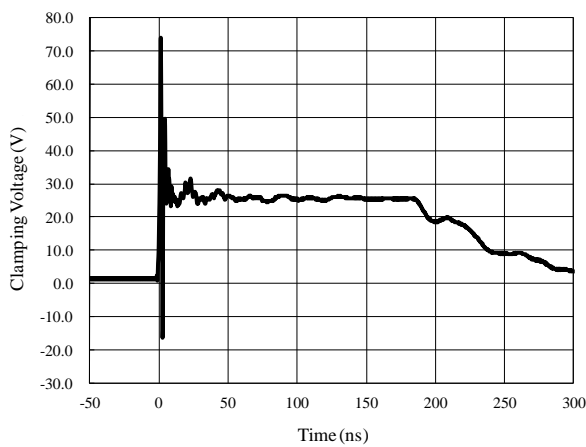
### Pulse Waveform



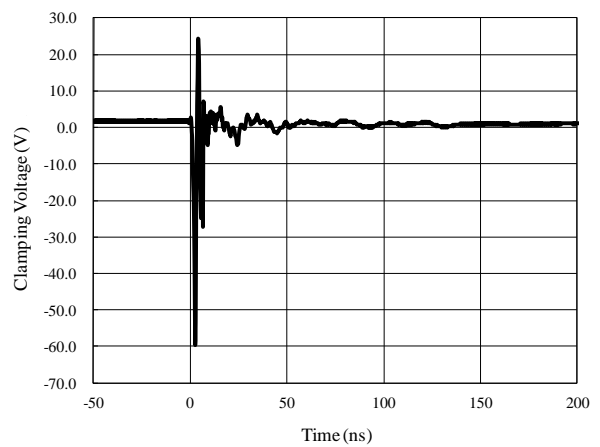
### Clamping Voltage vs. Peak Pulse Current (8/20µs)



### ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



### ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)



## Application Information

The SY205212SLC is designed to protect one line against system EOS by clamping down the voltage at a low level. Figure 2 shows the typical use of SY205212SLC for the USB type-C. The SY205212SLC Pin1 should connect with power or control lines, and Pin2 should connect to the ground plane on the board.

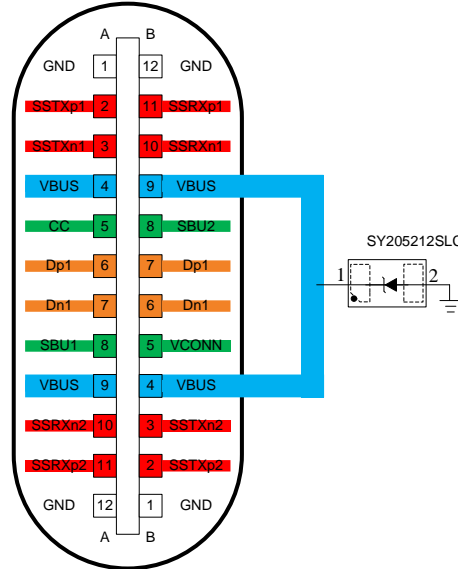


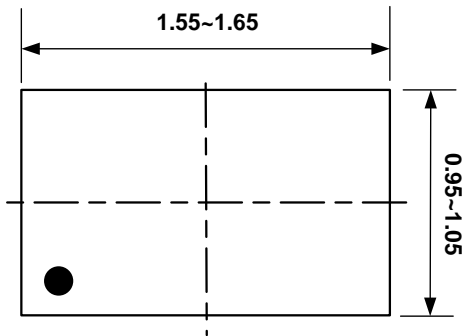
Figure 2. SY205212SLC Typical Application for USB Type-C

## PCB Layout Guidelines

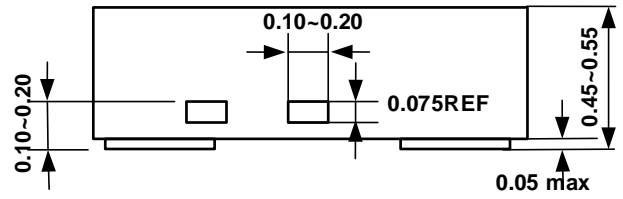
For optimum ESD protection and circuit performance, following PCB layout guidelines are recommended:

- Place the SY205212SLC as close to the connectors or terminal ports as possible.
- The distance between the SY205212SLC ground pin and the GND reference path should be as short as possible.
- Use a large via to connect the SY205212SLC Pin2 to the ground.
- Avoid running signals near board edges.
- The SY205212SLC should be placed near the protected line.

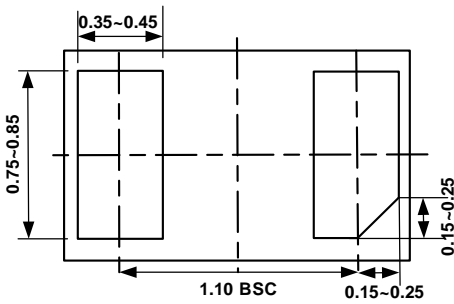
## DFN1.6x1.0-2 Package Outline



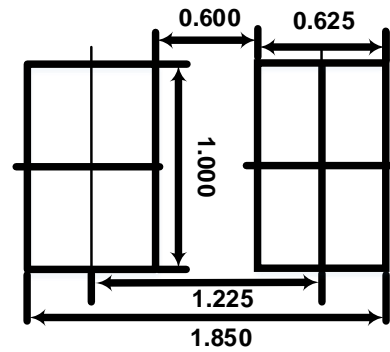
TOP VIEW



SIDE VIEW



BOTTOM VIEW

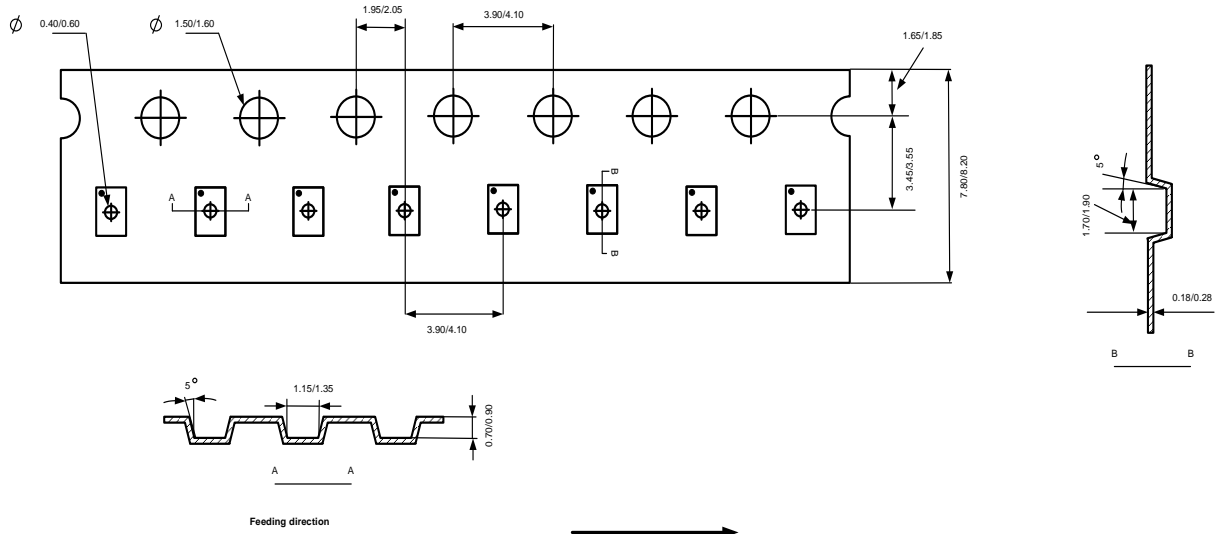


Recommended PCB Layout  
(Reference Only)

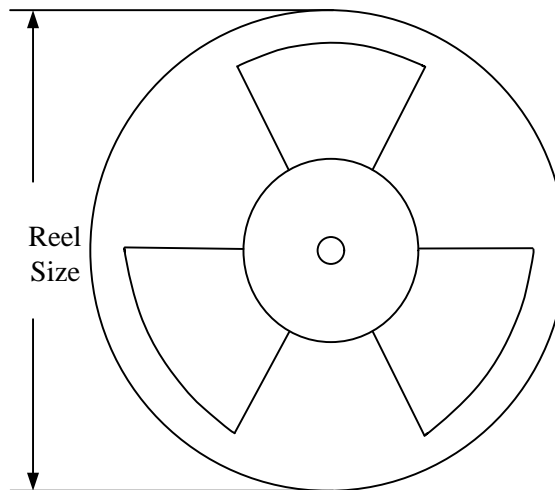
**Note:** All dimensions are in millimeters and exclude mold flash and metal burr.

## Tape and Reel Specification

### DFN1.6x1.0-2 Taping Orientation



### Carrier Tape & Reel Specification for Packages



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel (pcs)
DFN1.6x1.0-2	8	4	7"	3000



## Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	10/26/2018	Initial Release	
1.0	10/26/2019	Production Release	

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