### **SY205248DWD**

### **Single Line TVS Diode for ESD Protection**

### **General Description**

SY205248DWD is a single-line transient voltage suppressor (TVS) designed to provide electrostatic discharge (ESD) protection in consumer applications. The SY205248DWD is designed to protect sensitive semiconductor components from damage or upset due to ESD and other over-current transient events. It complies with IEC 61000-4-2 (ESD)(±30kV air, ±30kV contact discharge), and IEC 61000-4-5 (surge) 9A  $(8/20 \mu s)$ .

SY205248DWD can protect one unidirectional line. The SY205248DWD is available in a DFN1.0×0.6-2 package with a working voltage of 24V.

#### **Features**

- For Operating Voltage of 24V and Below
- Capacitance: 85pF (Typical)
- Protects One Data, Control, or Power Line
- Low Leakage Current: 0.01µA @ VRWM (Typical)
- Low Clamping Voltage
- Transient Protection for a Single Line.
  - IEC 61000-4-2 (ESD) ±30kV (Air)±30kV (Contact)
  - IEC 61000-4-5 (Surge) 9A (8/20µs)

### **Applications**

- VBUS, VBAT
- Desktops, Servers, and Notebooks
- Cellular Phones
- Microprocessor-Based Equipment
- Portable Instrumentation

#### **Mechanical Characteristics**

- DFN1.0×0.6-2 Package
- Marking: Device Code, Date Code
- Packaging: Tape and Reel

## **Circuit Diagram**

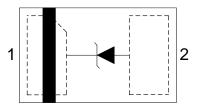




### **Ordering Information**

Part Number	Package Type	Top Mark	
SY205248DWD	DFN1.0×0.6-2 RoHS Compliant and Halogen Free	ВМ	

### Pinout (Top View)



# **Marking Codes**



Note 1: "B" is device code, fixed.

Note 2: "M" is date code

Absolute Maximum Rating				
Parameter	Symbol	Min	Max	Unit
Peak Pulse Power (8/20µs)	P <sub>PK</sub>		320	W
Peak Pulse Current (8/20µs)	IPP		9	Α
ESD per IEC 61000-4-2 (Air)	V	20	20	14/
ESD per IEC 61000-4-2 (Contact)	V <sub>ESD</sub>	-30	30	kV
Operating Temperature	Торт	-40	+125	°C
Storage Temperature	T <sub>STG</sub>	-55	+150	°C

Electrical Characteristics T <sub>A</sub> = 25°C						
Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Nominal Reverse Working Voltage	$V_{RWM}$				24	V
Reverse Leakage Current @ V <sub>RWM</sub>	$I_R$	$V_{RWM} = 24V$ , $T_A = 25$ °C			0.1	μA
Reverse Breakdown Voltage @ I <sub>T</sub>	$V_{BR}$	$I_T = 1 \text{mA}$	25		30	V
Forward Voltage @ I <sub>F</sub>	$V_{F}$	I <sub>F</sub> =1mA	0.4		1.2	V
Clamping Voltage @ IPP	Vc(1)	$I_{PP} = 9A, t_p = 8/20 \mu s$		36		V
Clamping Voltage @ IPP	Vc(1)	$I_{PP} = 16A, t_p = 10/100ns$		30		V
Dynamic Resistance	R <sub>DYN</sub> (1.2)	t <sub>p</sub> = 10/100ns		0.05		Ω
Parasitic Capacitance	C <sub>ESD</sub> (1)	$V_R = 0V$ , $f = 1MHz$		85	100	pF

**Note 1:** Guaranteed by design and not subject to production test.

Note 2:  $R_{DYN}$  calculated based on  $I_{PP}$ =8A to  $I_{PP}$ =16A,  $t_p$  = 10/100ns.



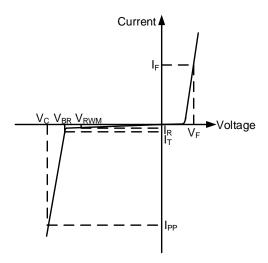
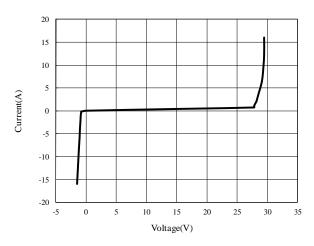


Figure 1. Uni-directional TVS

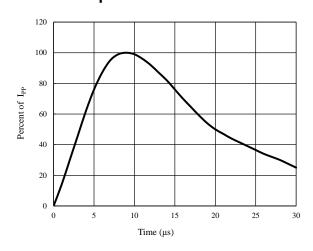


## **Typical Performance Characteristics**

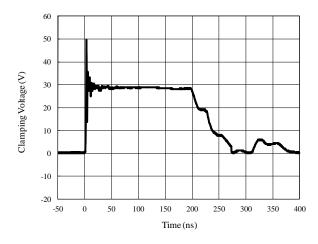
### TLP Testing of I/O to GND



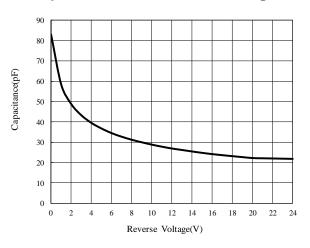
### 8/20µs Pulse Waveform



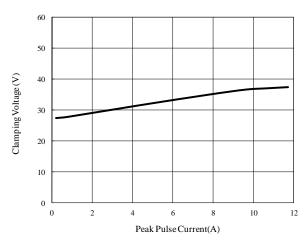
ESD Clamping of I/O to GND (+8kV Contact per IEC 61000-4-2)



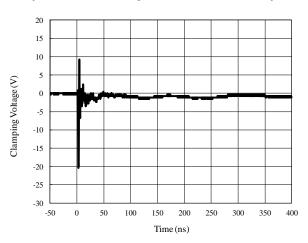
### Capacitance vs. Reverse Voltage



### Clamping Voltage vs. Peak Pulse Current



ESD Clamping of I/O to GND (-8kV Contact per IEC 61000-4-2)





### **Application Information**

The SY205248DWD protects one bidirectional data line against over-voltage and over-current transient events by clamping it to an acceptable reference.

The SY205248DWD pin connections are shown in Figure 2. The protected line is connected at Pin1 while Pin2 is connected to GND, which should connect to a ground plane on the board. All path lengths connected to pins of SY205248DWD should be as short as possible to minimize the parasitic inductance.

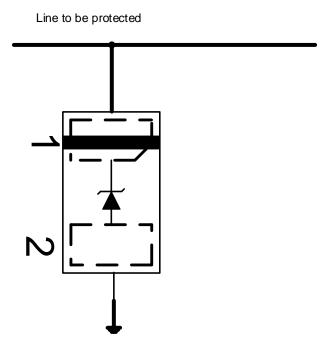


Figure 2. ESD/Surge Protection Circuit

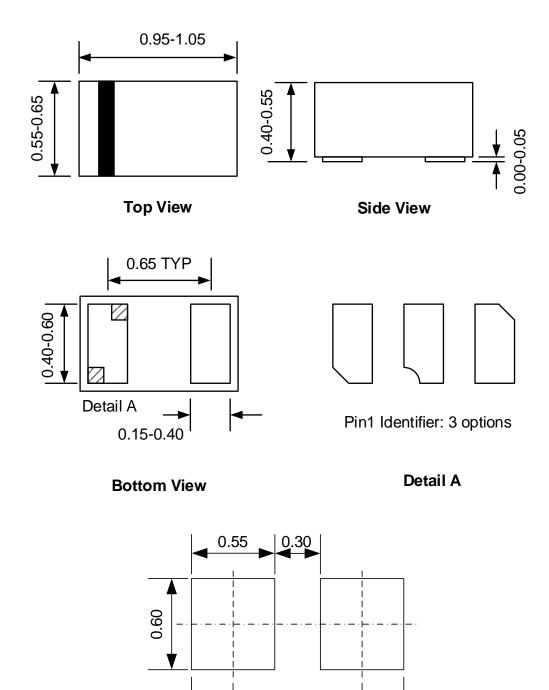
## **PCB Layout Guidelines**

For optimum ESD protection and circuit performance, the following circuit board guidelines are recommended:

- Place SY205248DWD as close to the connector or terminal ports as possible.
- Use a large via to connect the SY205248DWD pin to the ground.
- Avoid running signals near board edges.
- The SY205248DWD should be placed near the protected line.
- The distance between the SY205248DWD ground pin and the GND reference path should be as short as possible.



### DFN1.0×0.6-2 Package Outline



0.85

1.40

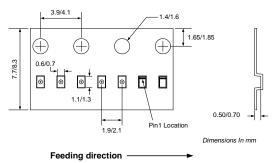
**Recommended PCB Layout** (Reference only)

Note: All dimensions are in millimeters and exclude mold flash and metal burr.

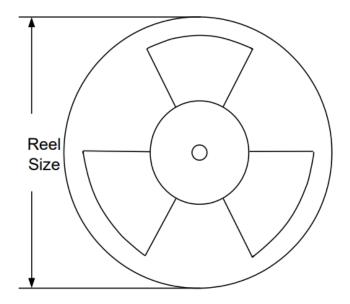


# **Tape and Reel Specification**

## **DFN1.0×0.6-2 Taping Orientation**



### **Carrier Tape & Reel Specification for Packages**



Package Types	Tape Width (mm)	Pocket Pitch(mm)	Reel Size (Inch)	Qty per Reel(pcs)
DFN1.0×0.6-2	8	2	7"	10000





### **Revision History**

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Revision Number	Revision Date	Description	Pages changed
0.9	07/08/2022	Initial Release	
1.0	07/08/2023	Production Release	



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