

General Description

The SY20737H is a high-voltage input Linear Voltage Regulator (LDO) operating with input voltages from 4V to 36V and capable of delivering 500mA to a load, with ultra-low ground current and low dropout voltage.

The SY20737H has an adjustable output that can be configured using two external resistors. The device offers protection features, including an over-current limit, output short and over-temperature protections.

The Enable input allows disabling the part to reduce power consumption.

The High-Power Supply Rejection Ratio (PSRR) and low noise makes this part suitable for many applications in industrial and consumer products.

The SY20737H is available in a compact DFN 2mmx3mm-8pin package.

Features

- Input Voltage Range: 4V to 36V
- $V_{ABS} = 40V$
- $V_{FB}: 1.235V (\pm 1\%)$
- Output Voltage Tolerance: $\pm 1\%$
- Line Regulation: $0.2\%/V$
- Load Regulation: 0.25%
- PSRR: 60dB
- Noise Level: $150\mu VRMS$
- Operating T_J : $-40^\circ C$ to $125^\circ C$
- Auto Retry-During Fault Conditions
- Compact Package: DFN2x3-8

Applications

- Portable Consumer Equipment
- Portable Instrumentation
- Industrial Equipment
- SMPS Post Regulators

Typical Application

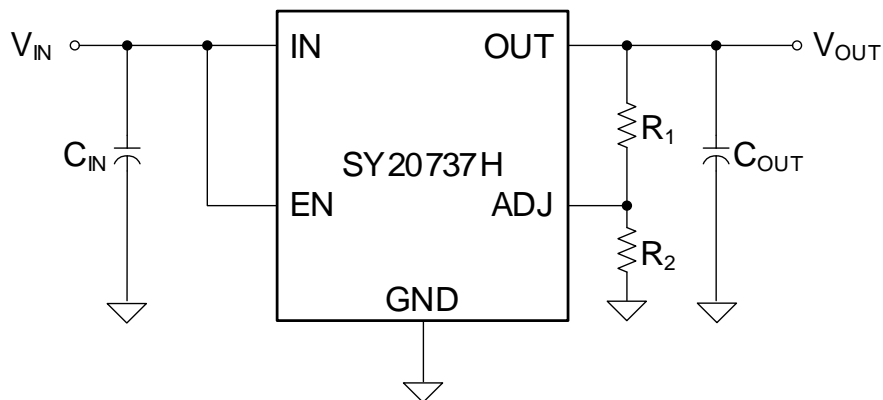


Figure 1. Schematic Diagram

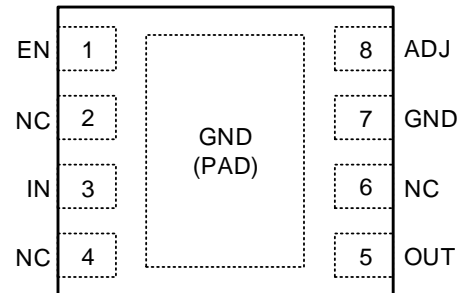


Ordering Information

| Ordering Part Number | Package Type | Top Mark |
|----------------------|---|----------|
| SY20737HDGD | DFN2x3-8 RoHS Compliant and Halogen Free | 4Axyz |

x=year code, y=week code, z=lot number code

Pinout (top view)



Pin Description

| Pin Name | Pin Number | Pin Description |
|----------|------------|---|
| EN | 1 | Enable. CMOS-compatible control input. Logic high = enable. Logic low or open = shutdown. |
| NC | 2, 4, 6 | No connection. |
| IN | 3 | Supply input. |
| OUT | 5 | Regulator output. |
| GND | 7 | Ground. |
| ADJ | 8 | Adjustable part only. Feedback input. Connect to resistive voltage-divider network. |

Block Diagram

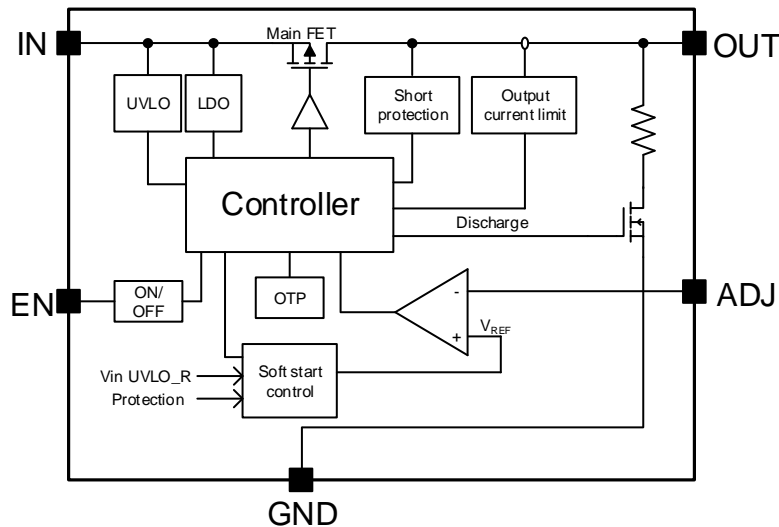


Figure 2. Block Diagram

Absolute Maximum Ratings

| Parameter (Note1) | Min | Max | Unit |
|---------------------------------------|------|-----|------|
| IN, EN, OUT, ADJ | -0.3 | 40 | V |
| Lead Temperature (Soldering, 10 sec.) | | 260 | °C |
| Junction Temperature, Operating | -40 | 150 | |
| Storage Temperature | -65 | 150 | |

Thermal Information

| Parameter (Note2) | Typ | Unit |
|--|------|------|
| θ_{JA} Junction-to-ambient Thermal Resistance | 46 | °C/W |
| θ_{JB} Junction-to-Board Thermal Resistance | 22.5 | |
| θ_{JC} Junction-to-case Thermal Resistance | 28 | |
| P_D Power Dissipation $T_A = 25^\circ\text{C}$ | 2.17 | W |

Recommended Operating Conditions

| Parameter (Note 3) | Min | Max | Unit |
|---------------------------------|-----|-----|------|
| IN | 4 | 36 | V |
| EN, OUT, ADJ | 0 | 36 | |
| Junction Temperature, Operating | -40 | 125 | °C |



Electrical Characteristics

($V_{IN} = V_{EN} = 12V$, $T_J = -40^{\circ}C \sim 125^{\circ}C$, typical values are at $T_J = 25^{\circ}C$, unless otherwise specified, the values are guaranteed by test, design, or statistical correlation.)

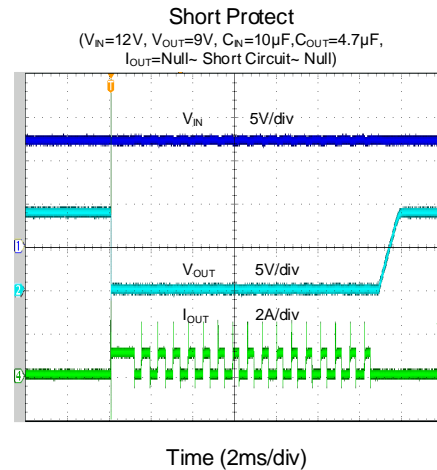
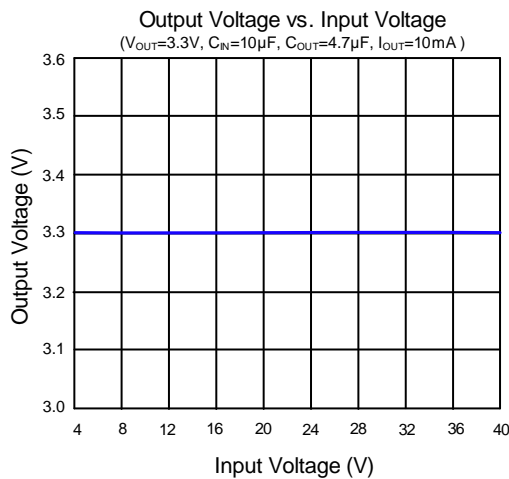
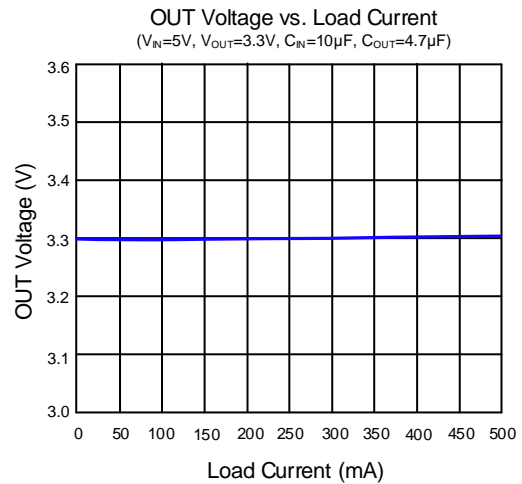
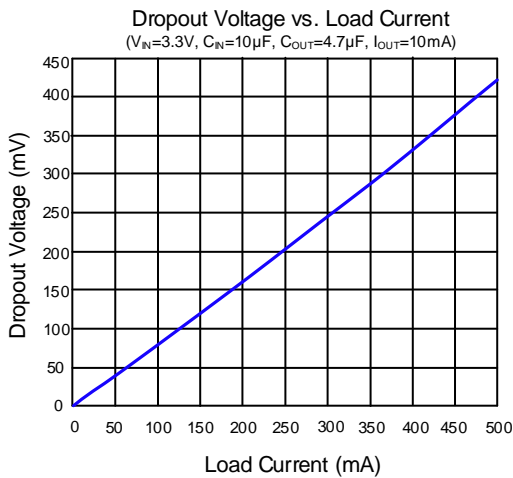
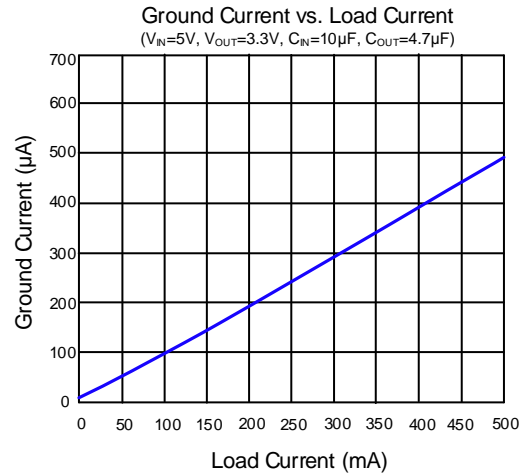
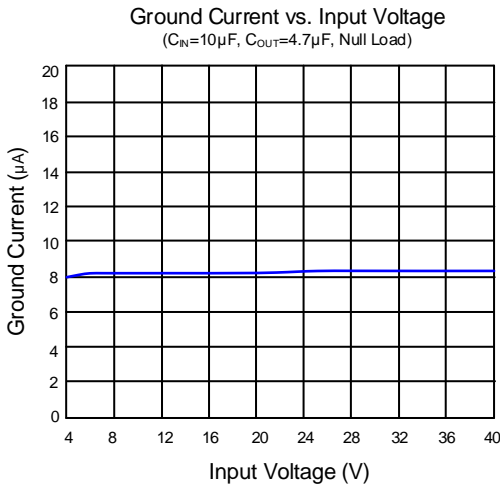
| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---------------------------------|-------------------|--|-------|-------|-------|---------------|
| Input Voltage | V_{IN} | | 4 | | 36 | V |
| Reference Voltage | V_{REF} | $T_A = 25^{\circ}C$ | 1.223 | 1.235 | 1.247 | V |
| | | $T_J = -40^{\circ}C \sim 125^{\circ}C$ | 1.210 | 1.235 | 1.260 | V |
| Line Regulation | ΔV_{LNR} | $I_{OUT} = 10mA$, $4V \leq V_{IN} \leq 36V$ | | 1 | 1.5 | mV/V |
| Load Regulation | ΔV_{LDR} | $V_{IN} = 5V$, $10mA \leq I_{OUT} \leq 0.5A$, | | 0.25 | 1.0 | % |
| Dropout Voltage | ΔV_{DROP} | $I_{OUT} = 10mA$ | | 10 | 20 | mV |
| | | $I_{OUT} = 300mA$ | | 300 | 540 | mV |
| | | $I_{OUT} = 500mA$ | | 500 | 750 | mV |
| Shutdown Current | I_{SHDN} | $V_{EN} = 0V$, $V_{IN} = 24V$ | | | 5 | μA |
| Ground Pin Current | I_{GND} | No Load | | 7 | 14 | μA |
| | | $I_L = 0.1mA$ | | 90 | 190 | μA |
| | | $I_L = 50mA$ | | 250 | 900 | μA |
| | | $I_L = 150mA$ | | 1.0 | 2.5 | mA |
| | | $I_L = 500mA$ | | 6.5 | 30.0 | mA |
| Output Current | I_O | $V_{IN} = V_{OUT} + 1V$ | 0 | | 500 | mA |
| Current Limit | I_{LIMIT} | $V_{OUT} = 0.9 \times V_{OUT}(\text{normal})$ | 600 | 900 | 1200 | mA |
| Input Voltage UVLO Threshold | V_{UVLO} | V_{IN} rising | | | 3.9 | V |
| UVLO Hysteresis | $V_{UVLO,HYS}$ | | | 200 | | mV |
| Shutdown Discharge Resistance | R_{DIS} | | | 600 | | Ω |
| Ripple Rejection | PSRR | | | 60 | | dB |
| Output Noise | e_{NO} | $I_L = 10mA$, $C_L = 1.0\mu F$, $C_{IN} = 1\mu F$, (10Hz – 100kHz) | | 150 | | μV_{RMS} |
| Enable Input Logic-low Voltage | V_{IL} | OFF | | | 0.4 | V |
| Enable Input Logic-high Voltage | V_{IH} | ON | 1.5 | | | V |
| Thermal Shutdown Temperature | T_{SD} | | | 150 | | $^{\circ}C$ |
| Thermal Shutdown Hysteresis | T_{HYS} | | | 20 | | $^{\circ}C$ |

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^{\circ}C$ on a high effective single layer thermal conductivity test board of JESD51-2, -5, -7, -8, -14 thermal measurement standard.

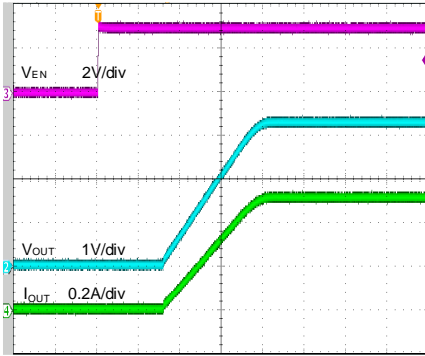
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics



Startup from Enable

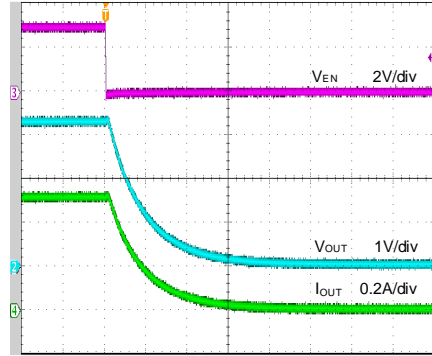
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_N=10\mu F$, $C_{OUT}=4.7\mu F$, $I_{OUT}=500mA$)



Time (400µs/div)

Shutdown from Enable

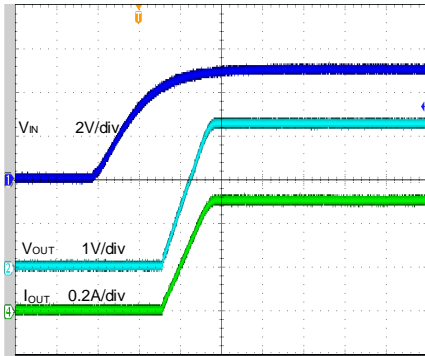
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_N=10\mu F$, $C_{OUT}=4.7\mu F$, $I_{OUT}=500mA$)



Time (40µs/div)

Startup from V_{IN}

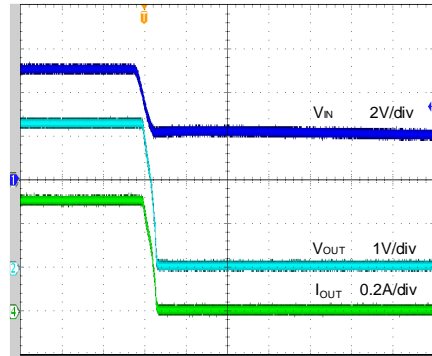
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_N=10\mu F$, $C_{OUT}=4.7\mu F$, $I_{OUT}=500mA$)



Time (800µs/div)

Shutdown from V_{IN}

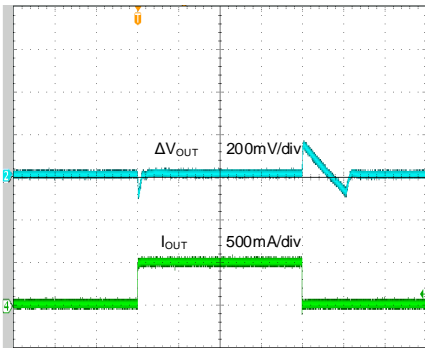
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_N=10\mu F$, $C_{OUT}=4.7\mu F$, $I_{OUT}=500mA$)



Time (2ms/div)

Load Transient

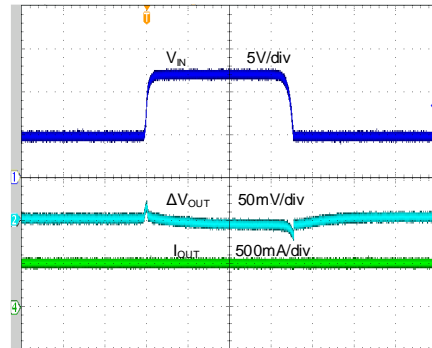
($V_{IN}=5V$, $V_{OUT}=3.3V$, $C_N=10\mu F$, $C_{OUT}=4.7\mu F$, $I_{OUT}=10mA \sim 500mA \sim 10mA$)



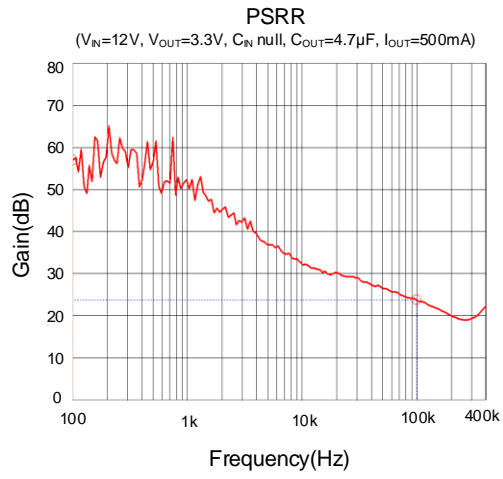
Time (100µs/div)

Line Transient

($V_{IN}=5V \sim 12V \sim 5V$, $V_{OUT}=3.3V$, $C_N=10\mu F$, $C_{OUT}=4.7\mu F$, $I_{OUT}=500mA$)



Time (2ms/div)

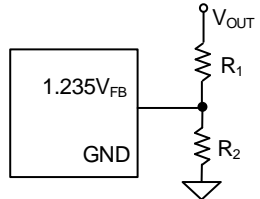


Application Information

The SY20737H is a 500mA high-current capacity linear regulator with ultra-low ground current and low dropout voltage. The SY20737H has an adjustable output that can be set by two external resistors. The device provides protection features, including over-current limit, output short and over-temperature protections.

Feedback Resistor Dividers R₁ and R₂:

Choose R₁ and R₂ to program the proper output voltage. To minimize the power consumption under light loads, choosing large resistance values for both R₁ and R₂ is recommended. A value of between 10kΩ and 10MΩ is recommended for both resistors. As an example, for a V_{OUT} of 3.3V, if R₁=50.1kΩ is chosen, then using the following equation, R₂ can be calculated to be 30kΩ:

$$R_2 = \frac{1.235V}{V_{OUT} - 1.235V} \times R_1$$


Input Capacitor C_{IN}:

An input capacitor of about 10μF between the device input and ground pin is required. A typical X5R or better grade ceramic capacitor is recommended for most applications. Place the input capacitor as close as practical to the device to minimize the input noise.

Output Capacitor C_{OUT}:

The SY20737H is designed specifically to work with very small ceramic output capacitors for transient stability. A 4.7μF output capacitance can be used in this application. Higher capacitance values help to improve transient response. The output capacitor's ESR is critical because it forms a zero to provide phase lead which is required for loop stability.

Dropout Voltage:

The SY20737H has a very low dropout voltage due to its extra low R_{DS(ON)} of the main PMOS, which determines the lowest usable supply.

$$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$$

Over-Current and Short-Circuit Protection:

The device includes over-current and short-circuit protection. The current limiting circuit regulates the output current to its limit threshold to protect the device from damage. Under over-current or short-circuit conditions, the dissipated power on device can be high, which may trigger thermal protection.

Thermal Considerations:

The SY20737H can deliver a current of up to 500mA over the full operating temperature range. However, the maximum output current must be derated at a higher ambient temperature. Under all operating conditions the junction temperature must be within the range specified. The LDO power dissipation can be calculated based on the output current and the voltage drop across the regulator.

The dissipated power, P_D, can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

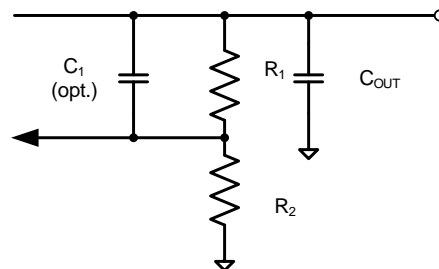
The operating junction temperature can be estimated by the following thermal formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where T_{J(MAX)} is the maximum junction temperature of die (125°C), T_A is the maximum ambient temperature and θ_{JA} is the junction to ambient thermal resistance for the package (46°C/W).

Load Transient Considerations:

The SY20737H integrates the compensation components to achieve stability and fast transient response. In some applications, adding a small ceramic capacitor in parallel with R₁ may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



PCB Layout Guide:

For the best performance of the SY20737H, the following guidelines must be followed:

1. Keep all power traces as short and wide as possible. A 2-layer- or 4-layer board is recommended for improved thermal performance and current flow capability.
2. Place the input/output capacitor close to the IC for better transient performance.
3. Maximize the copper area connected to GND and the exposed pad of the package to improve heat dissipation.

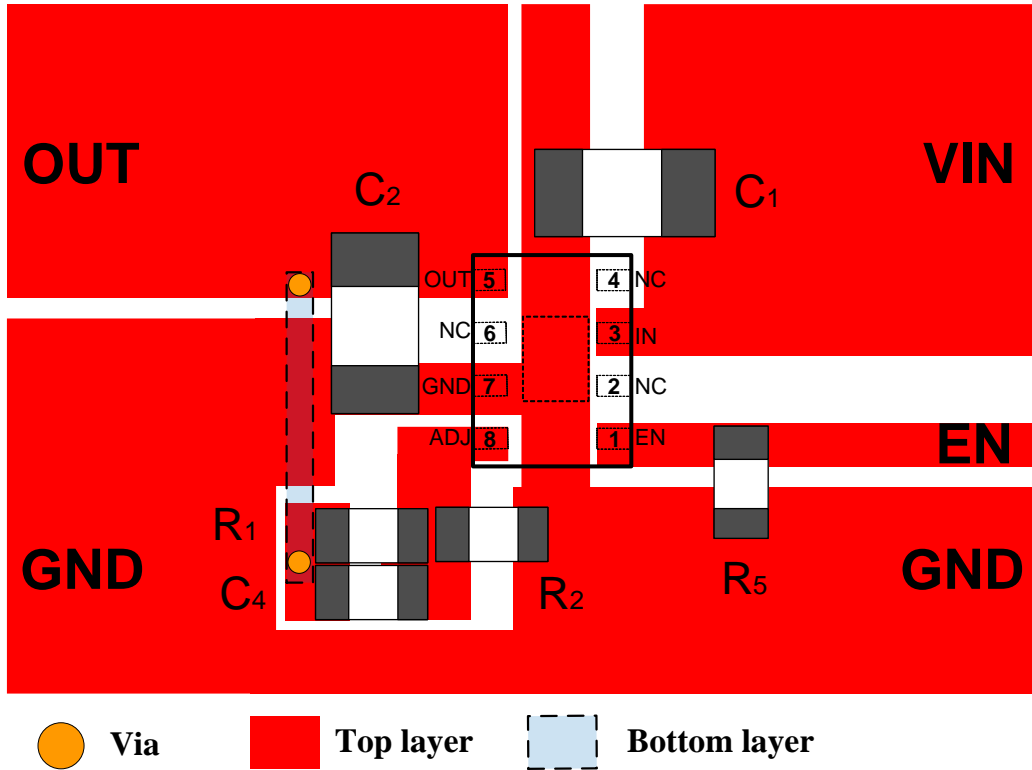
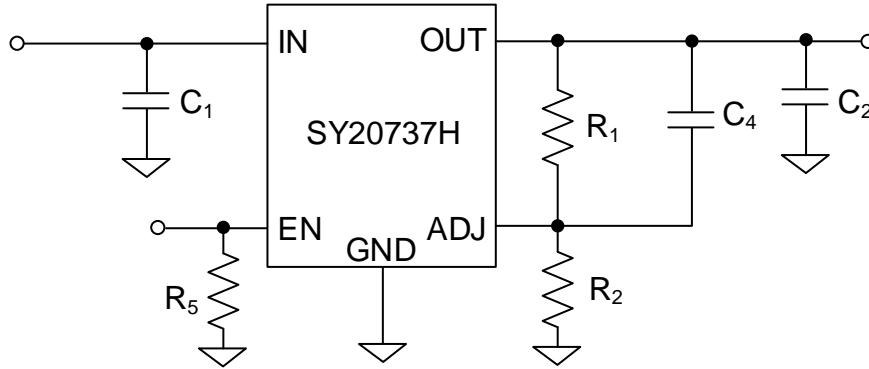


Figure 3. PCB Layout Suggestion

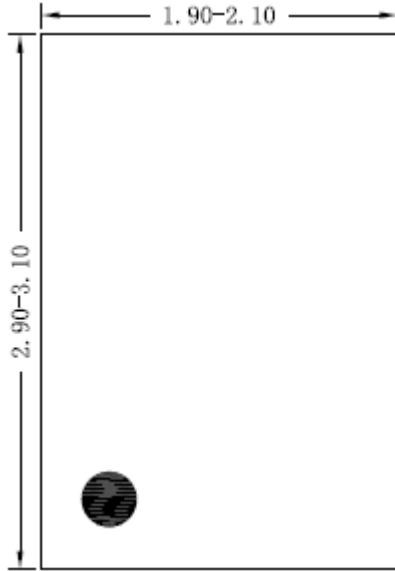
Application Schematic (V_{OUT}=3.3V)



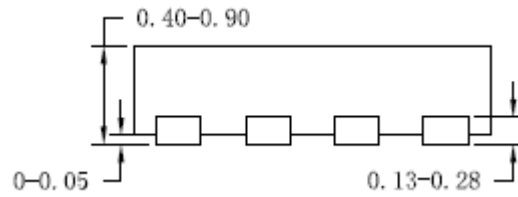
BOM List

| Reference Designator | Description | Part Number | Manufacturer |
|----------------------|--------------------|----------------|--------------|
| C ₁ | 10μF/50V/X5R,1206 | GRM31CR61H106K | Murata |
| C ₂ | 4.7μF/25V/X5R,1206 | GRM31CR61E475K | Murata |
| R ₁ | 50.1kΩ, 1%, 0603 | | |
| R ₂ | 30kΩ, 1%, 0603 | | |
| R ₅ | 1MΩ, 1%, 0603 | | |

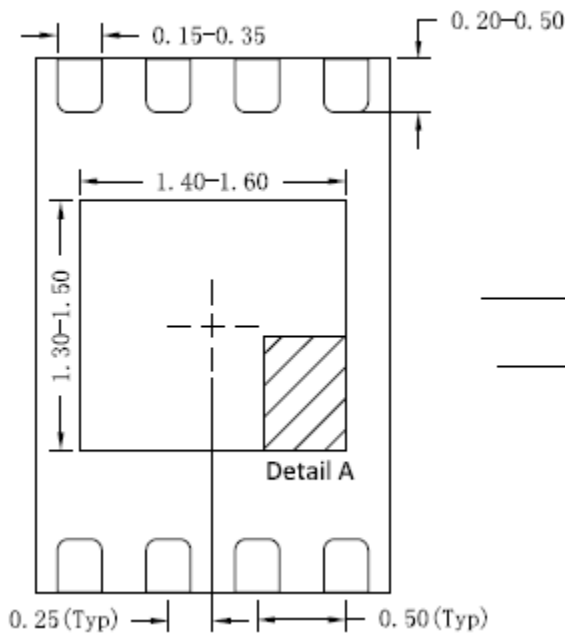
DFN2x3-8 Package Outline



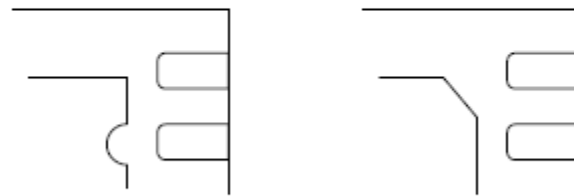
Top View



Side View

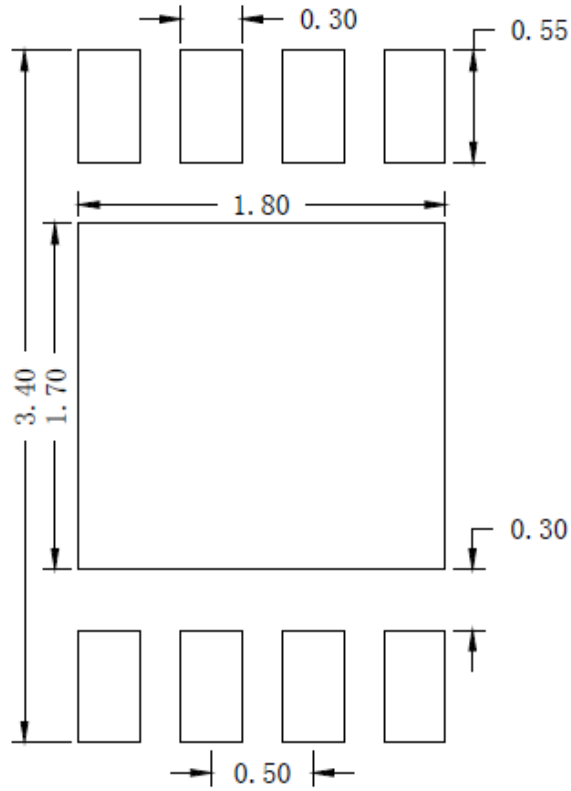


Bottom View



Detail A

Pin1 Identifier: two options

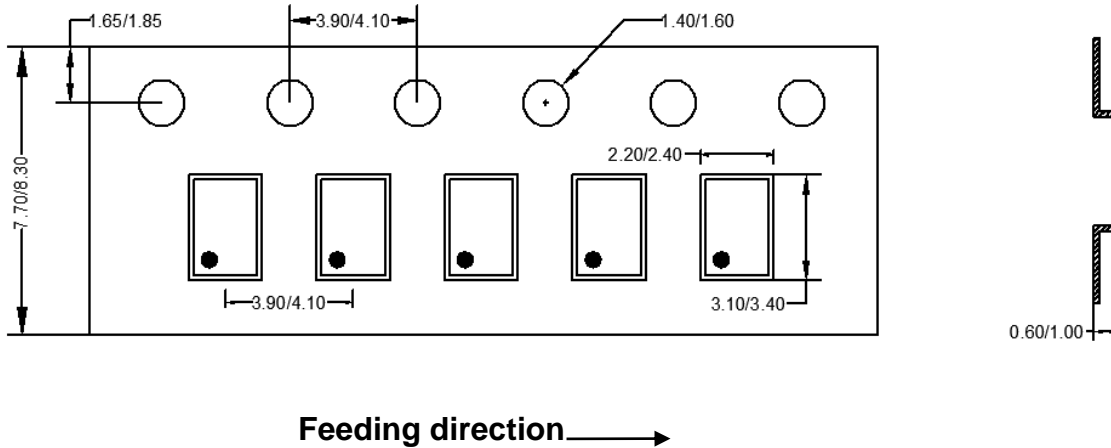


**Recommended PCB Layout
(Reference Only)**

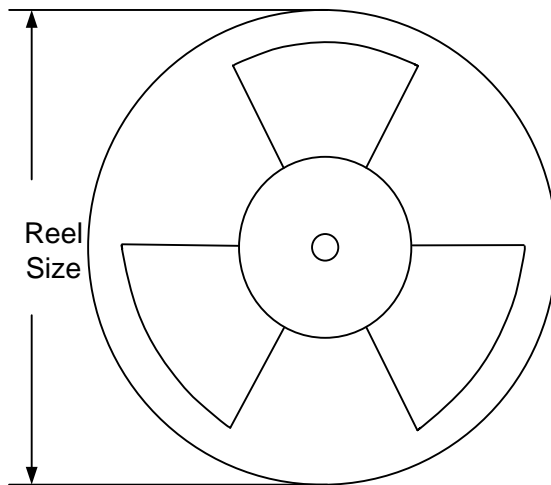
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping & Reel Specification

1. DFN2x3-8 Taping Orientation



2. Carrier Tape & Reel Specification for Packages



| Package type | Tape width (mm) | Pocket pitch(mm) | Reel size (Inch) | Trailer length(mm) | Leader length (mm) | Qty per reel |
|--------------|-----------------|------------------|------------------|--------------------|--------------------|--------------|
| DFN2x3 | 8 | 4 | 7" | 400 | 160 | 3000 |

3. Others: NA



Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please reference the latest revision.

| Date | Revision | Change |
|--------------|-----------------|------------------------------------|
| Sep.27, 2023 | Revision 1.0 | Language improvements for clarity. |
| Jul.28, 2020 | Revision 0.9 | Initial Release |

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