SY21240

High-Efficiency, Fast-Response, 9A Continuous/14A Peak, 24V Input, Synchronous Step-Down Regulator with ±1A V_{TT} LDO and ±10mA Buffered Reference

General Description

The SY21240 high-efficiency synchronous step-down DC/DC regulator is capable of delivering 9A continuous/14A peak current over a wide input voltage range of 4V to 24V. It provides a complete power supply with the highest density for DDR3, DDR3L, LPDDR3, and DDR4 memory. The included sink/source V_{TT} LDO can deliver ±1A output current.

Silergy's constant on-time (COT) ripple-based control strategy supports high input/output voltage ratios (low duty cycles), and fast transient response while maintaining a near-constant operating frequency over line, load, and output voltage ranges. This control method provides stable operation without complex compensation, even with low-ESR ceramic capacitors.

The SY21240 offers protection against multiple conditions, including cycle-by-cycle current limit, input undervoltage lockout, output undervoltage and overvoltage protection, internal soft-start, and thermal shutdown.

Only the input and output capacitors, inductor, and feedback resistors need to be selected for the targeted application.

The SY21240 is available in a compact QFN3mm×3mm-20 package.

Features

- 4–24V Input Voltage Range
- Up to 9A Continuous/14A Peak Output Current
- Low $R_{DS(ON)}$ for Internal Switches: 27mΩ Top, 9mΩ Bottom
- Integrated 1.2Ω Bypass Switch
- COT Ripple-Based Control to Achieve Fast Transient Responses
- 450µs Soft-Start Inrush Current Limit
- Pseudoconstant Frequency: 600kHz
- Adjustable Output Voltage
- ±1% 0.6V Internal Reference Voltage
- ±1A Source/Sink Current Capability
- Buffered Low-Noise ±10mA V_{TTREF} Output
- PFM/FCCM Selectable Light-Load Operation
- Power-Good Indicator
- Support for V_{TT} LDO High-Z in S3
- Output Tracking Discharge Function for the Regulator and V_{TT} LDO
- Cycle-by-Cycle Valley/Peak-Current Limit
- Latch-Off Mode Output Undervoltage (UVP), Overvoltage (OVP), and Overtemperature (OTP)
- Input and Bias Undervoltage (UVLO)
- RoHS-Compliant and Halogen-Free
- Compact Package: QFN3mm×3mm-20

Applications

- LCD TV/3DTV
- Set-Top Box
- Notebook
- High-Power AP

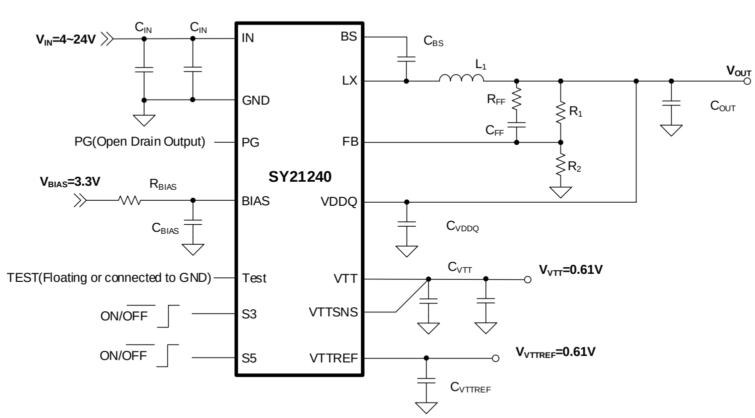


Figure 1. Typical Application Circuit

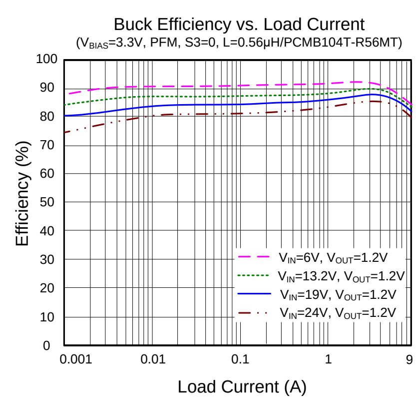


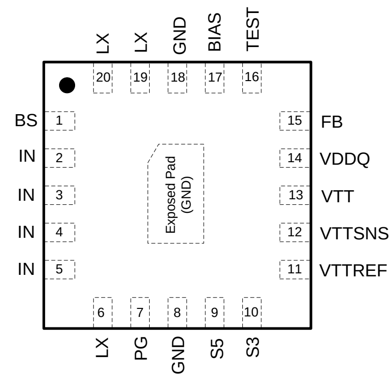
Figure 2. Efficiency vs. Load Current

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY21240RAC	QFN3×3-20 RoHS-Compliant and Halogen-Free	**BCL*xyz***

x = year code, y = week code, z = lot number code

Pinout (top view)



Pin Description

Pin No	Pin Name	Pin Description
1	BS	Bootstrap pin. High-side gate driver supply. Connect a 0.1µF ceramic capacitor between the BS and the LX pins.
2, 3, 4, 5	IN	Input pin. Decouple this pin to the GND pin with at least a 20µF ceramic capacitor.
6, 19, 20	LX	Inductor pin. Connect this pin to the switching node of the inductor.
7	PG	Power-good indicator. Open-drain, high-impedance output when the output voltage is within 90% to 120% of the regulation point.
8, 18, EP	GND	Ground pin.
9	S5	S5 signal input. Internally pulled low with an approximately 1MΩ resistor. This pin is also used for controlling the operating mode of the regulator under light-load conditions when the output is within the regulation range. If this pin is driven with a voltage less than 1.6V, the converter operates in ultrasonic mode (USM). If the voltage on this pin is larger than 2.2V, the converter operates in pulse-frequency-modulation mode (PFM).
10	S3	S3 signal input. Internally pulled low with an approximately 1MΩ resistor.
11	V_{TTREF}	Reference output pin with ±10mA output current capability. $V_{VTTREF} = V_{VDDQ}/2$ + 10mV. Decouple this pin to the GND pin with at least a 1.0µF ceramic capacitor.
12	V_{TTSNS}	V_{TT} LDO remote-sense input. Connect this pin using one Kelvin connection with the positive side of the V_{TT} output capacitor.
13	V_{TT}	Power output of the V_{TT} LDO. $V_{VTT} = V_{VDDQ}/2$ + 10mV. Decouple this pin to the GND pin with at least a 22µF ceramic capacitor.
14	V_{DDQ}	Power supply for the V_{TT} LDO. Connect V_{DDQ} to the output capacitor of the regulator directly with a thick (>30 mil) trace. Do not leave this pin floating.
15	FB	Output feedback pin. Connect this pin to the center point of the output resistor-divider to program the output voltage: V_{SET} = 0.6 × (1 + R1/R2).
16	TEST	For factory use only. Leave this pin floating or connect it to GND.
17	BIAS	External 3.3V V_{CC} input. Power supply for internal circuitry. Use an RC filter circuit between this pin and the supply source.

Block Diagram

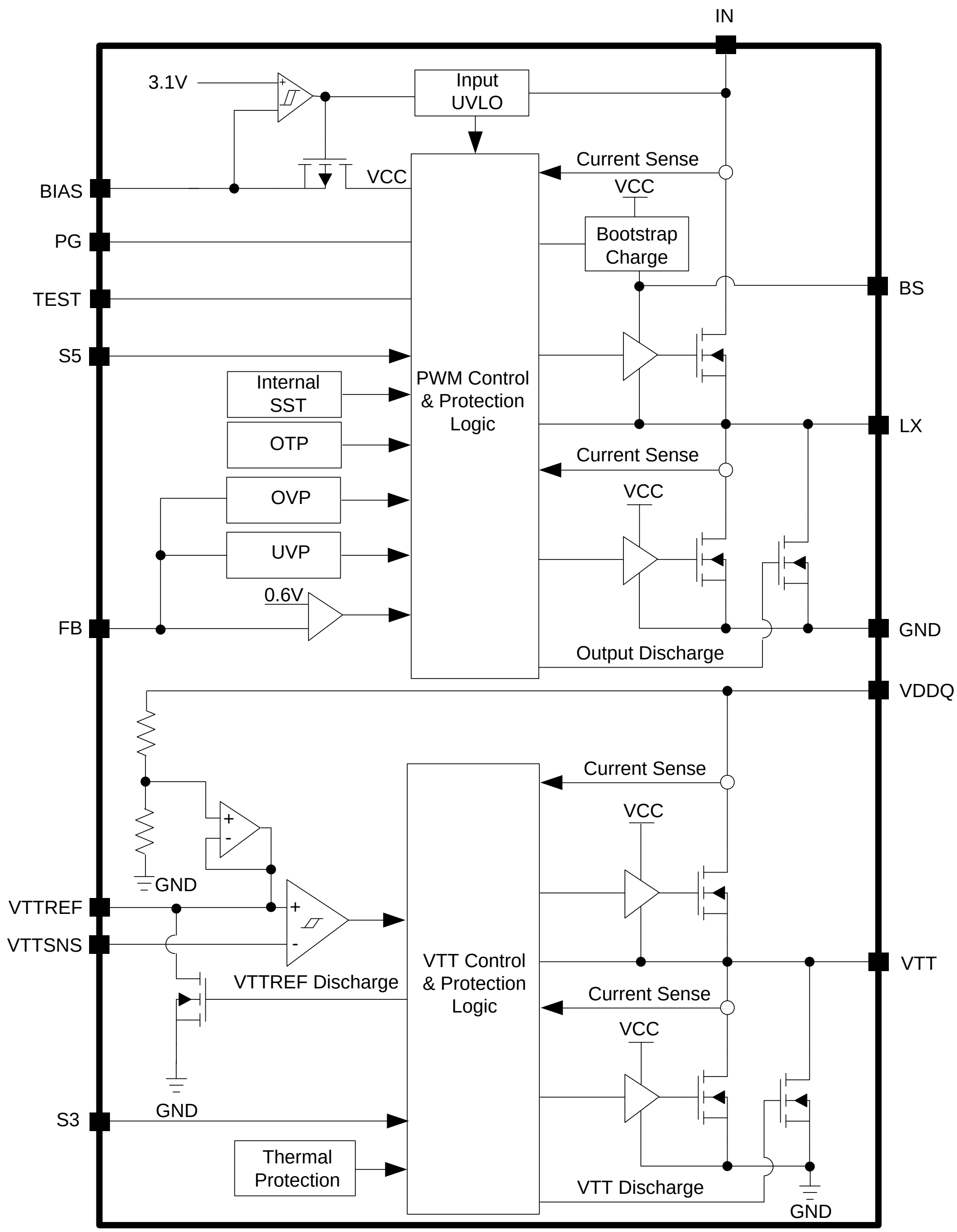


Figure 3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN	-0.3	26	V
IN-LX, LX, PG, S3, S5, TEST	-0.3	IN + 0.3	
BS-LX, BIAS, VDDQ, VTT, VTTSNS, VTTREF, FB	-0.3	4	
Dynamic LX Voltage in 10ns Duration (3)	GND-5	IN + 3	
Dynamic LX Voltage in 20ns Duration (3)	GND-1	IN + 1	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Min	Max	Unit
θ_{JA} Junction-to-ambient Thermal Resistance		30	°C/W
θ_{JC} Junction-to-case Thermal Resistance		4.5	
P_D Power Dissipation T_A = 25°C		3.33	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4	24	V
BIAS	3.1	3.6	
V_{DDQ}	1	2.5	
Junction Temperature	-40	125	°C
Ambient Temperature	-40	85	

Electrical Characteristics

(V_{IN} = 12V, V_{BIAS} = 3.3V, V_{OUT} = 1.2V, C_{OUT} = 88μF, C_{FF} = 220pF, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		4		24	V
	UVLO Threshold	$V_{IN,UVLO}$	V_{IN} rising			3.95	V
	UVLO Hysteresis	$V_{IN,HYS}$			0.3		V
BIAS	UVLO Threshold	$V_{BIAS,UVLO}$	V_{BIAS} rising	2.8			V
	UVLO Hysteresis	$V_{BIAS,HYS}$			0.2		V
	Shutdown Current	$I_{BIAS,SHDN}$	S3 = S5 = 0			1	μA
	Quiescent Current in S3 State	$I_{BIAS,Q1}$	S3 = 0, S5 = 1, I_{OUT} = 0A, I_{VTTREF} = 0A, V_{OUT} = V_{SET} × 105%		85	110	μA
	Quiescent Current in S0 State	$I_{BIAS,Q2}$	S3 = S5 = 1, I_{OUT} = 0A, I_{VTTREF} = 0A, I_{VTT} = 0A, V_{OUT} = V_{SET} × 105%		125	155	μA
Output	Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
	FB Input Current	I_{FB}	V_{FB} = 3.3V	-50		50	nA
	Discharge Current	I_{DIS}	V_{OUT} = 1.2V		70		mA
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET}		450		μs
	OVP Threshold	V_{OVP}	V_{FB} rising	117	120	123	% V_{REF}
	OVP Hysteresis	$V_{OVP,HYS}$			5		% V_{REF}
	OVP Delay	$t_{OVP,DLY}$	(Note 4)		20		μs
	UVP Threshold	V_{UVP}	V_{FB} falling		33		% V_{REF}
	UVP Delay	$t_{UVP,DLY}$	(Note 4)		10		μs
MOSFET	Top FET $R_{DS(ON)}$	$R_{DS(ON)1}$			27		mΩ
	Bottom FET $R_{DS(ON)}$	$R_{DS(ON)2}$			9		mΩ
	Top FET Current Limit	$I_{LMT,TOP}$			20		A
	Bottom FET Current Limit	$I_{LMT,BOT}$		13.5	16	18	A
	Bottom FET Reverse-Current Limit	$I_{LMT,RVS}$	USM mode	2	3.5	5	A
Enable	S5/S3 Input Voltage High	$V_{S5/S3,H}$		1			V
	S5/S3 Input Voltage Low	$V_{S5/S3,L}$				0.3	V
	S5 Voltage for USM Mode	$V_{S5,USM}$		1		1.6	V
	S5 Voltage for PFM Mode	$V_{S5,PFM}$		2.2		V_{IN}	V
Frequency	Switching Frequency	f_{SW}	V_{OUT} = 1.2V, CCM	510	600	690	kHz
	Ultrasonic Mode Frequency	f_{USM}	USM mode, I_{OUT} = 0A		27		kHz
	Min ON Time	$t_{ON,MIN}$	V_{IN} = V_{INMAX} (Note 4)		50		ns
	Min OFF Time	$t_{OFF,MIN}$			210		ns
Power-Good	Rising Threshold	V_{PG}	V_{FB} rising (good)	87	90	93	% V_{REF}
	Hysteresis	$V_{PG,HYS}$			6		% V_{REF}
	Delay Time	$t_{PG,R}$	Low to high (Note 4)		150		μs
		$t_{PG,F}$	High to low (Note 4)		15		μs
	Low Voltage	$V_{PG,LOW}$	V_{FB} = 0V, I_{PG} = 2mA			0.3	V
V_{DDQ}	Input Voltage Range	$V_{VDDQ,IN}$		1		2.5	V
	Input Current in S0 State	I_{VDDQ}	S3 = 1, S5 = 1, V_{VDDQ} = 1.2V, I_{VTTREF} = 0A, I_{VTT} = 0A		7	15	μA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
V_{TT}	Output Source Current Limit	$I_{LMT,VTT,SOU}$	V_{TT} source current	1.6			A
	Output Sink Current Limit	$I_{LMT,VTT,SIN}$	V_{TT} sink current	1.6			A
	Output Error $V_{VTT,ERR}$ = $\lvert V_{VTT}$ - (V_{VDDQ}/2 + 10mV)$\rvert$	$V_{VTT,ERR}$	V_{VDDQ} = 1.2V, I_{VTT} = 0A		5	15	mV
V_{TTREF}	Output Source Current Limit	$I_{LMT,VTTREF,SOU}$	V_{TTREF} source current	20			mA
	Output Sink Current Limit	$I_{LMT,VTTREF,SIN}$	V_{TTREF} sink current	20			mA
	V_{TTREF} Output Voltage Tolerance $V_{VTTREF,TOL}$ = $\lvert V_{VTTREF}$ - (V_{VDDQ}/2 + 10mV)$\rvert$	$V_{VTTREF,TOL}$	V_{VDDQ} = 1.2V, I_{VTT} = 0A		5	15	mV
			V_{VDDQ} = 1.2V, V_{TTREF} source 10mA		15	25	mV
			V_{VDDQ} = 1.2V, V_{TTREF} sink 10mA		15	25	mV
OTP	OTP Temperature	T_{OTP}	T_J rising (Note 4)		150		°C
	OTP Temperature Hysteresis	$T_{OTP,HYS}$	(Note 4)		15		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a 8.5cm×8.5cm size, four-layer Silergy Evaluation Board with 2-oz copper.

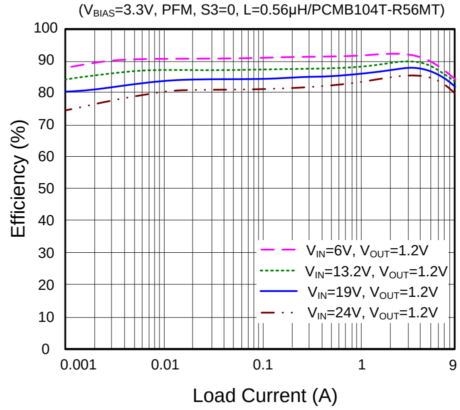
Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Guaranteed by design.

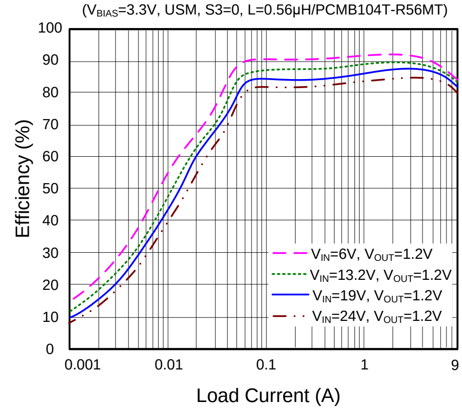
Typical Performance Characteristics

(T_A = 25°C, V_{IN} = 12V, V_{BIAS} = 3.3V, V_{OUT} = 1.2V, L = 0.56μH, C_{OUT} = 88μF, C_{VTT} = 22μF, C_{VTTREF} = 1μF, unless otherwise noted)

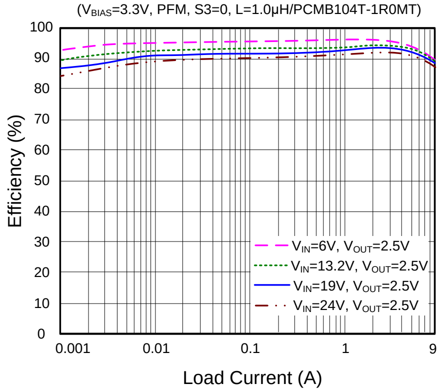
Buck Efficiency vs. Load Current
(V_{BIAS}=3.3V, PFM, S3=0, L=0.56μH/PCMB104T-R56MT)



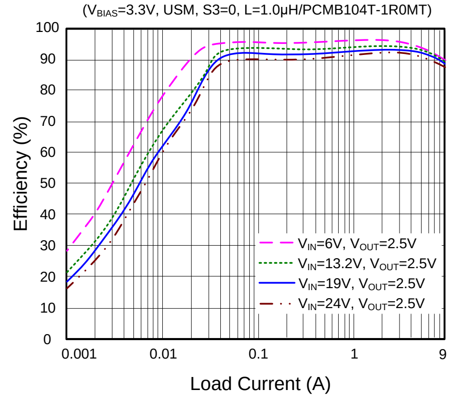
Buck Efficiency vs. Load Current
(V_{BIAS}=3.3V, USM, S3=0, L=0.56μH/PCMB104T-R56MT)



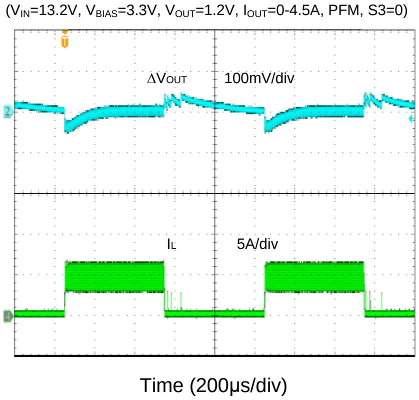
Buck Efficiency vs. Load Current
(V_{BIAS}=3.3V, PFM, S3=0, L=1.0μH/PCMB104T-1R0MT)



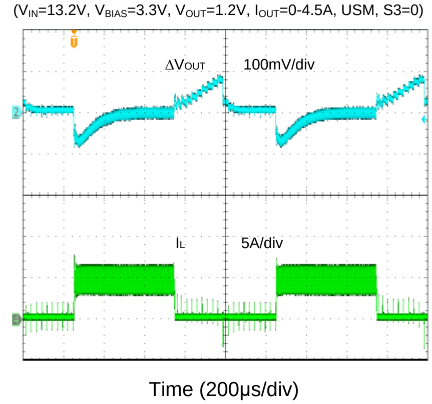
Buck Efficiency vs. Load Current
(V_{BIAS}=3.3V, USM, S3=0, L=1.0μH/PCMB104T-1R0MT)



Buck Load Transient
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0-4.5A, PFM, S3=0)

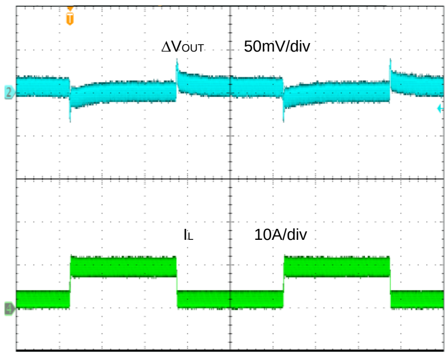


Buck Load Transient
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0-4.5A, USM, S3=0)



Buck Load Transient

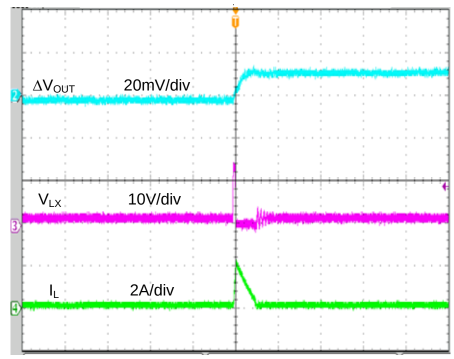
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.9A-9A, S3=0)



Time (200μs/div)

Buck Output Ripple

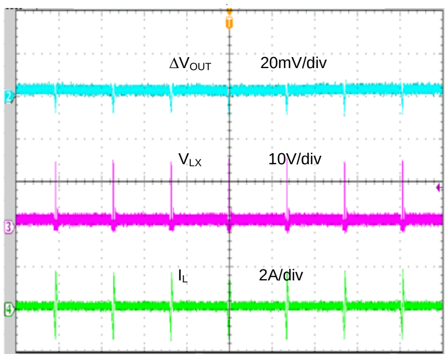
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A, PFM, S3=0)



Time (2μs/div)

Buck Output Ripple

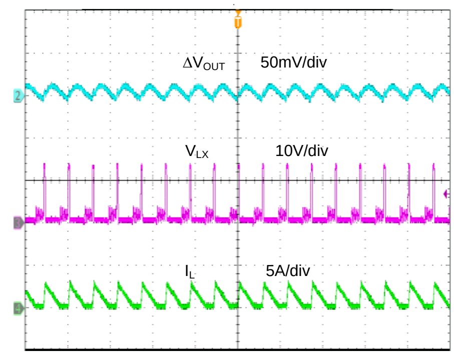
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A, USM, S3=0)



Time (20μs/div)

Buck Output Ripple

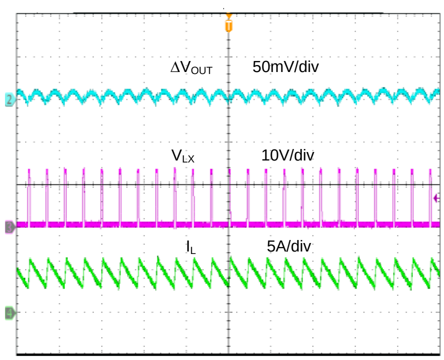
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0.9A, S3=0)



Time (4μs/div)

Buck Output Ripple

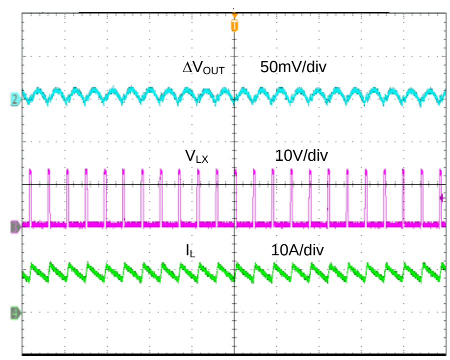
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=4.5A, S3=0)



Time (4μs/div)

Buck Output Ripple

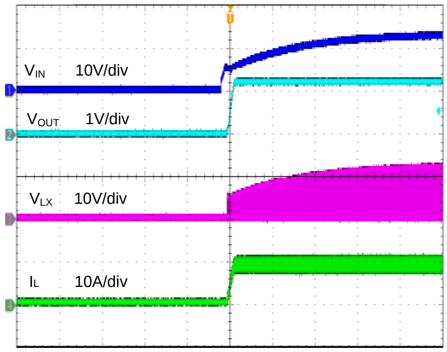
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (4μs/div)

Buck Startup from V_{IN}

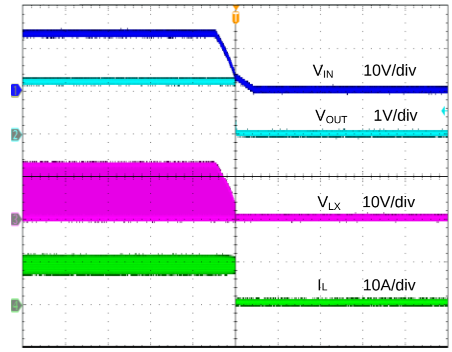
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (2ms/div)

Buck Shutdown from V_{IN}

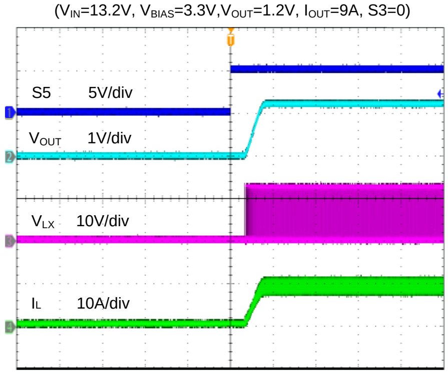
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (2ms/div)

Buck Startup from S5

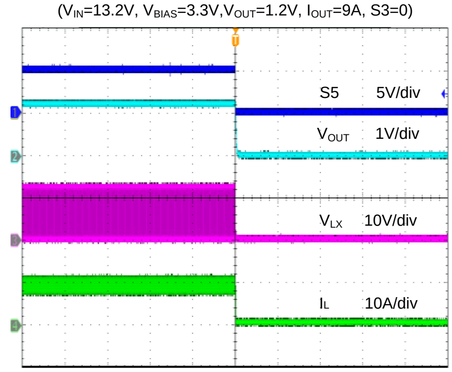
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (800µs/div)

Buck Shutdown from S5

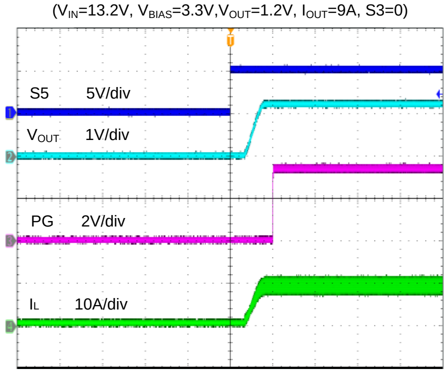
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (800µs/div)

PG Test When S5 On

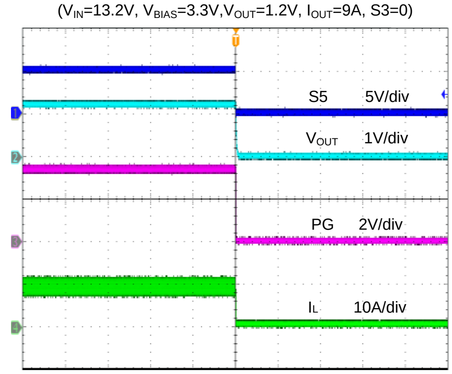
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (800µs/div)

PG Test When S5 Off

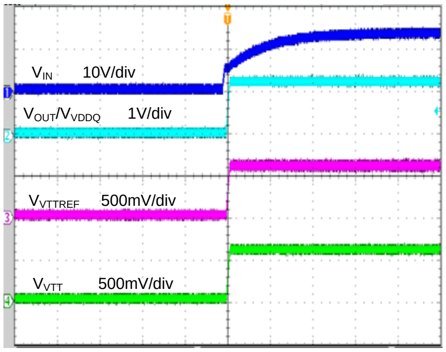
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, S3=0)



Time (800µs/div)

VTT Startup from V_{IN}

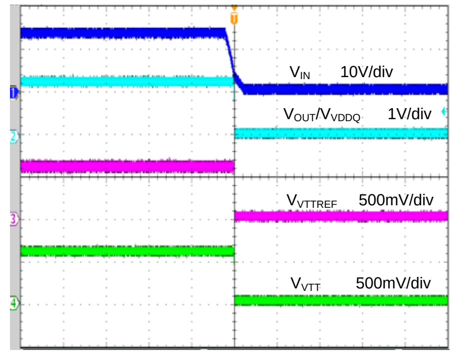
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, I_{VTT}=1A)



Time (4ms/div)

VTT Shutdown from V_{IN}

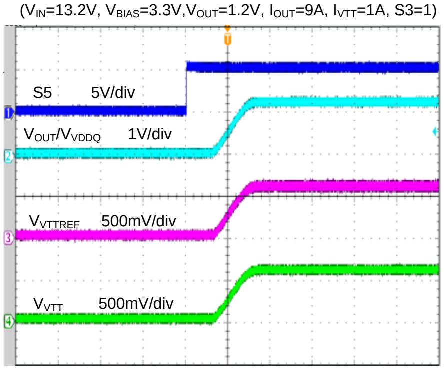
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, I_{VTT}=1A)



Time (4ms/div)

VTT Startup from S5

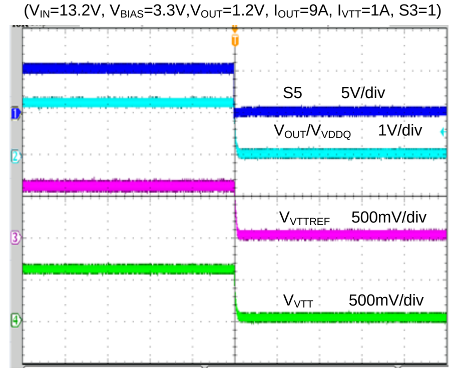
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, I_{VTT}=1A, S3=1)



Time (400µs/div)

VTT Shutdown from S5

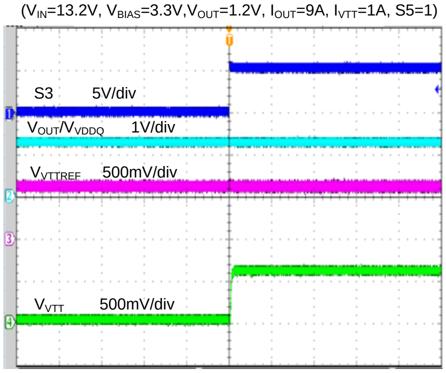
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, I_{VTT}=1A, S3=1)



Time (400µs/div)

VTT Startup from S3

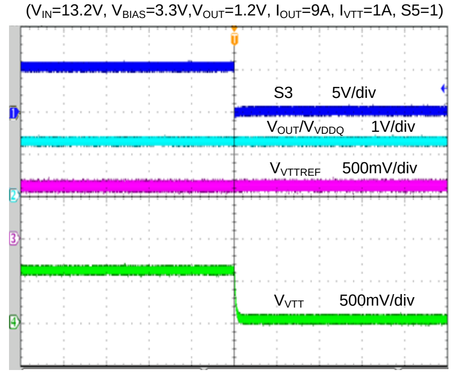
(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, I_{VTT}=1A, S5=1)



Time (400µs/div)

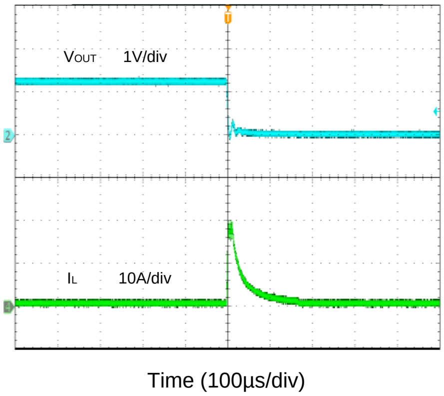
VTT Shutdown from S3

(V_{IN}=13.2V, V_{BIAS}=3.3V,V_{OUT}=1.2V, I_{OUT}=9A, I_{VTT}=1A, S5=1)

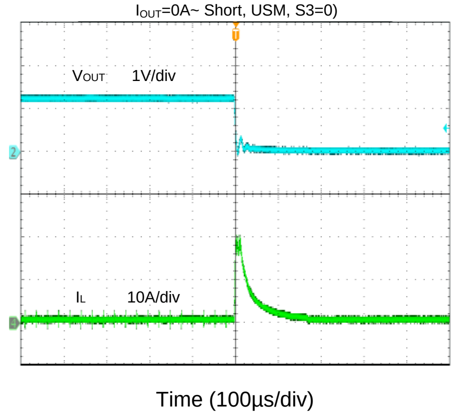


Time (400µs/div)

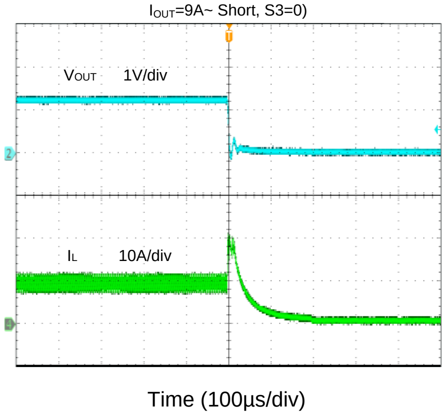
Buck Output Short Circuit
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A~ Short, PFM, S3=0)



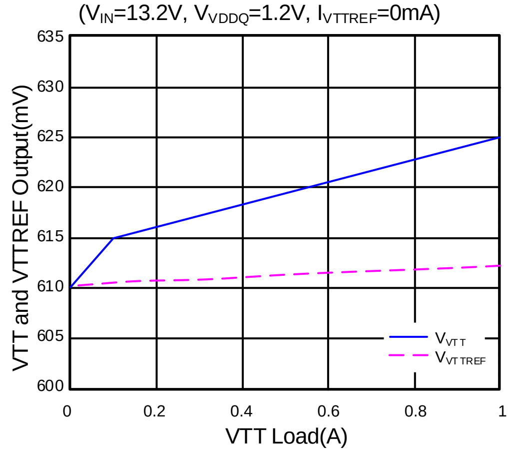
Buck Output Short Circuit
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=0A~ Short, USM, S3=0)



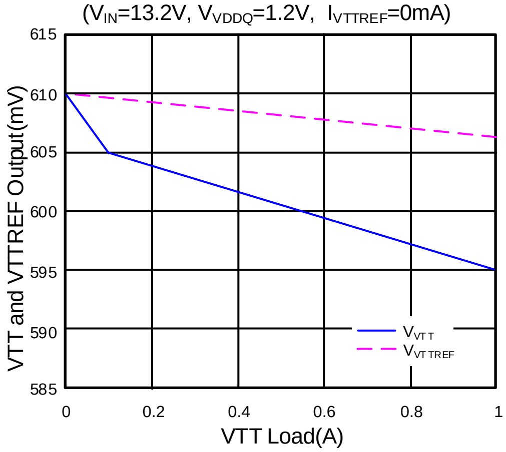
Buck Output Short Circuit
(V_{IN}=13.2V, V_{BIAS}=3.3V, V_{OUT}=1.2V, I_{OUT}=9A~ Short, S3=0)



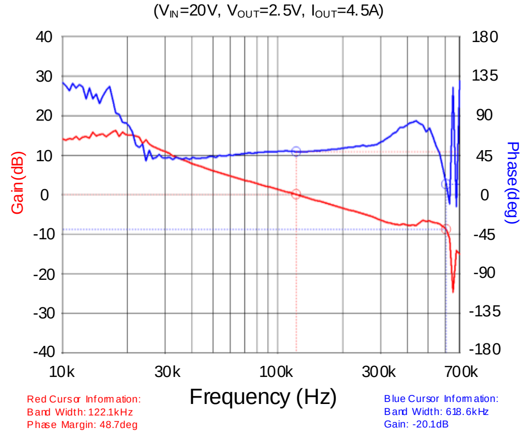
VTT Load Regulation (Sink Current)
(V_{IN}=13.2V, V_{VDDQ}=1.2V, I_{VTTREF}=0mA)



VTT Load Regulation (Source Current)
(V_{IN}=13.2V, V_{VDDQ}=1.2V, I_{VTTREF}=0mA)



Bode Plot
(V_{IN}=20V, V_{OUT}=2.5V, I_{OUT}=4.5A)



Detailed Description

General Features

Constant-on-time Architecture

The one-shot circuit or on-time generator, which determines how long to turn on the high-side power switch, is fundamental to any constant-on-time (COT) architecture. Each on-time (t_{ON}) is a fixed period internally calculated to operate the step-down regulator at the desired switching frequency, considering the input and output voltage ratio, $t_{ON} = (V_{OUT}/V_{IN}) \times (1/f_{SW})$. For example, considering that a hypothetical converter targets 1.2V output from a 10V input at 600kHz, the target on-time is (1.2V/10V) × (1/600kHz) = 200ns. Each t_{ON} pulse is triggered by the feedback comparator when the output voltage measured at the FB pin drops below the internal voltage reference value. After one t_{ON} period, a minimum off-time ($t_{OFF,MIN}$) is imposed before any further switching is initiated, even if the output voltage is less than the target. This approach avoids making any switching decisions during the noisy periods immediately after switching events, or while the switching node (LX) is rapidly rising or falling.

There is no fixed clock in the COT architecture, so the high-side power switch can turn on almost immediately after a load transient. Subsequent switching pulses can be quickly initiated, ramping the inductor current up to meet load requirements with minimal delays. Conventional current-mode or voltage-mode control methods determine when to turn off the high-side power switch and turn on the low-side synchronous rectifier based on current feedback, feedback voltage, internal ramps, and internal compensation signals, so these must all be monitored. These small signals are difficult to observe in a noisy switching environment immediately after switching large currents, which makes such architectures difficult to use.

Minimum Duty Cycle and Maximum Duty Cycle

There is no limitation for minimum duty cycle in COT architecture. This is because when the on-time is close to the minimum value, the switching frequency can be reduced as needed to always ensure proper operation.

The SY21240 can operate with an input voltage as low as 4V to generate an output voltage as high as 2.5V across the entire temperature range (T_J = -40–125°C).

Instant-PWM Operation

Silergy's instant-PWM control method adds several proprietary improvements to the traditional COT architecture. First, whereas most legacy COT implementations require a dedicated connection to the output voltage terminal to calculate the t_{ON} duration, the instant-PWM control method derives this signal internally.

Additionally, it optimizes operation with low-ESR ceramic output capacitors. In many applications it is desirable to utilize very low ESR ceramic output capacitors, but legacy COT regulators may become unstable in these cases because the beneficial ramp signal that results from the inductor current flowing into the output capacitor may become too small to maintain stable operation. For this reason, instant-PWM synthesizes a virtual replica of this signal internally. This internal virtual ramp and the feedback voltage are combined and compared to the reference voltage. When the sum is lower than the reference voltage, the t_{ON} pulse is triggered as long as the minimum t_{OFF} has been satisfied and the inductor current measured flowing through the low-side synchronous rectifier is lower than the bottom FET current limit. When the t_{ON} pulse is triggered, the low-side synchronous rectifier turns off and the high-side power switch turns on. The inductor current then ramps up linearly during the t_{ON} period. At the end of the t_{ON} period, the high-side power switch turns off, the low-side synchronous rectifier turns on, and the inductor current ramps down linearly.

This action also initiates the minimum t_{OFF} timer to ensure sufficient time for stabilizing any transient conditions and settling of the feedback comparator before the next cycle is initiated. This minimum t_{OFF} is relatively short so that transient t_{ON} can be retriggered with minimal delay during high-speed load, allowing the inductor current to ramp quickly and provide sufficient energy to the load.

In order to avoid shoot-through, a dead time (t_{DEAD}) is generated internally between the high-side power switch turn-off and the low-side synchronous rectifier on-period or the low-side synchronous rectifier turn-off and the high-side power turn-on period.

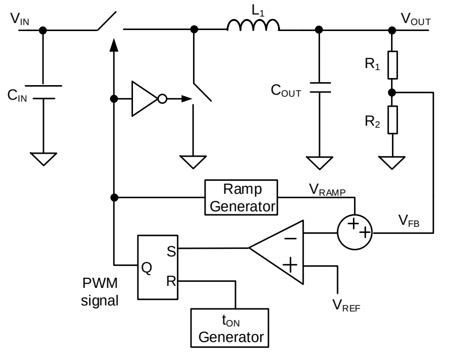


Figure 4. Instant PWM

Light-Load Operation Mode Selection

PFM or USM light load operation is selected using the S5 pin. S5 is not only used as an enable pin, but also for mode selection to control the operation of the regulator under light-load conditions, after the output is within the regulation range. When the voltage on this pin is lower than 1.6V and higher than its rising threshold, the regulator operates under ultrasonic mode (USM). If the voltage on this pin is greater than 2.2V, the buck regulator operates under pulse-frequency modulation mode (PFM).

If the PFM light-load operation is selected, under light load conditions (typically when $I_{OUT} < ½ \times \Delta I_L$), the current through the low-side synchronous rectifier will ramp to near zero before the next t_{ON} time. When this occurs, the low-side synchronous rectifier turns off, preventing recirculation current that can seriously reduce efficiency under light-load conditions. As the load current is further reduced and the combined feedback and ramp signals remain much greater than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed. The apparent operating switching frequency will drop accordingly, further enhancing efficiency. The switching frequency can be in the audible range under deep light-load or no-load conditions. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The device enters CCM once the load current exceeds this threshold. Above this level, the switching frequency stays fairly constant over the entire output current range. The transition level of the load current is determined as follows:

$$I_{OUT\_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1-D)}{2 \times f_{SW} \times L_1}$$

If USM light-load operation is selected, the control loop keeps the switching frequency above the audible frequency range, even under deep light-load or null-load conditions. Once the device detects that both the high-side power switch and the low-side synchronous rectifier turn off for more than a specified duration, it forces the low-side synchronous rectifier to turn on in advance of one t_{ON} cycle and discharge the output capacitor in order to keep the switching frequency is out of audio range. A separate control loop is used to force the low-side synchronous rectifier on to prevent the output voltage from becoming too high.

Bias Input Supply

The SY21240 requires a bias input supply to power the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a 4.7µF low-ESR ceramic capacitor from BIAS to GND if the supply voltage is sourced by a clean power rail. Connect a 5.1Ω resistor before the capacitor to reduce the ripple, if necessary.

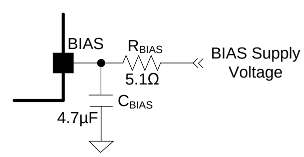


Figure 5. Bias input supply

Input and Bias Undervoltage Lockout (UVLO)

To prevent operation before all internal circuitry is ready, and to ensure that the power and synchronous rectifier switches can operate properly, instant-PWM incorporates two input undervoltage lockout protections: input UVLO and bias UVLO. The SY21240 remains in a low-current state and all switching actions are inhibited until V_{IN} and V_{BIAS} exceed their respective UVLO (rising) thresholds. At that time, if S5 is enabled, the device will start up by initiating a soft-start ramp. If V_{IN} falls below $V_{IN,UVLO}$ by more than the input UVLO hysteresis, or if V_{BIAS} falls below $V_{BIAS,UVLO}$ by more than the bias UVLO hysteresis, the device will stop switching.

The input UVLO threshold can be increased for applications that require it by using a resistor-divider as shown in Figure 6. For calculating the resistor values, the internal pulldown resistor connected to S5 (approximately 1MΩ) must be taken into account.

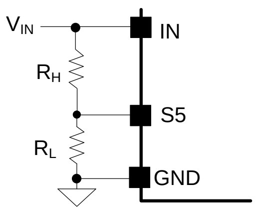


Figure 6. UVLO adjustment

S5/S3 Control

The SY21240 has two enable pins to control the synchronous buck regulator, V_{TT} LDO and buffered reference V_{TTREF}. When the input voltage and the bias voltage both exceed their own UVLO (rising) threshold, the voltages at the S5 and S3 pins are not allowed to be 2V higher than the input voltage at the same time. This can be easily achieved by making sure that these pins are driven low during startup.

The buck regulator, V_{TTREF}, and V_{TT} are all turned on under S0 state (S5 = S3 = high). Under S3 state (S3 = low, S5 = high), only V_{DDQ} and V_{TTREF} outputs are turned on while V_{TT} is turned off and left in a high-impedance state (high Z). The V_{TT} output floats and does not sink or source current while in this state. Under S4/S5 states (S5 = S3 = low), the buck regulator, V_{TTREF}, and V_{TT} outputs are all turned off, and discharge circuits are enabled. V_{TTREF} and V_{TT} outputs track V_{DDQ} discharge after entering S4/S5 state. See S5/S3 control logic details in Table 1.

Table 1. S5/S3 Control Logic

S3	S5	STATE	BUCK	V_{TTREF}	V_{TT}
High	High	S0	On	On	On
Low	High	S3	On	On	Off (High-Z)
Low	Low	S4/S5	Off (Discharge)	Off (Discharge)	Off (Discharge)

The S5/S3 inputs are high-voltage-capable inputs with logic-compatible thresholds. When S5/S3 are driven above 1V, normal device operation is enabled. When S5/S3 are driven below 0.3V, the device will be shut down, reducing bias input current to less than 1.0µA.

It is not recommended to connect S5/S3 to the IN pin directly. Use a resistor with a value between 1kΩ and 1MΩ if S5/S3 are pulled high to IN.

Startup and Shutdown

The SY21240 incorporates an internal soft-start circuit to smoothly ramp the outputs to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 450µs, which avoids high current flow and transients during startup. The startup and shutdown sequences are shown in Figure 6.

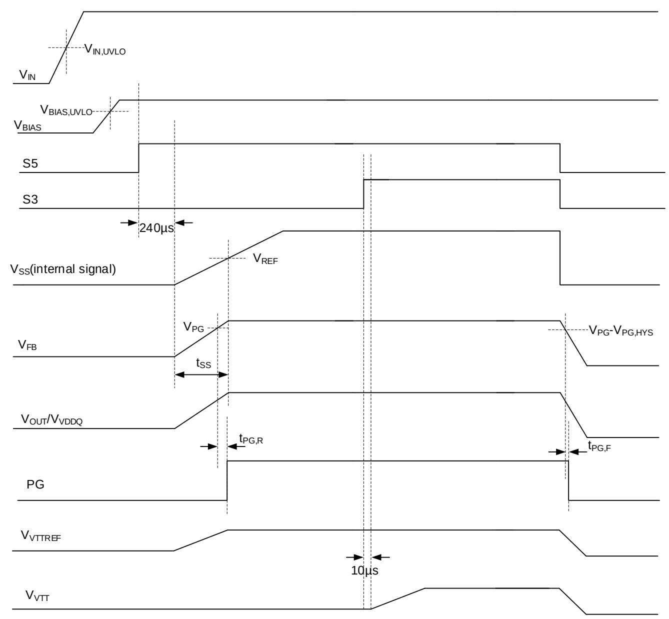


Figure 7. Startup and shutdown sequence

If the output is pre-biased to a certain voltage before startup, the device disables the switching of both the high-side power switch and the low-side synchronous rectifier until the voltage on the internal soft start circuit voltage V_{SS} exceeds the sensed output voltage at the FB node.

Output Discharge and V_{TTREF}/V_{TT} Discharge

The SY21240 discharges the output voltage when the converter shuts down (from V_{IN} falling, S5 driven low, or thermal shutdown), so that output voltage can be discharged in a minimal amount of time, even if the output load current is zero. The discharge MOSFET in parallel with the low-side synchronous rectifier turns on after the low-side synchronous rectifier turns off when shutdown logic is triggered. The output discharge current is typically 70mA. Note that the discharge MOSFET is not active outside of these shutdown conditions.

V_{TTREF} and V_{TT} discharge MOSFETs are turned on after buck output discharge turn-on actions under S4/S5 state. V_{TTREF} and V_{TT} voltage will track buck converter output voltage proportionally after entering this state.

V_{TT}/V_{TTREF} Output

The SY21240 integrates high-performance, low drop-out linear regulators (V_{TT} and V_{TTREF}) to provide complete DDR3/DDR3L power solutions. The V_{TTREF} is a buffered low-noise output with 10mA source/sink current capability. V_{TTREF} always tracks $V_{VDDQ}/2$ + 10mV using an internal divider. A minimum 1.0μF low-ESR ceramic capacitor must be connected close to the V_{TTREF} terminal for stable operation.

The V_{TT} is connected to an LDO output with 1A source/sink current capability. V_{TT} responds quickly to track V_{TTREF} within ±40mV under all conditions. A minimum 22μF low-ESR ceramic capacitor must be connected close to the V_{TT} terminal. The V_{TTSNS} should make one Kelvin connection with the positive node of the V_{TT} output capacitor.

In order to avoid shoot-through, a ±5mV offset voltage is added to the reference voltage of the V_{TT} and V_{TTREF} sink/source MOSFETs so that the V_{DDQ} input current is small when the V_{TT}/V_{TTREF} output currents are zero, even under state S3.

Output Power-Good Indicator

The buck converter power-good indicator is an open-drain output controlled by a window comparator connected to the feedback signal. If V_{FB} is greater than $V_{PG,R}$ and less than V_{OVP} for at least the power-good delay time (low to high), PG will be high-impedance.

PG should be connected to BIAS or another voltage source through a resistor (e.g., 100kΩ). After the input and bias voltages exceed their respective UVLO (rising) threshold, the PG FET is turned on so that the PG pin is driven low before the output voltage is ready. After the feedback voltage V_{FB} reaches V_{PG}, the PG internal MOSFET is turned off (after one delay time, typical 150μs). When V_{FB} drops to V_{PG} less than the hysteresis $V_{PG,HYS}$ or exceeds V_{OVP} for at least one OVP delay time, PG is pulled low (after a delay time of 15μs, typical).

External Bootstrap Capacitor

The SY21240 integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 0.1μF low-ESR ceramic capacitor to be connected between BS and LX.

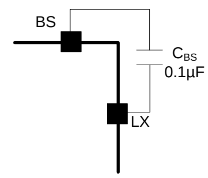


Figure 8. Bootstrap capacitor connection

Fault Protection Modes

Buck Output Current Limit

Instant-PWM architecture incorporates a cycle-by-cycle "valley" current limit. The inductor current is measured in the low-side synchronous rectifier when it turns on and as the inductor current ramps down. If the current exceeds the current-limit threshold, t_{ON} is inhibited until the current returns to a level at or below the limit threshold, as shown in Figure 9.

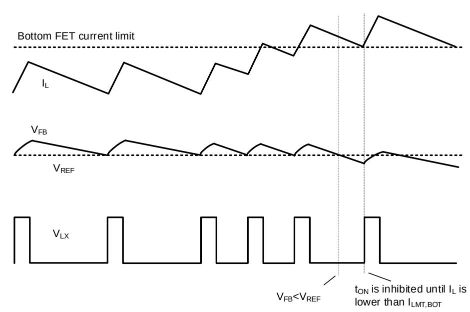


Figure 9. Output current limit

When the valley current-limit is reached, the output current-limit value is given by the following equations:

$$I_{LMT,OUT} = I_{LMT,BOT} + \Delta I_L/2,$$

where ΔL is derived as follows:

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

The overcurrent limit protection (OCP) limits the inductor current. When the load current is higher than the bottom FET current limit threshold by one half of the peak-to-peak inductor ripple current, the output voltage starts to drop. When the feedback voltage falls lower than the undervoltage protection threshold (UVP) and continues for one UVP delay time, the device will latch off. Overtemperature protection may also be triggered under an overcurrent condition, and the device will OTP latch off.

The buck regulator also incorporates a cycle-by-cycle "peak" current limit (top FET current limit). The high-side power-switch current is monitored during t_{ON} time. If the monitored current exceeds the threshold, the high-side power switch is turned off, the low-side synchronous rectifier is turned on, and t_{ON} is inhibited. t_{ON} is no longer inhibited once low-side synchronous-rectifier current is lower than the bottom-FET current-limit value.

V_{TT}/V_{TTREF} Output Current Limit

The V_{TT} LDO has an internal non-latched minimum 1.6A current limit for both sink and source cases. Once the current limit is reached, it adjusts the gate of the sink or source MOSFET to limit the current, at which point the V_{TT} LDO output voltage stops being regulated. Similarly, V_{TTREF} has an internal non-latched current limit of at least 20mA.

Buck Output Undervoltage Protection (UVP)

If V_{OUT} falls below approximately 33% of the target output voltage for approximately 10μs, which may occur if the output short circuits or the load current is higher than the maximum current capability, the output undervoltage protection (UVP) will be triggered, and the device will latch off, as shown in Figure 10. Cycle the S5 input to re-enable the device.

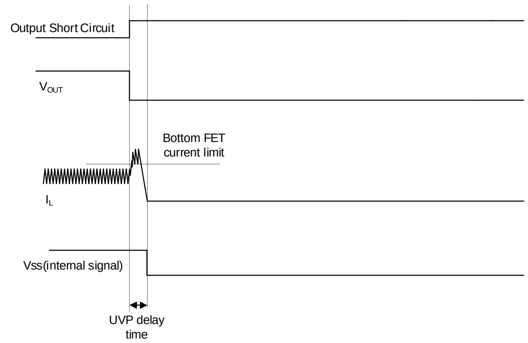


Figure 10. Output undervoltage protection

Buck Output Overvoltage Protection (OVP)

If the output voltage rises above the feedback regulation level, the high-side power switch remains off until the output voltage falls below the target. The behavior under the different conditions is described below.

When operating in PFM light-load mode, if the output voltage remains high, the low-side synchronous rectifier remains on until the inductor current reaches zero and switching is suppressed. Switching is resumed once the output voltage no longer exceeds the OVP threshold, and the combined feedback and ramp signals are lower than the reference voltage. If the output voltage exceeds the output overvoltage threshold for more than the OVP delay time, output overvoltage protection (OVP) is triggered and the device will latch off. Cycle S5 to re-enable the device.

When operating in USM mode, if the output voltage remains high, the low-side synchronous rectifier forced turn-on time will be longer and the inductor current average value will grow increasingly negative as the device attempts to lower the output voltage. This will subsequently trigger the reverse-current limit. If the output voltage continues to rise and exceeds the output overvoltage threshold for more than the OVP delay time, output overvoltage protection (OVP) is triggered and the device will latch off. Cycle the S5 input to re-enable the device. False OVP may occur under USM light mode if the chosen inductance is too small and the reverse-current limit is triggered.

Buck Overtemperature Protection (OTP)

Instant-PWM includes buck converter overtemperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will latch off the device when the buck thermal sensor detects that the junction temperature exceeds 150°C. See Figure 11. Once the junction temperature cools by approximately 15°C, cycle the S5 input to re-enable the device. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

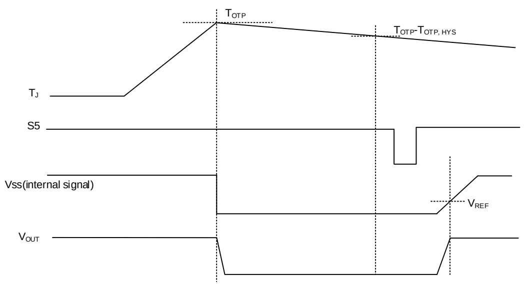


Figure 11. Overtemperature protection

Application Information

Feedback Resistor-Divider R1 and R2

Choose R1 and R2 to program the buck converter output voltage. A value between 10kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. For example, if V_{SET} is 1.2V and R_1 = 100kΩ, then R2 can be calculated as 100kΩ using the following equation:

$$R2 = \frac{0.6V}{V_{SET} - 0.6\text{V}} \times R1$$

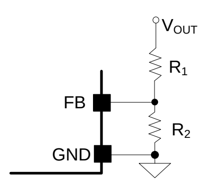


Figure 12. Feedback resistor selection

Buck Inductor Selection

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage.

Instant-PWM operates well over a wide range of inductor values. This flexibility allows for optimization to find the best trade-off of efficiency, cost, and size for a particular application. Selecting a low inductor value will help reduce size and cost, and enhance transient response, but will increase peak inductor ripple current, reducing efficiency and increasing output voltage ripple. Using a low DC resistance (DCR) for the inductors may help reduce DC losses and increase efficiency. Higher inductor values tend to have higher DCR and will slow transient response.

A reasonable compromise between size, efficiency, and transient response can be determined by selecting a ripple current (ΔI_L) approximately 20–50% of the desired full output load current. Start calculating the approximate inductor value by selecting the input and output voltages, the operating frequency (f_{SW}), and the maximum output current ($I_{OUT,MAX}$), and then estimating a ΔI_L as some percentage of that current:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Use this inductance value to determine the actual inductor ripple current (ΔI_L) and required peak-current inductor current $I_{L,PEAK}$.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L_1}$$

$$I_{L,PEAK} = I_{OUT,MAX} + \Delta I_L/2$$

Select an inductor with a saturation current and thermal rating in excess of $I_{L,PEAK}$.

If USM light-load operation is selected, make sure the inductor value is high enough to avoid triggering the reverse-current limit under steady state when the load current is zero.

For maximum efficiency, select an inductor with a low DCR that meets the inductance, size, and cost targets. Low-loss ferrite materials should be considered.

Buck Inductor Design Example

Consider a typical design for a device providing $1.2V_{OUT}$ at 9A from $24V_{IN}$, operating at 600kHz and using target inductor ripple current (ΔI_L) of 40%, or 3.6A. First determine the approximate inductance value:

$$L_1 = \frac{1.2V \times (24V - 1.2V)}{24V \times 600kHz \times 3.6A} = 0.53\mu H$$

Next, select the nearest standard inductance value (in this case 10.56μH) and calculate the resulting inductor ripple current (ΔI_L):

$$\Delta I_L = \frac{1.2V \times (24V - 1.2V)}{24V \times 600kHz \times 0.56\mu H} = 3.39A$$

$$I_{L,PEAK} = 9A + 3.39A/2 = 10.70A$$

The resulting 3.39A ripple current is approximately 37.7% (3.39A/9A), well within the 20–50% target.

$$I_{L,PEAK,RVS} = 2.66A/2 = 1.70A < I_{LIM,RVS}$$

Finally, select an available inductor with a saturation current higher than the resulting $I_{L,PEAK}$ of 10.70A.

Buck Input Capacitor Selection

Input filter capacitors reduce the ripple voltage on the input, filter the switched current drawn from the input supply, and reduce potential EMI. When selecting an input capacitor, be sure to select a voltage rating at least 20% greater than the maximum voltage of the input supply and a temperature rating higher than the system requirements. X5R series ceramic capacitors are most often selected due to their small size, low cost, surge-current capability, and high RMS current ratings over a wide temperature and voltage range. However, systems that are powered by a wall adapter or other long and therefore inductive cabling may be susceptible to significant inductive ringing at the input to the device. In these cases, consider adding some bulk capacitance like electrolytic, tantalum, or polymer type capacitors. Using a combination of bulk capacitors (to reduce overshoot or ringing) in parallel with ceramic capacitors (to meet the RMS current requirements) is helpful in these cases.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

where D is the switching converter duty cycle.

The worst-case condition occurs at D = 0.5, then

$$I_{CIN\_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current.

The input capacitor determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

$$V_{CIN\_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN\_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. Two 10μF X5R capacitors are sufficient in most applications. Place the ceramic input capacitor as close to the device IN and GND pins as possible.

Buck Output Capacitor Selection

Instant-PWM provides excellent performance with a wide variety of output capacitor types. Ceramic and POS types are most often selected due to their small size and low cost. Total capacitance is determined by the transient response and output voltage ripple requirements of the system.

Buck Output Ripple

Output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitors ESR (ESR ripple), as well as the stored charge (capacitive ripple). When considering the total ripple, both should be considered.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$
$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

Consider a typical application with ΔI_L = 3.39A using four 22μF ceramic capacitors, each with an ESR of approximately 6mΩ for a parallel total of 88μF and 1.5mΩ ESR.

$$V_{RIPPLE,ESR} = 3.39A \times 1.5m\Omega = 5.09mV$$
$$V_{RIPPLE,CAP} = \frac{3.39A}{8 \times 88\mu F \times 600kHz} = 8.03mV$$

Total calculated ripple = 13.12mV. The actual capacitive ripple may be higher than the calculated value because the capacitance decreases with the voltage across the capacitor.

Using a 150μF 40mΩ POS cap, the result is as follows:

$$V_{RIPPLE,ESR} = 3.39A \times 40m\Omega = 135.6mV$$
$$V_{RIPPLE,CAP} = \frac{3.39A}{8 \times 150\mu F \times 600kHz} = 4.71mV$$

Total ripple = 140.31mV.

Buck Output Transient Undershoot/Overshoot

If very fast load transients must be supported, consider the effect of the output capacitor on the output transient undershoot and overshoot. The instant-PWM architecture responds quickly to changing load conditions, but additional effects must be considered, especially when using small ceramic capacitors. These capacitors have low capacitance at low output voltages, which results in insufficient stored energy for a good load-transient response. Output-transient undershoot and overshoot have two causes: voltage changes caused by the ESR of the output capacitor, and voltage changes caused by the output capacitance and inductor current slew rate.

ESR undershoot or overshoot may be calculated as $V_{ESR} = \Delta I_{OUT} \times ESR$. Using the ceramic capacitor example above and a fast load transient of ±4.5A, V_{ESR} = ±4.5A × 1.5mΩ = ±6.75mV. The POS capacitor result with the same load transient is V_{ESR} = ±4.5A × 40mΩ = ± 180mV.

Capacitive undershoot (load increasing) is a function of the output capacitance, load step, inductor value, input-output voltage difference, and maximum duty-cycle factor. During a fast load transient, the maximum duty-cycle factor of instant-PWM is a function of t_{ON} and the minimum t_{OFF}, as the control scheme is designed to rapidly ramp the inductor current by grouping together many t_{ON} pulses in this case. The maximum duty-cycle factor D_{MAX} may be calculated as:

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF,MIN}}$$

Given this, the capacitive undershoot may be calculated as:

$$V_{UNDERSHOOT,CAP} = -\frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times (V_{IN,MIN} \times D_{MAX} - V_{OUT})}$$

Consider a 4.5A load increase using the ceramic capacitor case when V_{IN} = 20V. At V_{OUT} = 1.2V, the result is t_{ON} = 100ns, $t_{OFF,MIN}$ = 210ns, D_{MAX} = 100 / (100 + 210) = 0.323, and

$$V_{UNDERSHOOT,CAP} = -\frac{0.56\mu H \times (4.5A)^2}{2 \times 88\mu F \times (20V \times 0.323 - 1.2V)} = -12.25mV$$

Using the POS capacitor case, the above result is

$$V_{UNDERSHOOT,CAP} = -\frac{0.56\mu H \times (4.5A)^2}{2 \times 150\mu F \times (20V \times 0.323 - 1.2V)} = -7.19mV$$

Capacitive overshoot (load decreasing) is a function of the output capacitance, the inductor value and the output voltage.

$$V_{OVERSHOOT,CAP} = \frac{L_1 \times \Delta I_{OUT}^2}{2 \times C_{OUT} \times V_{OUT}}$$

Consider a 4.5A load decrease using the ceramic capacitor case above. At V_{OUT} = 1.2V the result is

$$V_{OVERSHOOT,CAP} = \frac{0.56\mu H \times (4.5A)^2}{2 \times 88\mu F \times 1.2V} = 53.69mV$$

Using the POS capacitor case, the above result is

$$V_{OVERSHOOT,CAP} = \frac{0.56\mu H \times (4.5A)^2}{2 \times 150\mu F \times 1.2V} = 31.50mV$$

Combine the ESR and capacitive undershoot and overshoot to calculate the total overshoot and undershoot for a given application.

Buck Feed-Forward Compensation (R_{FF}, C_{FF})

The SY21240 is internally compensated and optimized for low-duty-cycle applications. However, in some applications, especially where V_{OUT} > 1.2V, the feedback divider attenuates the AC component of the output. In these cases, transient response may be improved by adding feed-forward compensation. Values of R_{FF} = 1kΩ and C_{FF} = 220pF have been shown to perform well in most applications.

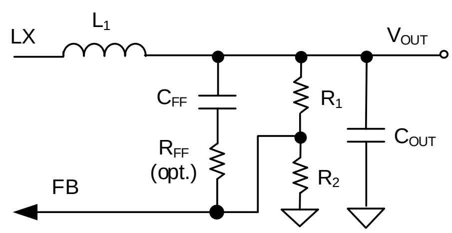


Figure 13. Feed-forward network

When C_{OUT} > 500µF and the minimum load current is low, use the values R_{FF} = 1kΩ and C_{FF} = 2.2nF for the feed-forward network to provide sufficient ripple to the FB pin and enable small output ripple and good transient behavior.

Thermal Design Considerations

The maximum power dissipation depends on multiple factors: PCB layout, IC package thermal resistance, local airflow, and the junction temperature relative to ambient. The maximum power dissipation may be calculated as:

$$P_{D,MAX} = (T_{J,MAX} - T_A) / \theta_{JA}$$

Where, $T_{J,MAX}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

To comply with the recommended operating conditions, the maximum junction temperature is 125°C. The junction-to-ambient thermal resistance θ_{JA} is layout dependent. For the QFN3mm×3mm-20 package, the thermal resistance θ_{JA} is 30°C/W when measured on a standard Silergy four-layer thermal test board. These standard thermal test layouts have a very large area with long 2-oz. copper traces connected to each IC pin and very large, unbroken 1-oz. internal power and ground planes.

Meeting the performance of the standard thermal test board in a typical small evaluation board area requires wide copper traces well-connected to the IC's backside pads leading to exposed copper areas on the component side of the board as well as good thermal via from the exposed pad connecting to a wide middle-layer ground plane and, perhaps, to an exposed copper area on the board's solder side.

The maximum power dissipation at T_A = 25°C may be calculated using the following formula:

$$P_{D,MAX} = (125°C - 25°C) / (30°C /W) = 3.33W$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J,MAX}$ and thermal resistance θ_{JA}. Use the derating curve in figure below to calculate the effect of rising ambient temperature on the maximum power dissipation.

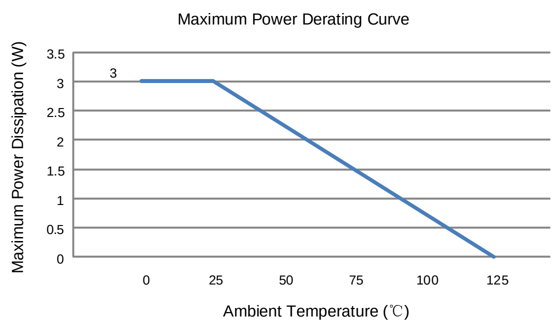
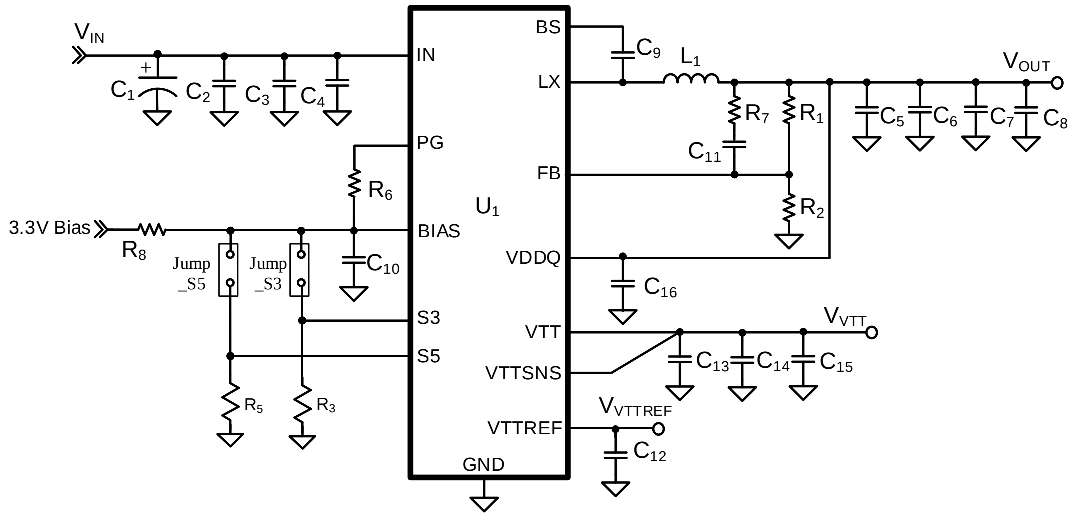


Figure 14. Maximum power dissipation

Application Schematic (V_{OUT} = 1.2V)



BOM List

Designator	Description	Part Number	Manufacturer
U_1	9A, Buck with VTT LDO	SY21240RAC	Silergy
C_1	47μF/50V, Electrolytic Cap		
C_2, C_3	10μF/50V/X5R, 1206	GRM31CR61H106KA12L	mμRata
C_4, C_9, C_{13}	0.1μF/50V/X5R, 0603	GRM188R61H104KA93D	mμRata
C_5, C_6, C_7, C_8, C_{14}, C_{16}	22μF/16V/X5R, 1206	GRM31CR61C226ME15L	mμRata
C_{10}	4.7μF/16V/X5R, 0603	GRM185R61C475KE11D	mμRata
C_{11}	220pF/50V/C0G, 0603	GRM1885C1H221JA01D	mμRata
C_{12}	1.0μF/25V/X5R, 0603	GRM155R61E105KE11D	mμRata
C_{15}	NC		
L_1	0.56μH/25A, inductor	PCMB104T-R56MT	CYNTEC
R_1, R_2, R_6	100kΩ, 1%, 0603		
R_4	NC		
R_3, R_5	1MΩ, 1%, 0603		
R_7	1kΩ, 1%, 0603		
R_8	5.1Ω, 1%, 0603		

Recommended Components for Typical Applications

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C11 (pF)	L1/Part Number
1.2	100	100	220	0.56μH/PCMB104T-R56MT
2.5	100	31.6	47	1.0μH/PCMB104T-1R0MT

Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

- **Buck Input Capacitors:** Place the input capacitors very close to IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND using large copper areas. An additional 0.1μF input ceramic capacitor, placed in parallel is recommended to reduce the input noise.
- **Buck Output Capacitors:** Guarantee the COUT GND connections are using a copper area connected to the GND plane using multiple vias, in order to achieve better accuracy and stability of output voltage.
- **BIAS Capacitor or RC Filter:** Place the BIAS capacitor close to BIAS using a short, direct copper trace to the nearest device GND pin (pin 18). Connect a 5.1Ω resistor before the capacitor if the supply voltage is not a clean DC rail.
- **V_{DDQ} Capacitor and V_{DDQ} Line:** Place the V_{DDQ} capacitor close to V_{DDQ} using a short, direct copper trace to the nearest device GND pin (pin 18). Connect the positive side of the V_{DDQ} capacitor to the output capacitor of the regulator directly with a thick (> 30 mil) trace to avoid a voltage drop on the input of the V_{TT} LDO.
- **V_{TT} and V_{TTREF} Capacitors:** Place the V_{TTREF} output capacitor C_{VTTREF} and the V_{TT} output capacitor C_{VTT} close to the V_{TTREF}/V_{TT} and GND pins, minimizing the loop formed by these connections to achieve better stability and load-transient response for the V_{TT} LDO.
- **V_{TT} Sense Feedback:** Use a Kelvin connection between V_{TTSNS} and the positive side of the V_{TT} output capacitor.
- **Buck Feedback Network:** Place the feedback components (R_{FF}, and C_{FF}) as close to the FF pin as possible. Avoid routing the feedback line near LX, BS, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection between the feedback sampling point and C_{OUT} (rather than connecting it to the inductor output terminal).
- **LX Connection:** Keep LX area small to prevent excessive EMI, while providing wide copper traces to minimize parasitic resistance and inductance. Wide LX copper trace between pin 6 and pin 19, 20 should be used for improved efficiency.
- **BS Capacitor:** Place the BS capacitor on the same layer as the device and keep the BS voltage path (BS, LX, and C_{BS}) as short as possible.
- **Control Signals:** It is not recommended to connect control signals directly to IN. A resistor in a range of 1kΩ to 1MΩ should be used if they are pulled high to the IN voltage rail.
- **GND Vias:** Place an adequate number of vias on the GND layer around the device for better thermal performance. The exposed GND pad should be connected by a copper area larger than its size. Place five GND vias on it for heat dissipation.
- **PCB Board:** A four-layer layout with 2-oz copper is strongly recommended to achieve better thermal performance. The top layer and bottom layer should use large power IN and GND copper areas where possible. The Middle1 layer should be used as the GND layer for conducting heat and shielding the Middle2 layer signal lines from top-layer crosstalk. Place signal lines on the Middle2 layer instead of the other layers so that the other power planes are not cut.

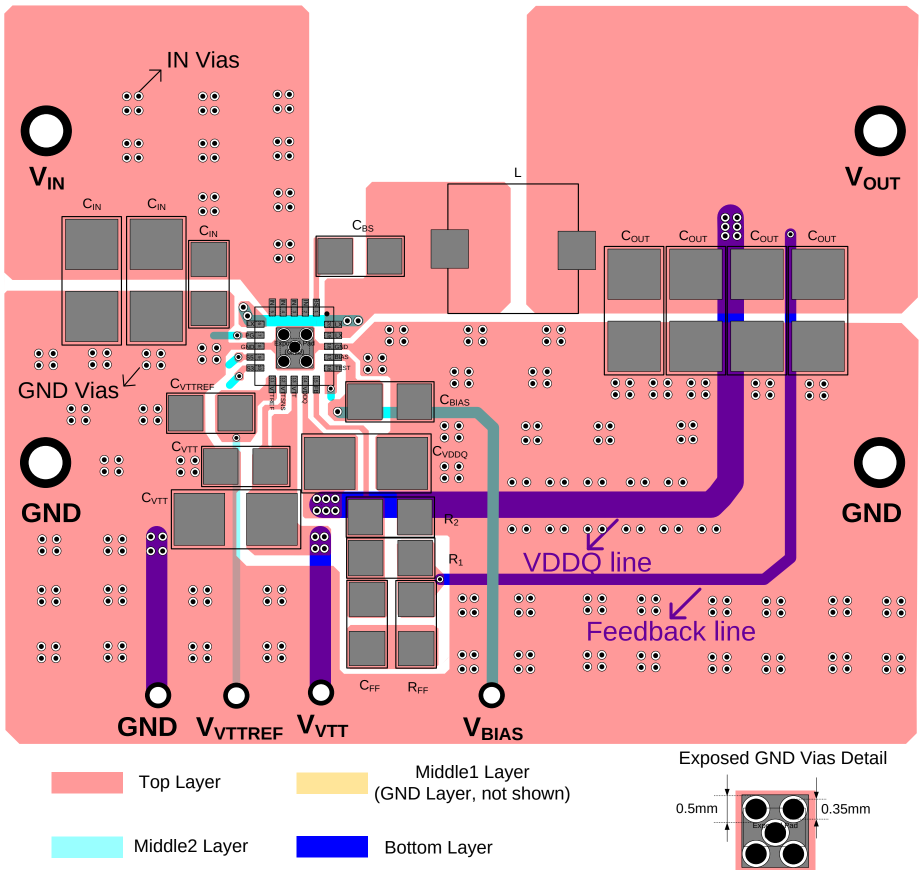
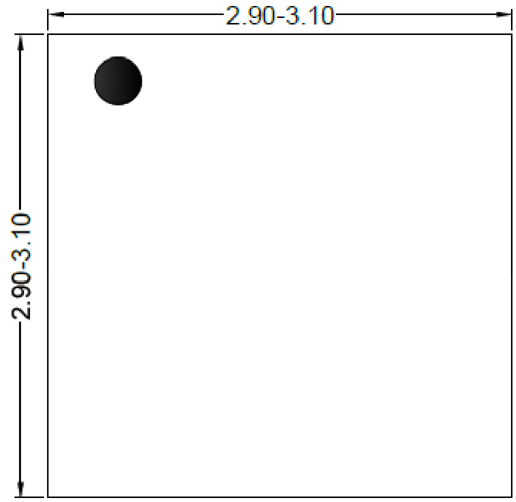
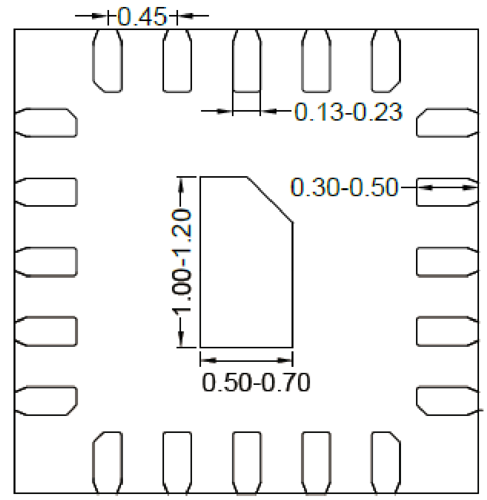


Figure 15. PCB Layout Suggestion

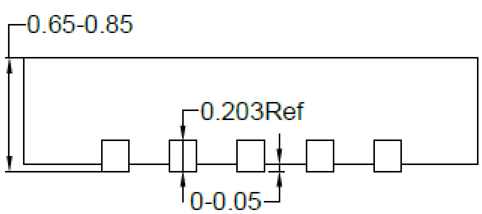
QFN3×3-20 Package Outline



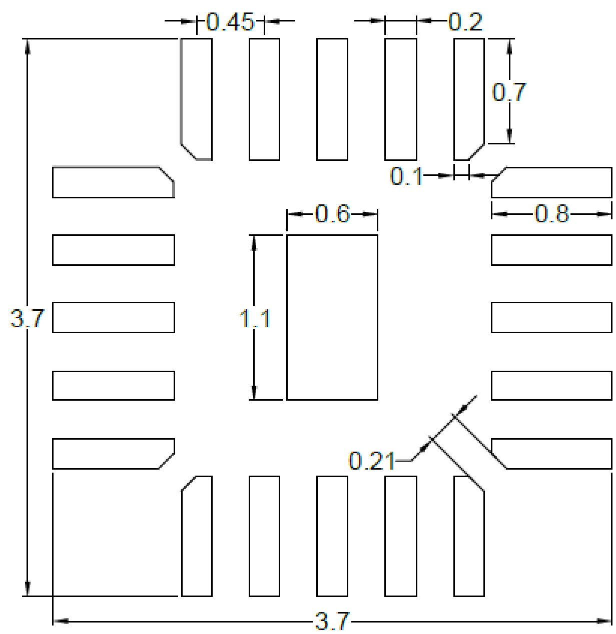
Top view



Bottom view



Side view



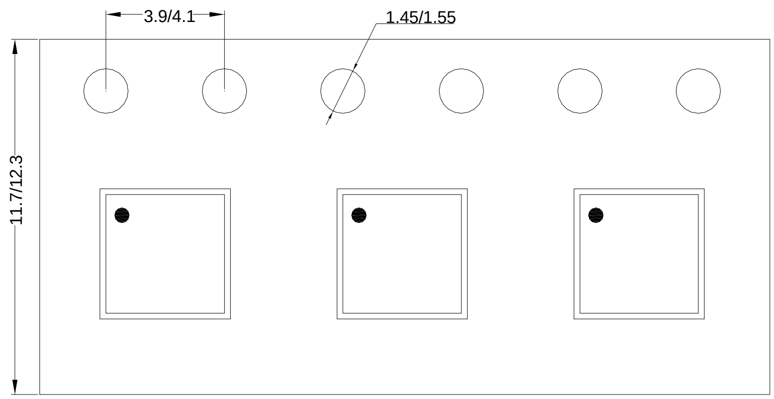
Recommended PCB layout

(Reference only)

Note: *All dimensions are in millimeters and exclude mold flash and metal burr.*

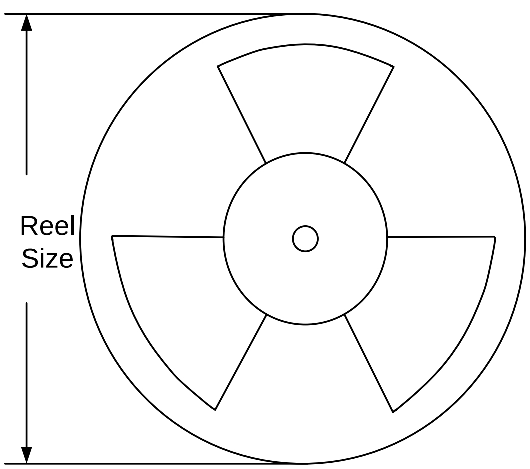
Taping and Reel Specification

QFN3×3-20 taping orientation



Feeding direction →

Carrier tape and reel specification for packages



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
QFN3×3	12	8	13"	400	400	5000

Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warrantied. Please make sure that you have the latest revision.

Date	Revision	Change
Jan.22, 2022	Revision 1.0	Production Release
Jan.22, 2021	Revision 0.9B	Add (IN-LX) voltage in Absolute Maximum Ratings.
Jul.07, 2020	Revision 0.9A	1. Output current of the Regulator changes from 10A continuous to 9A continuous; Update the related waveforms and the calculation formulas.
Apr.28, 2020	Revision 0.9	Initial Release

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