



SILERGY

SY2A27352

300mA, 36V Fast-Response LDO Regulator with Reset Output

General Description

The SY2A27352 is an automotive grade, 300mA high-current capacity linear regulator with ultra-low ground current and low drop-out voltage. The device offers protective features, including an over-current limit, output short protection, and over-temperature protection. The SY2A27352 has an adjustable output that can be configured using two external resistors.

The device offers an open-drain, active low reset output which can be used to hold a microcontroller in reset until the input voltage is above the preconfigured threshold. The reset duration can be adjusted using an optional, external capacitor.

The SY2A27352 is available in a compact SO8E package.

Features

- Wide Input Voltage Range: 4V to 36V
- Adjustable Output Voltage
- Low-Dropout Voltage: 300mV at Full Load 300mA
- High-Current Capability: 300mA Over Full Temperature Range
- Low Ground Current
- Over-Current Limit Protection
- Output Short Circuit Protection (Hiccup Mode)
- Over-Temperature Protection
- Reset Output with Programmable Timeout Period
- Package: SO8E
- RoHS Compliant and Halogen Free
- Automotive AEC- Q100 Grade 1 Qualified

Applications

- Industrial/Automotive Applications
- Portable/Battery-Powered Equipment
- Ultra-Low-Power Microcontrollers
- Cellular Handsets
- Medical Imaging

Typical Application

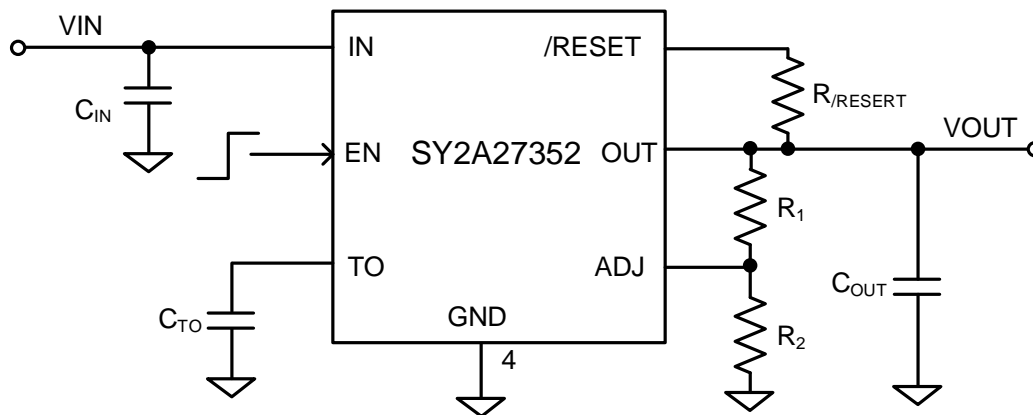


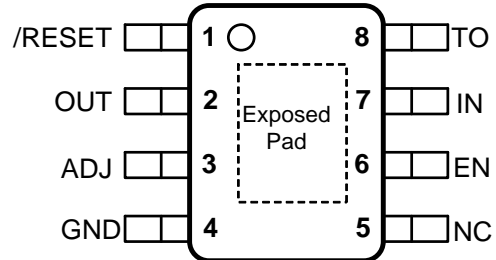
Figure 1. Typical Application Schematic

Ordering Information

Ordering Part Number	Package Type	Top Mark
SY2A27352FCA	SO8E RoHS Compliant and Halogen Free	BTExyz

x=year code, y=week code, z= lot number code

Pinout (top view)



Pin Name	Pin Number	Pin Description
/RESET	1	Open drain reset output. /RESET low when OUT is below the reset threshold and remains low for the reset timeout period after the reset conditions end. If no capacitor connects at the TO pin, RESET pulls high immediately after V_{OUT} exceeds the reset threshold. If it isn't used, leave it floating or connect to GND.
OUT	2	Output pin. Bypass this pin to the ground pin with a 4.7 μ F output capacitor.
ADJ	3	Output voltage adjustment pin. Feedback the output voltage through the resistor voltage divider network. $V_{OUT}=0.6 \times (1+R_1/R_2)$.
GND	4	Ground pin.
NC	5	No connection.
EN	6	Enable pin. Pull it low to shutdown or pull it high to enable; do not leave it floating.
IN	7	Power supply input. Bypass this pin to the ground pin with a 4.7 μ F capacitor.
TO	8	Reset timeout programming pin. Connect a capacitor from this pin to GND for different reset timeout times.
	Exposed Pad	The exposed pad should be connected to the ground plane for better thermal performance.

Block Diagram

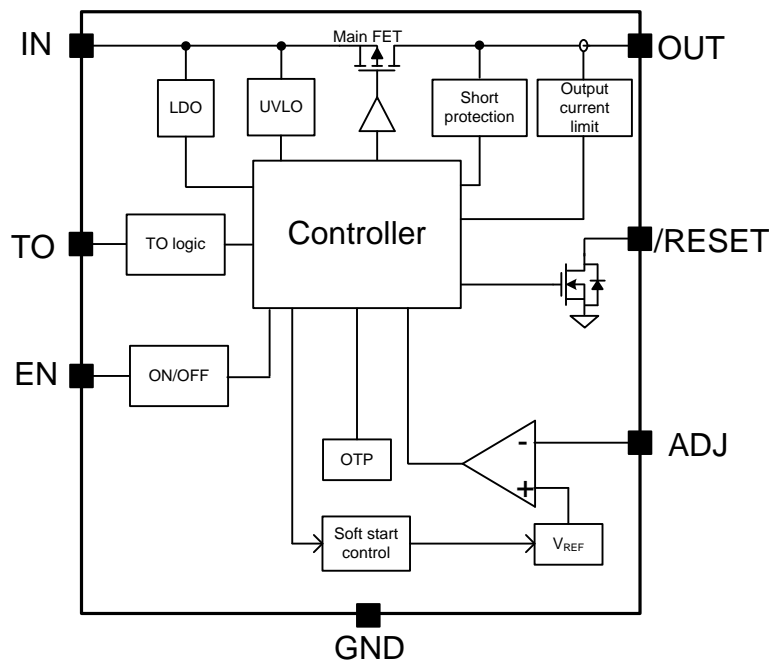


Figure 2. Block Diagram

Absolute Maximum Ratings

Parameter (Note1)	Min	Max	Unit
IN, EN, OUT, ADJ, /RESET	-0.3	40	V
TO	-0.3	3.6	
Lead Temperature (Soldering, 10 sec.)		260	°C
Junction Temperature, Operating	-40	150	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note2)	Typ	Unit
θ_{JA} Junction-to-ambient Thermal Resistance	38.3	°C/W
θ_{JC} Junction-to-case Thermal Resistance	12.6	
P_D Power Dissipation $T_A = 25^\circ\text{C}$	2.6	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
IN	4	36	V
EN, OUT, ADJ, /RESET	0	36	
TO	0	3.3	
Ambient Temperature	-40	125	°C



Electrical Characteristics

($V_{IN}=V_{EN}=12V$, $T_A=-40^{\circ}C\sim 125^{\circ}C$, unless otherwise specified, the values are guaranteed by test, design, or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typical	Max	Unit
Input Voltage	V_{IN}		4		36	V
Reference Voltage	V_{REF}	$T_A=-40^{\circ}C\sim 125^{\circ}C$	0.588	0.6	0.612	V
		$T_A=25^{\circ}C$	0.594	0.6	0.606	
ADJ pin Bias Current	I_{ADJ_Bias}	$V_{EN}=0V$, ADJ pin floating	-50		50	nA
Line Regulation	ΔV_{LNR}	$V_{IN}=4V$ to $36V$, $I_{OUT}=10mA$		1	1.5	mV/V
Load Regulation	ΔV_{LDR}	$V_{IN}=5V$, $I_{OUT}=10mA$ to $300mA$		0.25	0.5	%
Dropout Voltage	ΔV_{DROP}	$I_{OUT}=10mA$		10	20	mV
		$I_{OUT}=300mA$		300	540	mV
Quiescent Current	I_Q	$V_{IN}=(V_{OUT}+1V)$ to $36V$, $I_{OUT}=0mA$		7	14	μA
Shutdown Current	I_{SHDN}	$V_{EN}=0V$, $V_{IN}=24V$			5	μA
Current Limit	I_{limit}	$V_{OUT}=0.9*V_{OUT}(\text{normal})$	600	900	1200	mA
Output Short Protection Threshold	V_{ADJ_SHORT}	V_{FB} Falling	8	16	30	% V_{REF}
Output Short Off Time	t_{short_off}			16		ms
Power Supply Rejection	PSRR	Frequency=100Hz, $C_{OUT}=4.7\mu F$, $I_{OUT}=10mA$, $T_A=25^{\circ}C$		60		dB
		Frequency=100kHz, $C_{OUT}=4.7\mu F$, $I_{OUT}=10mA$, $T_A=25^{\circ}C$		35		
Input Voltage UVLO Threshold	V_{UVLO}	V_{IN} rising	2.9	3.3	4	V
UVLO Hysteresis	V_{UVLO_th}			200		mV
Enable Input Logic-High Voltage	$V_{EN,H}$		1.5			V
Enable Input Logic-Low Voltage	$V_{EN,L}$				0.4	V
Soft Start Time	t_{SS}			1		ms
Thermal Shutdown Temperature	T_{SD}			150		$^{\circ}C$
Thermal Shutdown Hysteresis	T_{HYS}			20		$^{\circ}C$
V_{TO} /RESET High-level Threshold	V_{TR}	V_{TO} rising	1.4	1.8	2.2	V
TO Default Rise Up time	$t_{To,Rise}$	OUT High, TO Floating, TO Rising from 0V to V_{TR}		1.6		μs
TO Charge Current	I_{TR}		8	16	24	μA
V_{OUT} /RESET Threshold	V_{OR}	V_{OUT} rising	85	90	95	% V_{OUT}
V_{OUT} /RESET Threshold Hysteresis	$V_{OR,HYS}$	V_{OUT} falling		5		% V_{OUT}
/RESET Output-Voltage Low					0.4	V

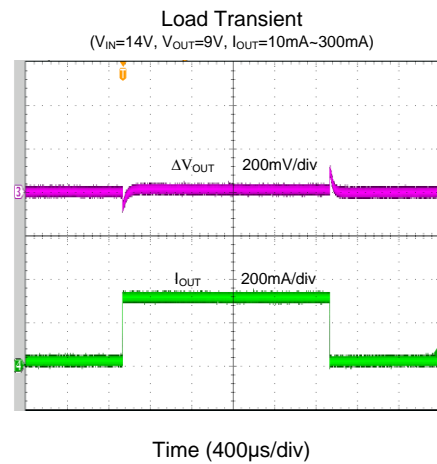
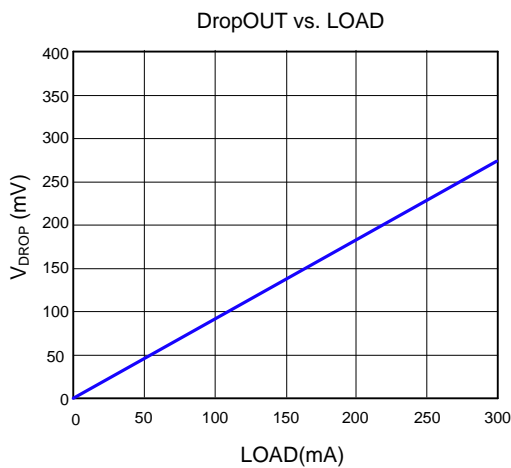
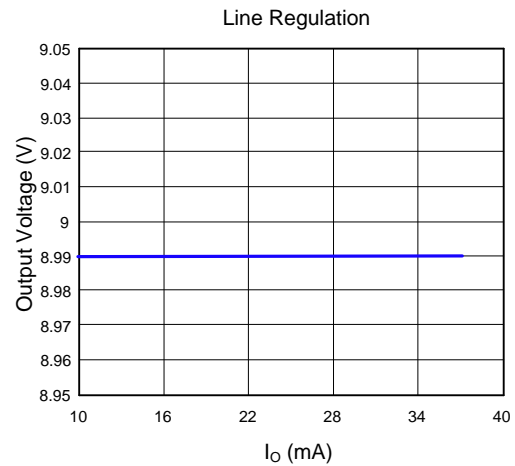
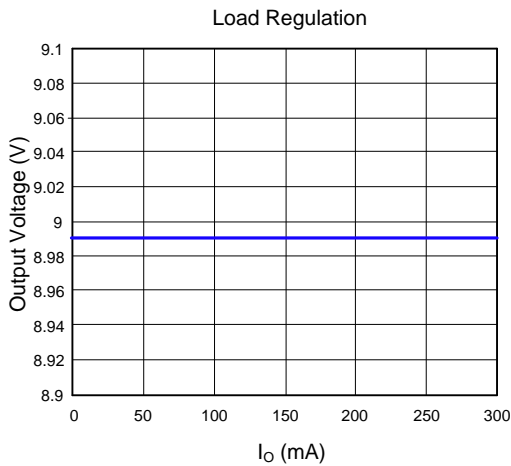
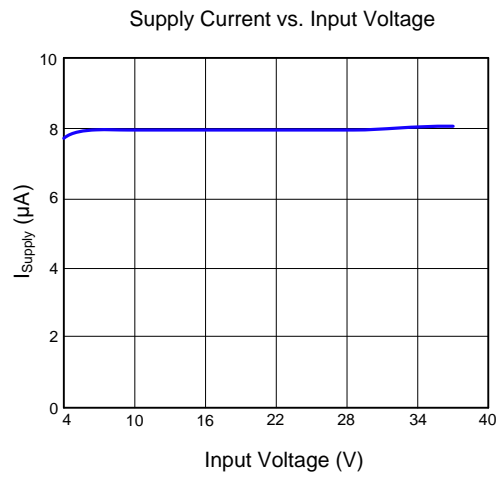
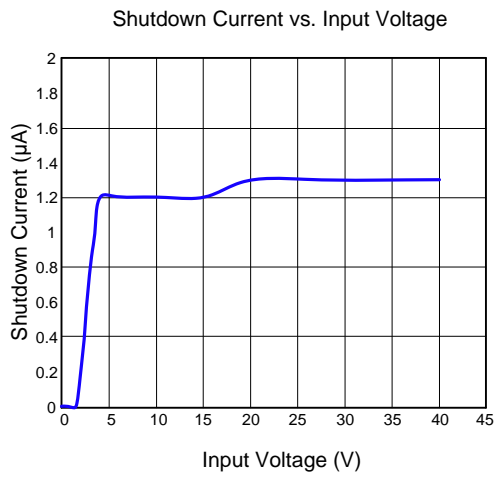


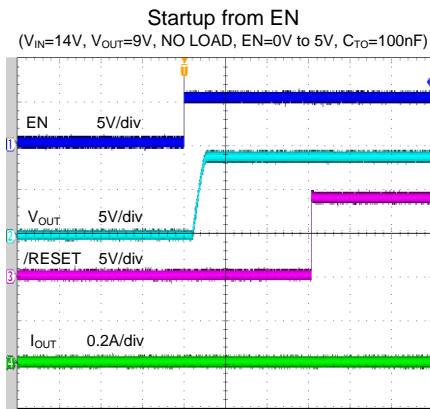
Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at $T_A = 25^\circ\text{C}$ on a low effective single-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

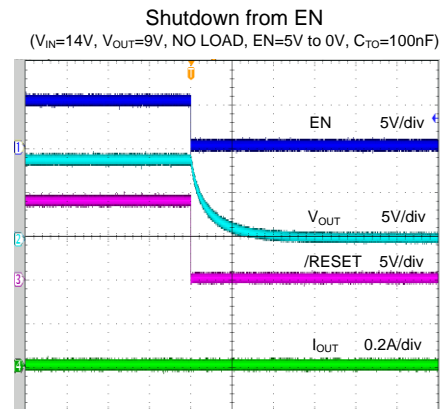
Note 3: The device is not guaranteed to function outside its operating conditions.

Typical Performance Characteristics

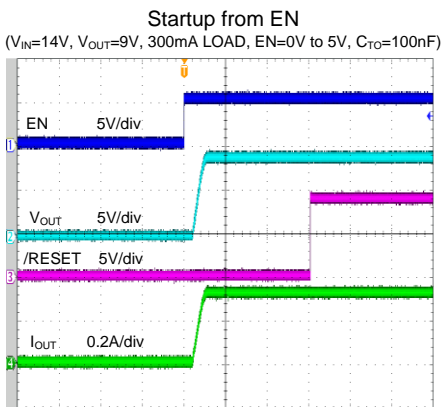




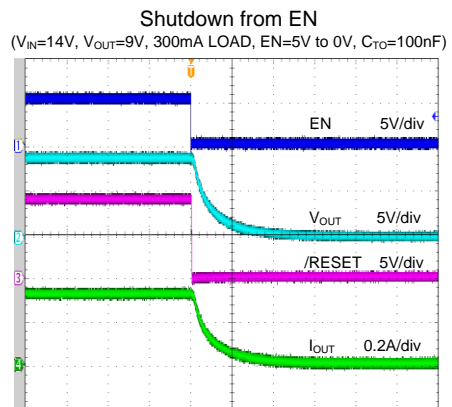
Time (4ms/div)



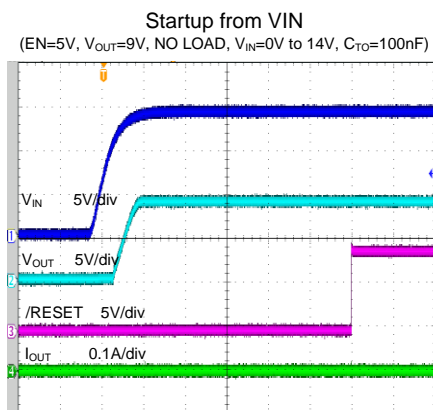
Time (2ms/div)



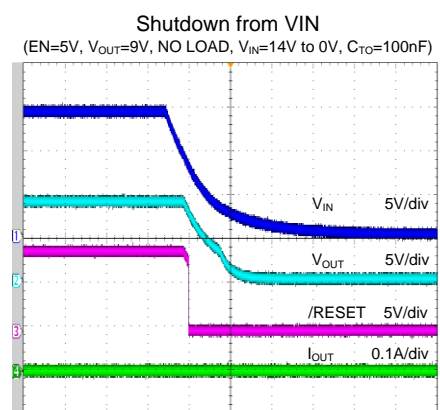
Time (4ms/div)



Time (100 μ s/div)

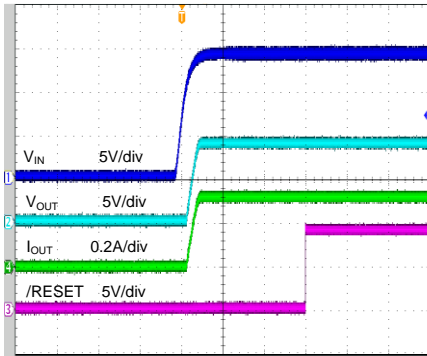


Time (2ms/div)



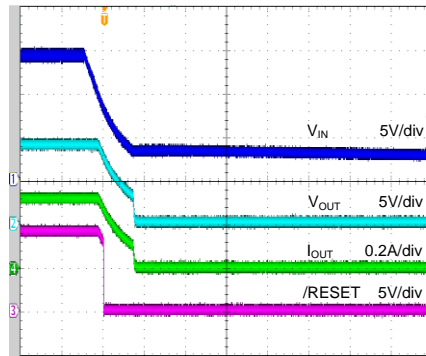
Time (100ms/div)

Startup from VIN
(EN=5V, V_{OUT}=9V, 300mA LOAD, V_{IN}=0V to 14V, C_{TO}=100nF)



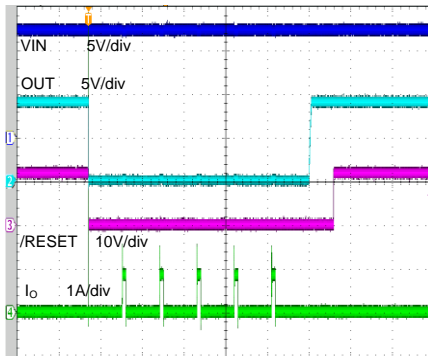
Time (4ms/div)

Shutdown from VIN
(EN=5V, V_{OUT}=9V, 300mA LOAD, V_{IN}=14V to 0V, C_{TO}=100nF)



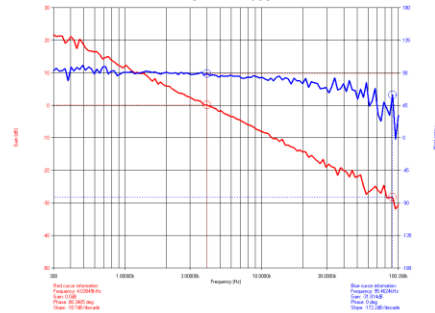
Time (4ms/div)

Short Protect
(VIN=12V, OUT=9V)

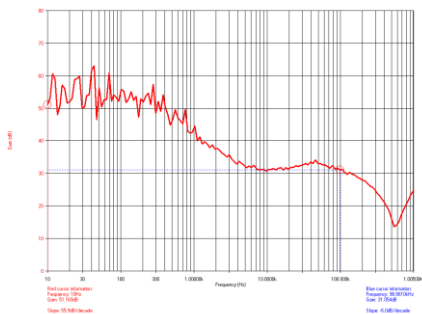


Time (20ms/div)

LOOP GAIN
(VIN=12V, OUT=9V, C_{OUT}=4.7uF, 300mA Load)
GAIN Phase



PSRR
(VIN=12V, OUT=9V, C_{OUT}=4.7uF, 300mA Load)



Application Information

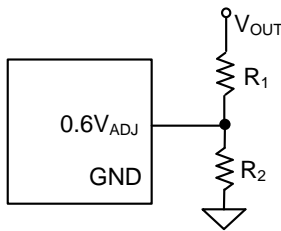
The SY2A27352 is a 300mA high-current capacity linear regulator with ultra-low ground current and low drop-out voltage. The device offers protection features, including an over-current limit, output short and over-temperature protections. The SY2A27352 has an adjustable output that can be configured using two external resistors.

Adjustable Output Voltage

Choose R_1 and R_2 to program the proper output voltage. To minimize power consumption under light loads, choosing large resistance values for both R_1 and R_2 is recommended. A value of between 10k Ω and 2M Ω is highly recommended for both resistors.

The output voltage can be selected using the following equation:

$$V_{OUT} = 0.6V \times (1 + R_1/R_2)$$



Over Temperature Protection (OTP)

The SY2A27352 includes over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will turn off the device when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C the IC will resume normal operation.

Output Short Circuit Protect

If V_{OUT} drops below 16% of the OUT set point, the short circuit protection mode will be initiated, and the device will be shut down for approximately 16ms. The device will then restart with a complete soft-start cycle. If the short circuit condition remains, another 'hiccup' cycle of shutdown and restart will continue indefinitely unless the OTP threshold is reached.

/RESET Function

The SY2A27352 includes an open-drain reset output. Once the output voltage exceeds the reset threshold voltage (90% of the OUT set point), the C_{TO} is charged with the current I_{TR} . /RESET will be in high-impedance state when the voltage on C_{TO} is larger than V_{TR} . If the output voltage is lower than the reset threshold voltage, the device discharges C_{TO} fast, and the /RESET pin is driven to low when the voltage on TO is lower than V_{TF} .

Timeout

The SY2A27352 features an adjustable reset timeout period. The internal capacitance produces a 1.6 μ s default delay when the TO pin is floating. Connect a capacitor from TO to the GND to set a higher timeout period than the default value. Use the following formula to determine the reset timeout capacitor:

$$C_{TO} = \frac{16\mu A \times T_{TIMEOUT}}{1.8V}$$

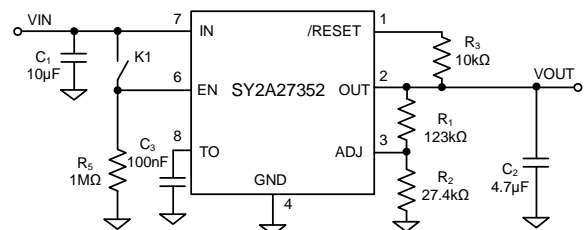
Input Capacitor C_{IN} and Output Capacitor C_{OUT}

To minimize the switching noise present in the system, improve power-supply rejection (PSRR) and transient response, place a typical X5R or high-grade ceramic capacitor close to the IN and GND pins. Care should be taken to minimize the loop area formed by the C_{IN} and the IN/GND pins. A 4.7 μ F ceramic capacitor with a voltage rating 20% higher than the maximum voltage is recommended for most applications.

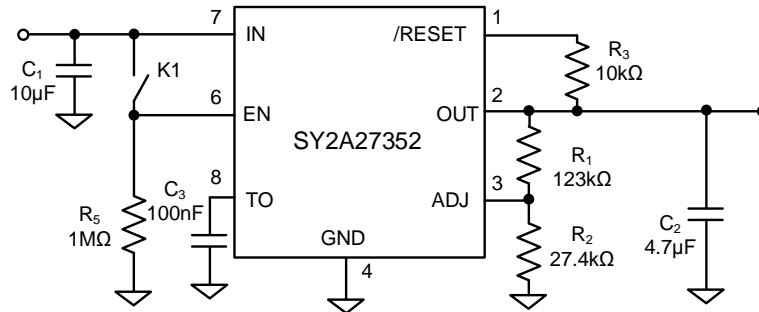
For stable operation over the full temperature range, a 4.7 μ F low-ESR ceramic capacitor is recommended for C_{OUT} . Using larger output-capacitor values such can help with reducing the noise, improve load-transient response and PSRR.

Example of the Typical Application (3.3V Output)

A typical application circuit with an output of 3.3V is shown below:



Application Schematic



BOM List

Designator	Description	Part Number	Manufacturer
C ₁	10µF/50V/1206	CL31A106KBHNNNE	SAMSUNG
C ₂	4.7µF/50V/1206	GRM31CR71H475KA12L	MuRata
C ₃	100nF/ 50V// 0603	GRM033R61E104KE14D	MuRata
C ₄	NULL		
R ₁	383kΩ/ 0603 (For 9V OUT)	RC0603FR-07383KL	YAGEO
	124kΩ/ 0603 (For 3.3V OUT)	RC0603FR-07124KL	YAGEO
R ₂	27.4kΩ/ 0603	RC0603FR-0727K4L	YAGEO
R ₃	10kΩ/ 0603	RC0603FR-0710KL	YAGEO
R ₅	100kΩ/ 0603	RC0603FR-07100KL	YAGEO

PCB Layout Guide

For best performance of the SY2A27352, the following guidelines must be followed:

1. Keep all power traces as short and wide as possible. A 2-layer- or 4-layer board is recommended for improved thermal performance and current flow capability. At least 6 vias are suggested around each power pin to distribute current to different PCB layers. These power pins include IN and OUT.
2. Place the input and output capacitors close to the LDO for better transient performance.
3. Maximize the copper area connected to the exposed pad to improve the heat transfer.

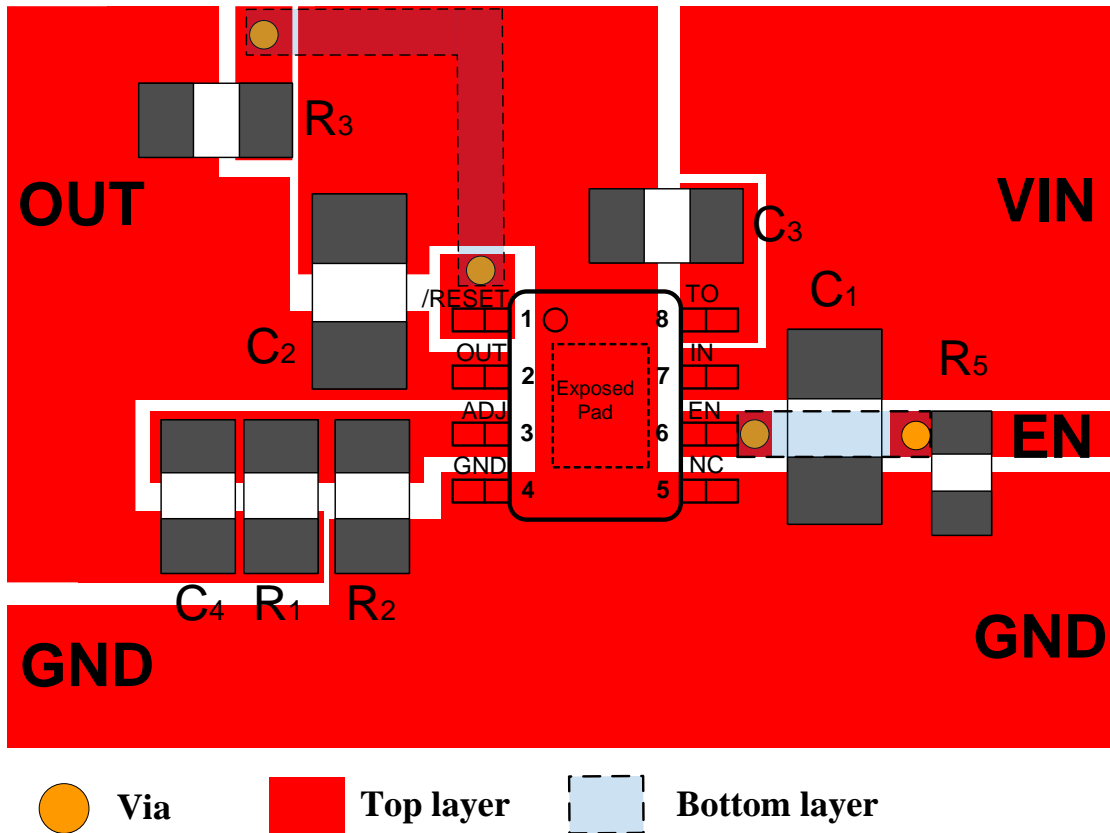
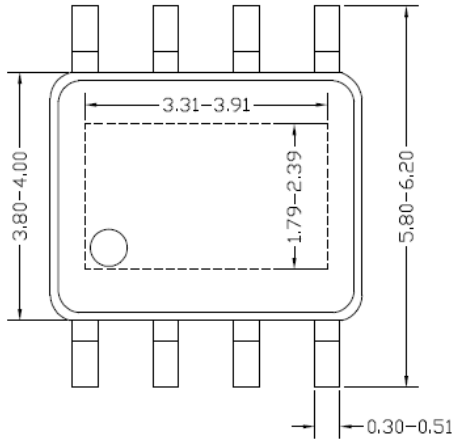
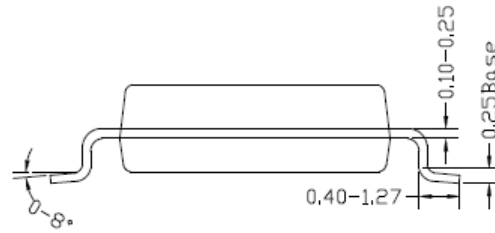


Figure 3. PCB Layout Suggestion

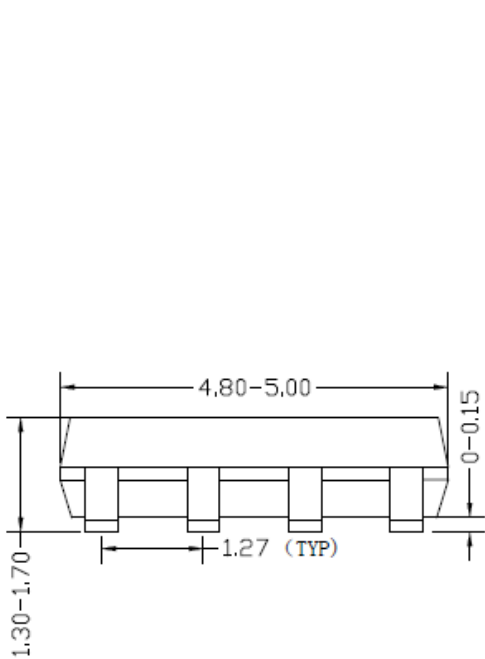
SO8E Package Outline & PCB Layout



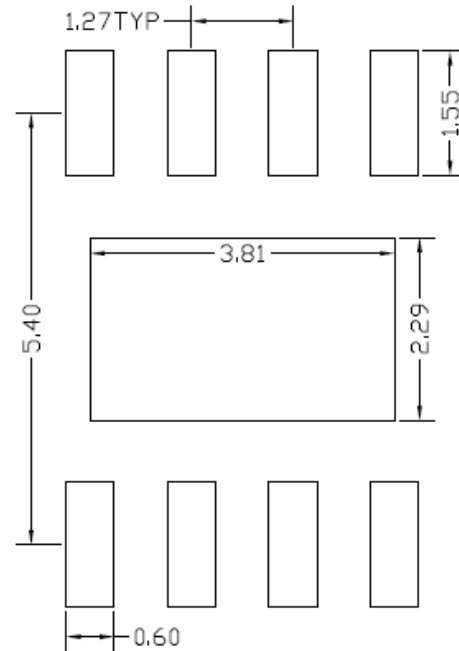
Top View



Side View



Front View

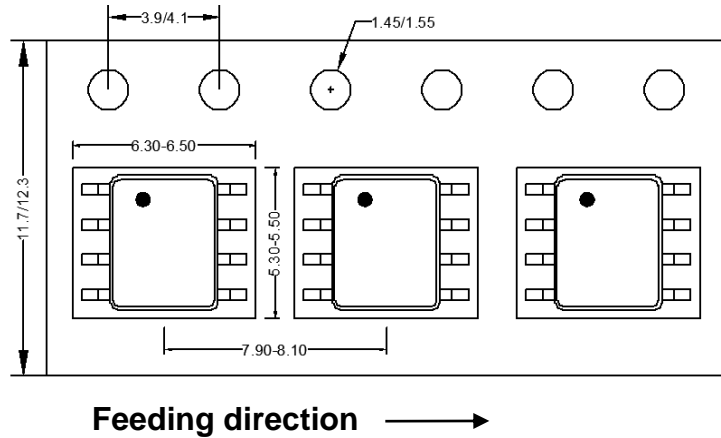


**Recommended PCB Layout
(Reference Only)**

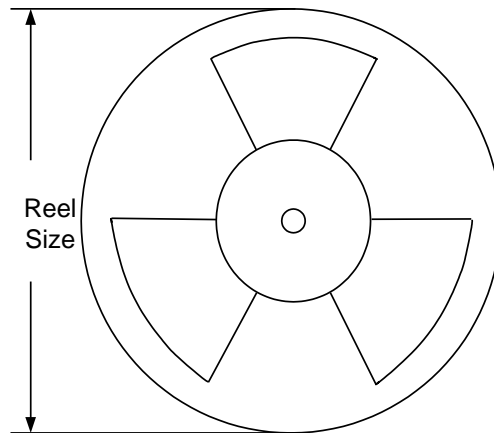
Note: All dimensions are in millimeters and exclude mold flash and metal burr.

Taping & Reel Specification

1. SO8E Taping Orientation



2. Carrier Tape & Reel Specification for Packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer * length(mm)	Leader * length (mm)	Qty per reel (pcs)
SO8E	12	8	13"	400	400	2500

3. Others: NA

Revision History

The revision history provided is for informational purposes only and is believed to be accurate; however, it is not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
Sep.25, 2023	Revision 1.0	Language improvements for clarity.
Apr.13, 2022	Revision 0.9C	Update the Input Voltage UVLO Threshold & Output Short Protection Threshold in EC table (page 4)
Sep.07, 2021	Revision 0.9B	1. Update the package outline drawing.
Jun.12, 2020	Revision 0.9A	1. Update the schematic diagram (page1); 2. Update the startup/shutdown waveforms (page7~8); 3. Update the PCB layout suggestion (page10).
Dec.27, 2019	Revision 0.9	Initial Release

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[AP7315-33W5-7](#) [LD56100DPU28R](#) [NCP154MX180300TAG](#) [AP2113AMTR-G1](#) [NJW4104U2-33A-TE1](#) [MP2013AGG-5-P](#)

[NCV8775CDT50RKG](#) [NJM2878F3-45-TE1](#) [S-19214B00A-V5T2U7](#) [S-19214B50A-V5T2U7](#) [S-19213B50A-V5T2U7](#) [S-19214BC0A-](#)

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