Applications Note: SY50131

Flyback Regulator
With Primary Side CV/CC Control For Adapters and Chargers

General Description

SY50131 is a single stage Flyback controller targeting at Constant Current/Constant Voltage (CC/CV) applications. It integrates a 600V MOSFET to decrease physical volume. Both the output current and voltage are sensed by primary side signal process. SY50131 operates quasi-resonant mode and adaptive PWM/PFM control for highest average efficiency. In addition, SY50131 has cable compensation to regulate the output voltage for better load regulation at cable terminal.

Ordering Information

SY50131□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY50131FAC	SO8	----

Features

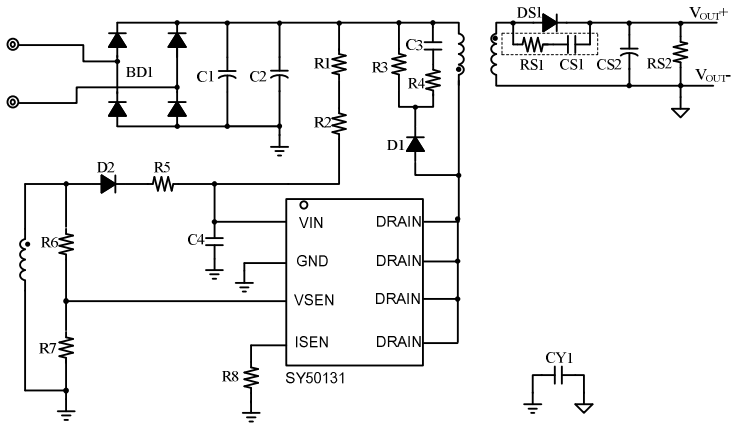
- Very tight PSR CC/CV regulation over entire operating range
- QR-mode operation for high efficiency
- PWM/PFM control for higher average efficiency
- Internal CC/CV loop compensation
- The self-adaption compensation for better stability
- Fast dynamic load transient response
- Cable compensation for better load regulation
- Low start up current: 4μA Max
- Reliable protections for OVP, SCP, OTP
- Reliable protections for safety requirement
- RoHS Compliant and Halogen Free
- Integrated 600V MOSFET
- Compact package: SO8

Applications

- AC/DC adapters
- Battery Chargers

Recommended operating output power		
Products	90~264Vac	176~264Vac
SY50131	5W	9W

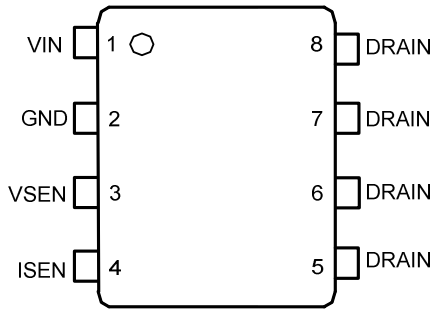
Typical Applications



Note：Ground node of current sample resistor must be connected to the ground of bus line capacitor

Figure 1. Schematic Diagram

Pinout (top view)



(SO8)

Top Mark: ATS*xyz* (device code: ATS, ***x=year code, y=week code, z= lot number code***)**

Pin	Name	Description
1	VIN	Power supply pin.
2	GND	Ground pin.
3	VSEN	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resistor divider and detects the inductor current zero crossing point.
4	ISEN	Current sense pin. Connect this pin to the source of the primary switch.
5	DRAIN	Drain of the internal power MOSFET.
6	DRAIN	Drain of the internal power MOSFET.
7	DRAIN	Drain of the internal power MOSFET.
8	DRAIN	Drain of the internal power MOSFET.

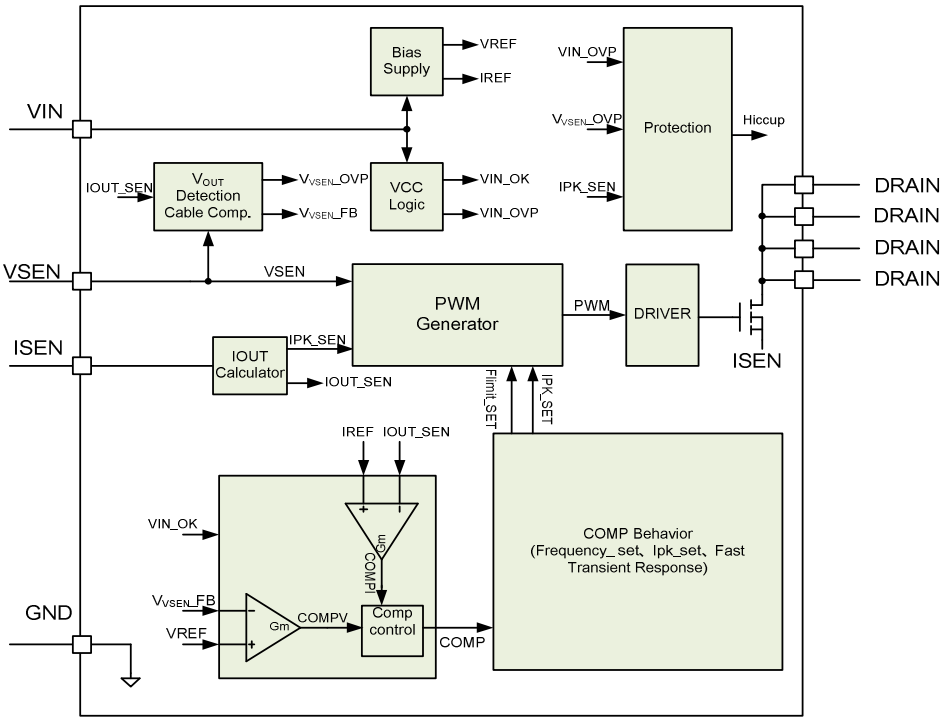
Absolute Maximum Ratings (Note 1)

VIN---------- 0.3V~21V
VSEN ---------- -0.3V~V_{VIN}+0.3V
ISEN---------- -0.3V~4V
Supply Current I_{VIN} ---------- 20mA
DRAIN---------- 600V
Power Dissipation, @ T_A = 25°C SO8 ---------- 1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA} ---------- 125°C/W
SO8, θ_{JC} ---------- 60°C/W
Junction Temperature Range ---------- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

VIN------- ---------- 9V~17.5V
ISEN---------- 0V~1V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 105°C

Block Diagram



Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
Input voltage range	V_{VIN}		9		17.5	V
VINturn-on threshold	$V_{VIN,ON}$			14.7		V
VINturn-off threshold	$V_{VIN,OFF}$			7		V
VIN OVP voltage	$V_{VIN,OVP}$			17.5		V
Start up Current	I_{ST}	$V_{VIN}<V_{VIN,OFF}$			4	µA
Operating Current	I_{VIN}	C_L=100pF,f=100kHz		1		mA
Quiescent Current	IQ	CL=0, f=2kHz		200		µA
Shunt current in OVP mode	$I_{VIN,OVP}$	$V_{VIN}>V_{VIN,OVP}$		7.5		mA
Current feedback modulator Section						
Internal reference voltage	V_{REF}		-1.5%	0.42	+1.5%	V
ISEN pin Section						
Current limit Voltage	VISEN,LIM	VFBV<0.4V		0.5		V
		VFBV>0.4V	-5%	1	+5%	V
Latch Voltage for ISEN	VISEN,EX			2		V
VSEN pin Section						
OVP voltage threshold	$V_{VSEN,OVP}$		-5%	1.45	+5%	V
Internal reference voltage	$V_{VSEN,REF}$		-1.5%	1.25	+1.5%	V
Cable Compensation coefficient	K_3			17.5		µA/V
Integrated MOSFET Section						
Breakdown Voltage	V_{BV}	V_{GS}=0V,I_{DS}=250µA	600			V
Gate Driver Section						
Gate driver voltage	V_{Gate}			12		V
Max ON Time	$t_{ON,MAX}$			24		µs
Min ON Time	$t_{ON,MIN}$				300	ns
Max OFF Time	$t_{OFF,MAX}$			500		µs
Maximum switching frequency	f_{MAX}			125		kHz
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on "2 x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

Operation

SY50131 is a high performance Flyback controller with primary side control and constant current and constant voltage regulation.

It integrates a 600V MOSFET to decrease physical volume.

The Device provides primary side control to eliminate the opto-isolators or the secondary feedback circuits, which would cut down the cost of the system.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the integrated MOSFET at voltage valley; the start up current of the device is rather small (4μA typically) to reduce the standby power loss further.

In order to improve the stability, the self-adaption compensation is applied.

The device provides reliable protections such as Over Voltage Protection (OVP), Short Circuit Protection (SCP), Over Temperature Protection (OTP), Output voltage OVP protection , VSEN pin short protection ,etc.

SY50131 can be applied in AC/DC adapters, Battery Chargers and other consumer electronics.

SY50131 is available with SO8 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to $V_{VIN,ON}$, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of Flyback transformer could supply enough energy to maintain V_{VIN} above $V_{VIN,OFF}$.

The whole start up procedure is divided into two sections shown in Fig.2. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

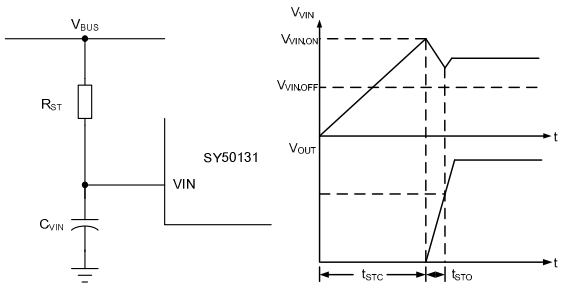


Fig.2 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below $V_{VIN\text{-}OFF}$, the IC will stop working.

Quasi-Resonant Operation(valley detection)

QR mode operation provides low turn-on switching losses for Flyback converter.

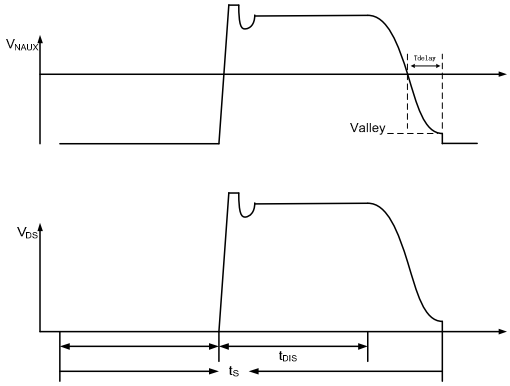


Fig.3 QR mode operation

The voltage across drain and source of the primary integrated MOSFET is reflected by the auxiliary winding of the Flyback transformer. VSEN pin detects the voltage across the auxiliary winding by a resistor divider.When the voltage on VSEN pin across zero, the MOSFET would be turned on after 400ns delay.

Output Voltage Control(CV control)

In order to achieve primary side constant voltage control, the output voltage is detected by the auxiliary winding voltage.

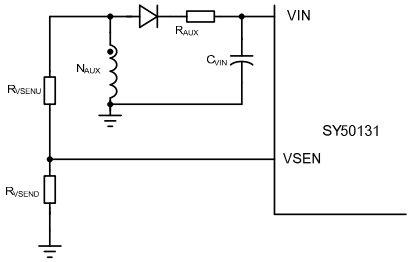


Fig.4 VSEN pin connection

As shown in Fig.5, during OFF time, the voltage across the auxiliary winding is

$$V_{AUX} = (V_{OUT} + V_{D,F}) \times \frac{N_{AUX}}{N_S} \quad (3)$$

N_{AUX} is the turns of auxiliary winding; N_S is the turns of secondary winding; $V_{D,F}$ is the forward voltage of the power diode.

At the current zero-crossing point, $V_{D,F}$ is nearly zero, so V_{OUT} is proportional with V_{AUX} exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by

$$\frac{V_{VSEN,REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \times \frac{N_{AUX}}{N_S} \quad (4)$$

Where $V_{VSEN,REF}$ is the internal voltage reference.

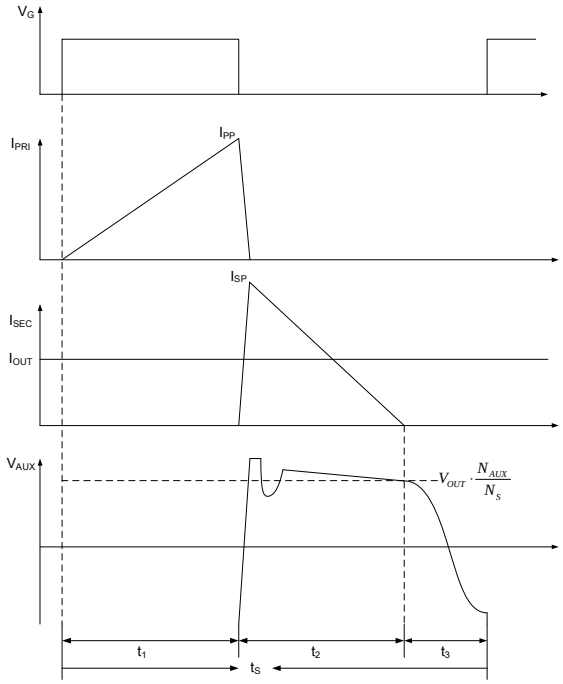


Fig.5 Auxiliary winding voltage waveforms

Output Current Control (CC control)

The output current is regulated by SY50131 with primary side detection technology, the maximum output current $I_{OUT,LIM}$ can be set by

$$I_{OUT,LIM} = \frac{k_1 \times V_{REF} \times N_{PS}}{R_S} \quad (5)$$

Where k_1 is the output current weight coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, $I_{OUT,LIM}$ can be programmed by N_{PS} and R_S.

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}} \quad (6)$$

K_1 is set to 0.5

When over current operation or short circuit operation happens, the output current will be limited at $I_{OUT,LIM}$. The V-I curve is shown as Fig.6.

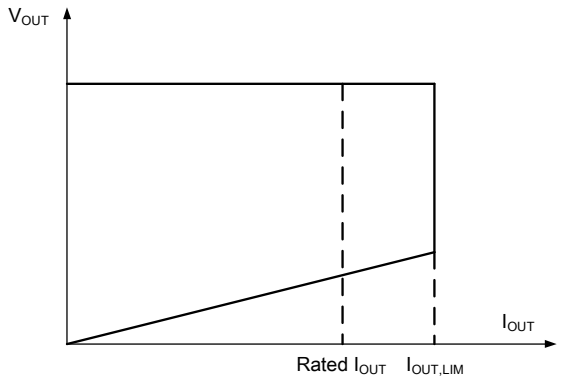


Fig.6 V-I curve

The IC provides line regulation modification function to improve line regulation performance of the output current.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISEN-C} is added to ISEN pin during ON time to improve such performance. This ΔV_{ISEN-C} is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISEN,C} = V_{BUS} \times \frac{N_{AUX}}{N_P} \times \frac{1}{R_{VSENU}} \times k_2 \quad (7)$$

Where R_{VSENU} is the upper resistor of the divider; k_2 is an internal constant as the modification coefficient.

The compensation is mainly related with R_{VSENU}, larger compensation is achieved with smaller R_{VSENU}. Normally, R_{VSENU} ranges from 50kΩ~150KΩ.

Cable Compensation

SY50131 has cable compensation to regulate the output voltage for better load regulation at cable terminal. When the converter output load increases from no load to full load, the voltage drops on the output cable are compensated by decreasing the voltage feedback signals, which is shown by Fig. 7.

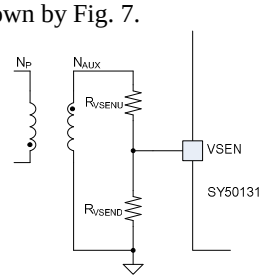


Fig. 7 Cable Compensation

$$R_{VSENU} = \frac{R_{Cable}}{2k_3 \cdot R_S} \cdot \frac{N_P}{N_S} \cdot \frac{N_{AUX}}{N_S} \quad (8)$$

k_3 is set to17.5uA/V.

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R_{cable} is the resistance on the cable. The cable compensation effect can be adjusted by change the resistance of R_{VSENU} to achieve good load regulation of different output cables. The larger R_{VSENU}, the stronger cable compensation effect will be achieved.

If the output current is below 10% the OCP point, there is no cable compensation.

Short Circuit Protection (SCP)

There are two kinds of situations, one is the valley signal cannot be detected by VSEN, the other is the valley signal can be detected by VSEN.

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so valley signal cannot be detected by VSEN. There are two cases , the one is without valley detection, MOSFET cannot be turned on until maximum off time is reached. If MOSFET is turned on with maximum off-time for 64 times continuously which can not detected valley, IC will be shut down and enter into hiccup mode. The other is that IC will be shut down and enter into hiccup mode when V_{VIN} below $V_{VIN,OFF}$ within 64 times .

When the output voltage is not low enough to disable valley detection in short condition, SY50131 will operate in CC mode until VIN is below $V_{IN,OFF}$.

In order to guarantee SCP function not effected by voltage spike of auxiliary winding, a filter resistor R_{AUX} is needed.

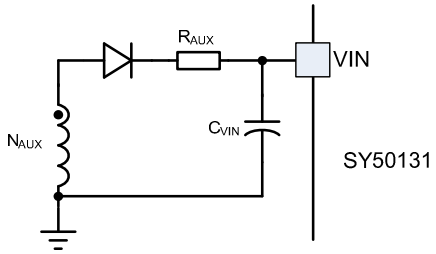


Fig. 8 Filter resistor R_{AUX}

Output voltage OVP protection

The secondary maximum voltage is limited by the SY50131.When the VSEN pin signal exceeds 1.45V, SY50131 will stop switching and discharge the VIN voltage. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged again by HV start up.

VSEN pin short protection

The SY50131 has a protection against faults caused by a shorted VSEN pin or a shorted pull-down resistor. During start-up, the voltage on the VSEN pin is monitored. In normal situations, the voltage on the VSEN pin reaches the sense protection trigger level. When the VSEN voltage does not reach this level, the VSEN pin is shorted and the protection is activated. The IC stops switching and discharge the VIN voltage. Once V_{VIN} is below $V_{VIN,OFF}$, the IC will shut down and be charged again by HV start up.

Power design

A few applications are shown as below.

Products	Input range	Output		Temperature rise
SY50131	90Vac~264Vac	5W	5V/1A	40℃
	90Vac~264Vac	6.5W	5V/1.3A	50℃
	90Vac~264Vac	7.0W	5V/1.4A	60℃

The test is operated in natural cooling condition at 25 ℃ ambient temperature .

Power Device Design

DIODE

When the operation condition is with maximum input voltage and full load, the voltage stress of secondary power diode is maximized;

$$V_{D\_R\_MAX}=\frac{\sqrt{2}V_{AC\_MAX}}{N_{PS}}+V_{OUT}\ (9)$$

Where $V_{AC,MAX}$ is maximum input AC RMS voltage; N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the rated output voltage.

When the operation condition is with minimum input voltage and full load, the current stress of power diode is maximized.

$$I_{D\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX}\ (10)$$

$$I_{D\_AVG}=I_{OUT}\ (11)$$

Where $I_{P\text{-}PK\text{-}MAX}$ is maximum primary peak current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the internal power MOSFET:

$$N_{PS}\le\frac{V_{MOS\_(BR)DS}\times 90\%-\sqrt{2}V_{AC\_MAX}-\Delta V_S}{V_{OUT}+V_{D\_F}}\ (12)$$

Where $V_{MOS,(BR)DS}$ is the breakdown voltage of the integrated MOSFET. $V_{D\text{-}F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.9.

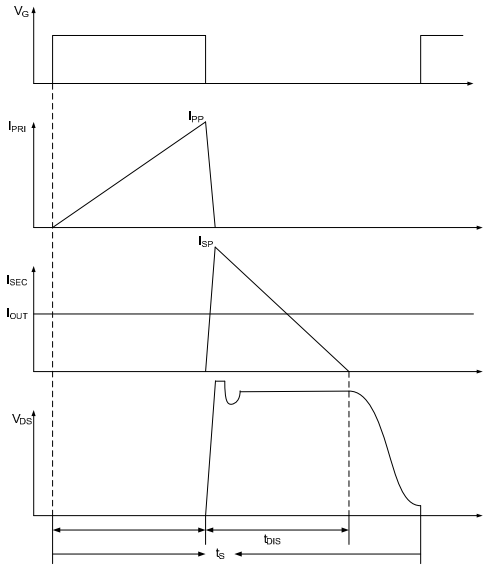


Fig.9 switching waveforms

When the operation condition is with minimum input AC RMS voltage and full load, the switching frequency is minimum frequency, the maximum peak current through integrated MOSFET and the transformer happens.

Once the minimum frequency $f_{S\text{-}MIN}$ is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D\_F}} \quad (13)$$

(b) Preset minimum frequency $f_{S\text{-}MIN}$

(c) Compute inductor L_M and maximum primary peak current $I_{P,PK,MAX}$

$$I_{P,PK,MAX} = \frac{2P_{OUT}}{\eta \times V_{DC,MIN}} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D,F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S,MIN}} \quad (14)$$

$$L_m = \frac{2P_{OUT}}{\eta \times I_{P,PK,MAX}^2 \times f_{S,MIN}} \quad (15)$$

Where C_{Drain} is the parasitic capacitance at drain of integrated MOSFET; η is the efficiency; P_{OUT} is rated full load power

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P,PK,MAX}}{V_{BUS}} \quad (16)$$

$$t_2 = \frac{L_m \times I_{P,PK,MAX}}{N_{PS} \times (V_{OUT} + V_{D,F})} \quad (17)$$

$$t_S = \frac{1}{f_{S,MIN}} \quad (18)$$

(e) Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P,RMS,MAX} = \frac{\sqrt{3}}{3} I_{P,PK,MAX} \times \sqrt{\frac{t_1}{t_S}} \quad (19)$$

(f) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (20)$$

$$I_{S,RMS,MAX} = \frac{\sqrt{3}}{3} N_{PS} \cdot I_{P,PK,MAX} \cdot \sqrt{\frac{t_2}{t_S}} \quad (21)$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. the parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P = \frac{L_M \times I_{P\_PK\_MAX}}{\Delta B \times A_e} \quad (22)$$

(d) Compute secondary turn N_S

$$N_S = \frac{N_P}{N_{PS}} \quad (23)$$

(e) compute auxiliary turn N_{AUX}

$$N_{AUX} = N_S \times \frac{V_{VIN}}{V_{OUT}} \quad (24)$$

Where V_{VIN} is the working voltage of VIN pin (11V~15V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Input capacitor C_{BUS}

Generally, the input capacitor C_{BUS} is selected by

$C_{BUS} = 2 \sim 3\mu F / W$

Or more accurately by

$$C_{BUS}=\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC,MIN}})+\frac{\pi}{2}}{\pi}\times\frac{P_{OUT}}{\eta}\times\frac{1}{2f_{IN}V_{AC,MIN}^{2}[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC,MIN}})^{2}]} \quad (25)$$

Where ΔV_{BUS} is the voltage ripple of BUS line.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{\Delta V_S}\times\frac{L_K}{L_M}\times P_{OUT} \quad (26)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD}=\frac{(N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S)^2}{P_{RCD}} \quad (27)$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

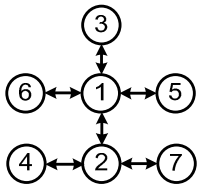
$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD}f_S\Delta V_{C\_RCD}} \quad (28)$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) The connection of primary ground is recommended as:

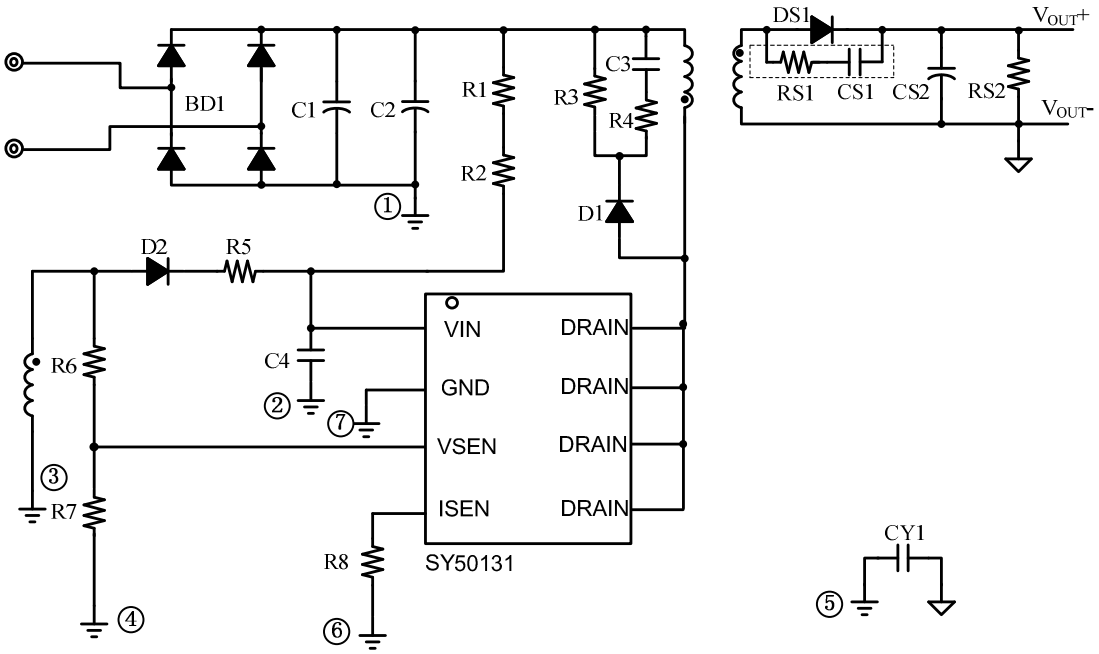


Ground ①: ground of BUS line capacitor
Ground ②: ground of bias supply capacitor
Ground ③: ground node of auxiliary winding
Ground ④: ground node of divider resistor
Ground ⑤: primary ground node of Y capacitor
Ground ⑥: ground node of current sample resistor.
Ground ⑦: ground of IC GND.

(d) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(e) Loop of 'Source pin – current sample resistor – GND pin' should be kept as small as possible.

(f) The resistor divider connected to VSEN pin is recommended to be put beside the IC.



Note：Ground node of current sample resistor must be connected to the ground of bus line capacitor

Design Notice

1. At no load, secondary side diode freewheeling time should be more than 1.8us.
2. VIN voltage prefer to larger than 11V for all conditions.
3. Some transformers structure may induce larger spike or larger ring on the current sample resistor at the initial of the primary switch turning on.This spike or ring may cause wrongly detection of the peak current and make the switch turn off earlier, so the accuracy feedback voltage sample cannot be guaranteed. The recommend structures are:0.5 Primary.----Shielding----Second.----Auxiliary.----0.5Primary.or Primary.----Shielding----Second.----Auxiliary; Do not use the structure like 0.5Primary.----Auxiliary----Second.----Shielding.----0.5Primary.
4. RCD snubber's influence:
   At no load and light load, capacitor's voltage may be discharged to a small value, when primary switch turn off , peak current needs to charge the snubber capacitor, this will affect the feedback voltage sample and induce larger ripple or other issues. The recommend parameters is: When Imin(Imin=0.15V/Rs)is 0.1A,the snubber capacitor should not be larger than 330pF.
5. At heavy load, the peak-to-peak voltage at the Vsen pin should be less than approximately 100mVp-p after off-min time(1.8us).This can be guaranteed by decreasing the leakage inductance and using proper RCD snubber.
6. R_{VSENU} is the upper resistor of the divider .Normally, its value should be in 50kΩ~150kΩ.
7. Because AP51 built in CC/CV loop , in order to ensure the stability, output capacitor should be in a range, that is Cout*(Vo/Io) should not be far away from 3.7m.For example, 5V2Aoutput case, Cout=3.7/2.5=1480uF, the output capacitor should be in the range of 1270uF to 1680uF. In other hand, switching frequency ripple should also be considerd. If switching frequency ripple is large, increase the capactiance properly or use low ESR capacitor.

Design Example

A design example of typical application is shown below step by step.(Cable Test)

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	5V
I_{OUT}	1A	η	80%

#2. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
$V_{AC,MIN}$	90V	V_{AC-MAX}	264V
ΔV_S	70V	$V_{MOS-(BR)DS}$	600V
P_{OUT}（Max）	5W	$V_{D,F}$	1.0V
C_{Drain}	100pF	f_{S-MIN}	65kHz
ΔV_{BUS}	30% V_{BUS}		

(a) Compute turns ratio N_{PS} first

$$N_{PS} \le \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2} V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$

$$= \frac{600V \times 0.9 - \sqrt{2} \times 264V - 70V}{5V + 1.0V}$$

$$= 16.108$$

N_{PS} is set to

N_{PS}=16

(b)$f_{S,MIN}$ is preset

f_{S_MIN}=65kHz

(c) Compute inductor L_M and maximum primary peak current $I_{P,PK,MAX}$

$$I_{P,PK,MAX} = \frac{2P_{OUT}}{\eta \times \left(\sqrt{2} V_{AC,MIN} - \Delta V_{BUS}\right)} + \frac{2P_{OUT}}{\eta \times N_{PS} \times (V_{OUT} + V_{D,F})} + \pi \sqrt{\frac{2P_{OUT}}{\eta} \times C_{Drain} \times f_{S,MIN}}$$

$$= \frac{2 \times 5W}{0.80 \times (\sqrt{2} \times 90V - 0.3 \times \sqrt{2} \times 90V)} + \frac{2 \times 5W}{0.80 \times 16 \times (5V + 1V)} + \pi \times \sqrt{\frac{2 \times 5W}{0.80} \times 100pF \times 65KHz}$$

$$= 0.299A$$

$$L_m = \frac{2P_{OUT}}{\eta \times I_{P,PK,MAX}^2 \times f_{S,MIN}}$$
$$= \frac{2 \times 5W}{0.80 \times (0.299A)^2 \times 65kHz}$$
$$= 2.15mH$$

Set: L_m=2.3mH

(d) Compute current rising time t_1 and current falling time t_2

$$t_1 = \frac{L_M \times I_{P,PK,MAX}}{V_{BUS}} = \frac{2.3mH \times 0.299A}{\sqrt{2} \times 90V} = 5.40\mu s$$

$$t_2 = \frac{L_m \times I_{P,PK,MAX}}{N_{PS} \times (V_{OUT} + V_{D,F})} = \frac{2.3mH \times 0.299A}{16 \times (5V + 1V)} = 7.16\mu s$$

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}} = \pi \times \sqrt{2.3mH \times 100pF} = 1.51\mu s$$

$$t_S = t_1 + t_2 + t_3 = 5.00\mu s + 6.24\mu s + 0.99\mu s = 14.07\mu s$$

(e) Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P,RMS,MAX} = \frac{\sqrt{3}}{3} I_{P,PK,MAX} \times \sqrt{\frac{t_1}{t_S}} = \frac{\sqrt{3}}{3} \times 0.299A \times \sqrt{\frac{5.40\mu s}{14.07\mu s}} = 0.107A$$

(f) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 16 \times 0.299A = 4.781A$$

$$I_{S,RMS,MAX} = N_{PS} \times \frac{\sqrt{3}}{3} I_{P,PK,MAX} \times \sqrt{\frac{t_2}{t_S}} = 16 \times \frac{\sqrt{3}}{3} \times 0.299A \times \sqrt{\frac{7.16\mu s}{14.07\mu s}} = 1.97A$$

#3. Select secondary power diode

Refer to Power Device Design

Compute the voltage and the current stress of secondary power diode

$$V_{D\_R\_MAX} = \frac{\sqrt{2} V_{AC\_MAX}}{N_{PS}} + V_{OUT} = \frac{\sqrt{2} \times 264V}{16} + 5V = 28.34V$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 16 \times 0.299A = 4.78A$$

$$I_{D\_AVG} = 1.0A$$

#4. Select the input capacitor C_{IN}

Refer to input capacitor C_{IN} Design

Known conditions at this step			
$V_{AC,MIN}$	90V	ΔV_{BUS}	30% $V_{AC,MIN}$

$$C_{BUS}=\frac{\arcsin(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC,MIN}})+\frac{\pi}{2}}{\pi}\times\frac{P_{OUT}}{\eta}\times\frac{1}{2f_{IN}V_{AC,MIN}^2[1-(1-\frac{\Delta V_{BUS}}{\sqrt{2}V_{AC,MIN}})^2]}$$

$$=\frac{\arcsin(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})+\frac{\pi}{2}}{\pi}\times\frac{5W}{0.80}\times\frac{1}{2\times 50\times 90V^2\times[1-(1-\frac{0.3\times\sqrt{2}\times 90V}{\sqrt{2}\times 90V})^2]}$$

$=11.13\mu F$

Set: $C_{BUS}=11.5\,\mu F$

Where ΔV_{BUS} is the voltage ripple of BUS line.

#5. Set VIN pin

Refer to Start up

Conditions			
$V_{BUS-MIN}$	$90V\times\sqrt{2}$	$V_{BUS-MAX}$	$264V\times\sqrt{2}$
I_{ST}	4μA (Max)	V_{IN-ON}	14.7V (typical)
$I_{VIN-OVP}$	7.5mA (typical)	t_{ST}	2s (designed by user)

(a) R_{ST} is preset

$$R_{ST}<\frac{V_{BUS}}{I_{ST}}=\frac{90V\times\sqrt{2}}{4\mu A}=31.81M\Omega\text{ ,}$$

$$R_{ST}>\frac{V_{BUS}}{I_{VIN\_OVP}}=\frac{264V\times 1.414}{7.5mA}=49.77k\Omega$$

Set R_{ST}

$R_{ST}=6M$

(b) Design C_{VIN}

$$C_{VIN}=\frac{(\frac{V_{BUS}}{R_{ST}}-I_{ST})\times t_{ST}}{V_{VIN\_ON}}=\frac{(\frac{90V\times 1.414}{6M\Omega}-4\mu A)\times 2s}{14.7V}=2.34\mu F$$

Set C_{VIN}

$C_{VIN}=3.3\mu F$

#6. Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
k_1	0.5	N_{PS}	16
V_{REF}	0.45V	$I_{OUT,LIM}$	1.2A

The current sense resistor is

$$R_S = \frac{k_1 \times V_{REF} \times N_{PS}}{I_{OUT}} = \frac{0.5 \times 0.42V \times 16}{2.4A} = 2.8\Omega$$

Set R_S

$R_S = 2.4\Omega$

#7. Set VSEN pin

Refer to V_{OUT}

First compute R_{VSENU}

Conditions			
V_{OUT}	5V	V_{VSEN_REF}	1.25V
R_{Cable}	0.31Ω	N_S	10
N_{AUX}	24	K_3	17.5u

$$R_{VSENU} = \frac{N_P}{N_S} \cdot R_{Cable} \cdot \frac{N_{AUX}}{N_S} \cdot \frac{1}{2K_3 \cdot R_S} = 118K\Omega$$

Set R_{VSENU}

$R_{VSENU} = 100K\Omega$

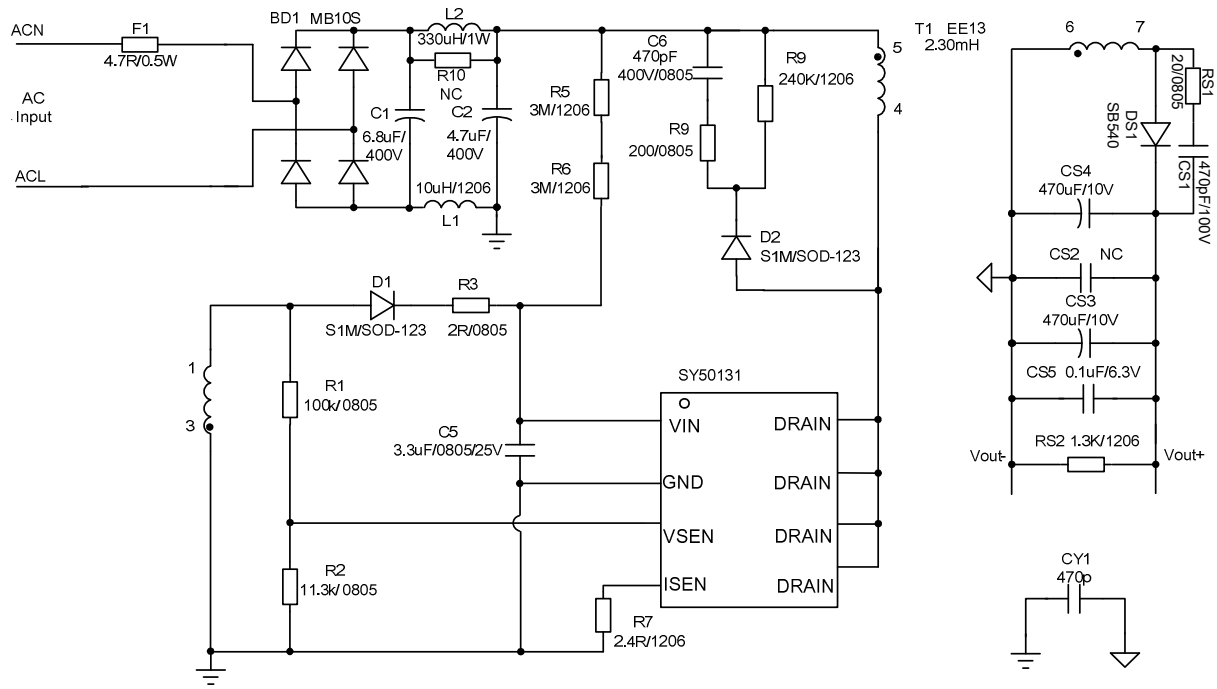
Then compute R_{VSEND}

$$R_{VSEND} = \frac{R_{VSENU}}{\frac{V_{OUT} N_{AUL}}{V_{VSEN,REF} N_S} - 1} = \frac{100K}{(\frac{5V \times 20}{1.25V \times 10} - 1)} = 11.6K$$

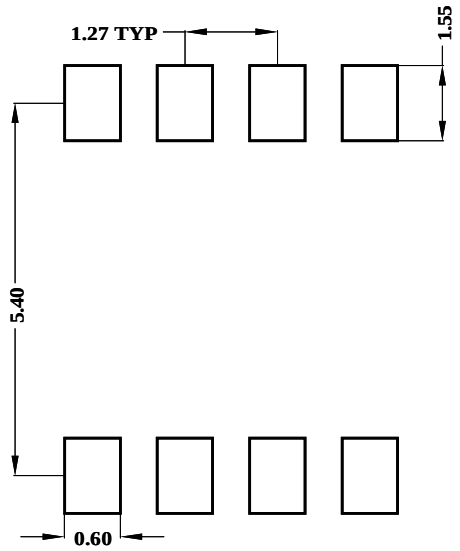
Set R_{VSEND}

$R_{VSEND} = 11.3k\Omega$

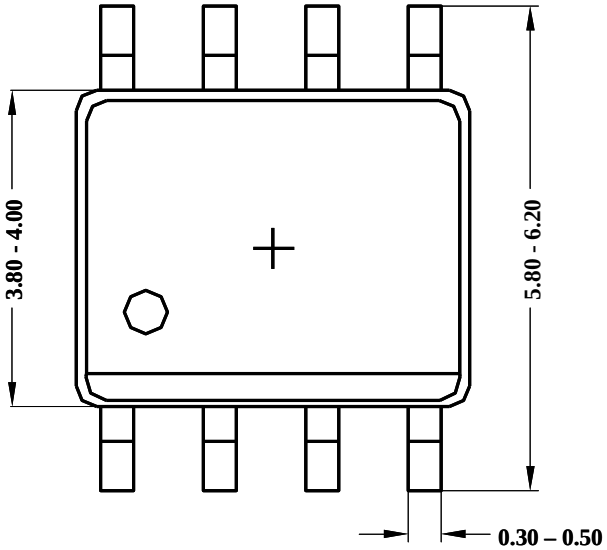
#8. Final result

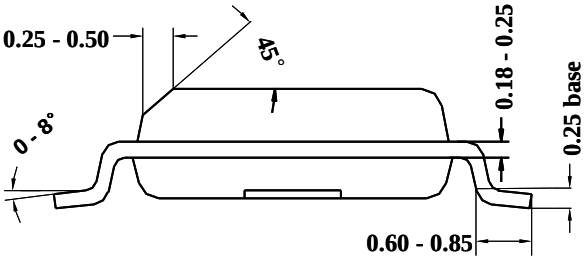


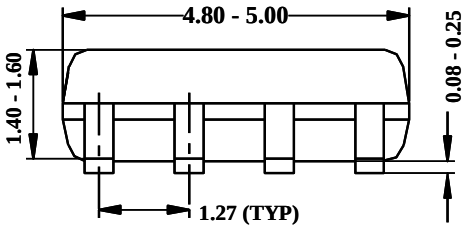
SO8 Package Outline & PCB Layout Design



Recommended Pad Layout







Notes: All dimensions are in millimeters.
All dimensions don't include mold flash & metal burr.

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