Applications Note: SY50283

Buck Regulator
With CV/CC Control

General Description

SY50283 is a Buck regulator targeting at constant current/constant voltage (CC/CV) applications. It integrates a 500V/7Ω MOSFET in a compact SO8 package to minimize the size.

SY50283 adopts the quasi-resonant operation and burst mode control to achieve the highest average efficiency and the best EMI performance. The no-load switching frequency can be as low as 2 kHz, minimizing the no-load power loss

SY50283 provides reliable protections such as short circuit protection (SCP), over voltage protection (OVP), over temperature protection (OTP), etc.

Features

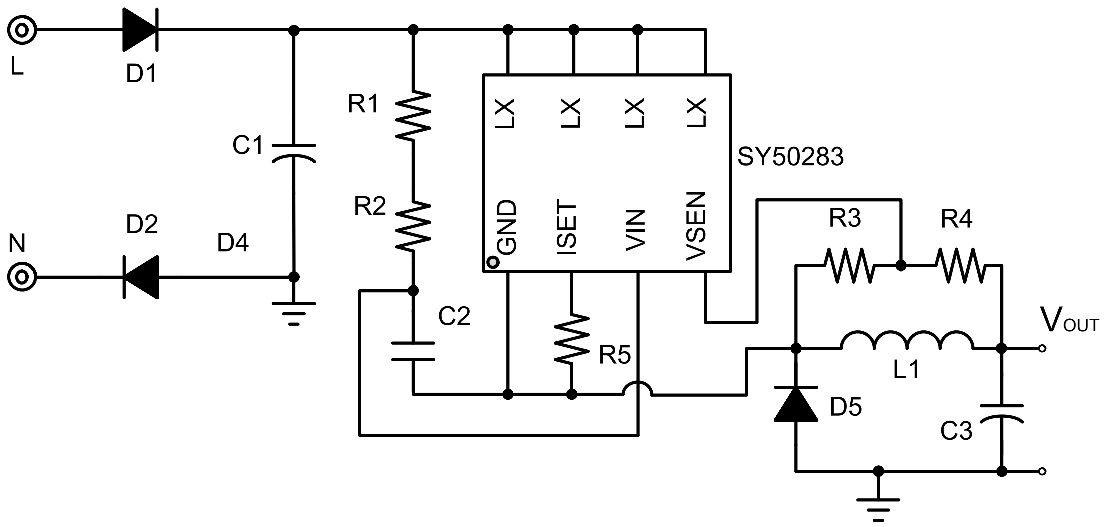
- Integrated 500V MOSFET
- CC/CV Control Eliminates Aux-winding
- Quasi-Resonant (QR) Mode to Achieve Low Switching Losses
- Low Start Up Current: 15μA Typical
- Maximum Frequency Limit: 45kHz
- Compact Package: SO8

Applications

- AC/DC Adapters
- Battery Chargers

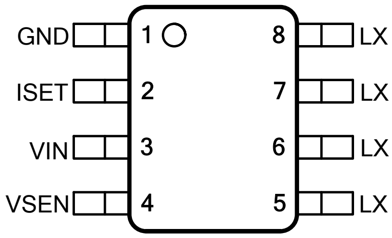
Recommended Operating Output Power	
Products	90~264Vac
SY50283	4.2W

Typical Applications



Ordering Information

SY50283□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code



Pinout (Top view)

Ordering Number	Package	Top Mark
SY50283FAC	SO8	BJUxyz

x=year code, y=week code, z= lot number code

Pinout (top view)

Pin Name	Pin number	Pin Description
GND	1	Ground Pin.
ISET	2	Current set pin. Connect a resistor to program the output limit current.
VIN	3	Power supply pin.
VSEN	4	Voltage sense pin. Connect to a resistor divider of inductor or auxiliary winding to sense output voltage.
LX	5,6,7,8	Internal HV MOSFET drain pin.

Absolute Maximum Ratings (Note 1)

ISET --- -0.3V~3.6V
VIN, VSEN -- -0.3V~17V
I_{VIN}--10mA
I_{LX}---1.4A
LX---500V
Power Dissipation, @ TA = 25 ℃ SO8---1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA}--125 ℃/W
SO8, θ_{JC}--60 ℃/W
Junction Temperature Range -- -45 ℃ to 150 ℃
Lead Temperature (Soldering, 10 sec.) --- 260 ℃
Storage Temperature Range -- -65 ℃ to 150 ℃

Recommended Operating Conditions

VIN --- 9V~16V
ISEN--- 0V~1V
Junction Temperature Range -- -40 ℃ to 125 ℃

Electrical Characteristics

(V_{VIN} = 12V (Note 3), T_A = 25 ℃ unless otherwise specified)

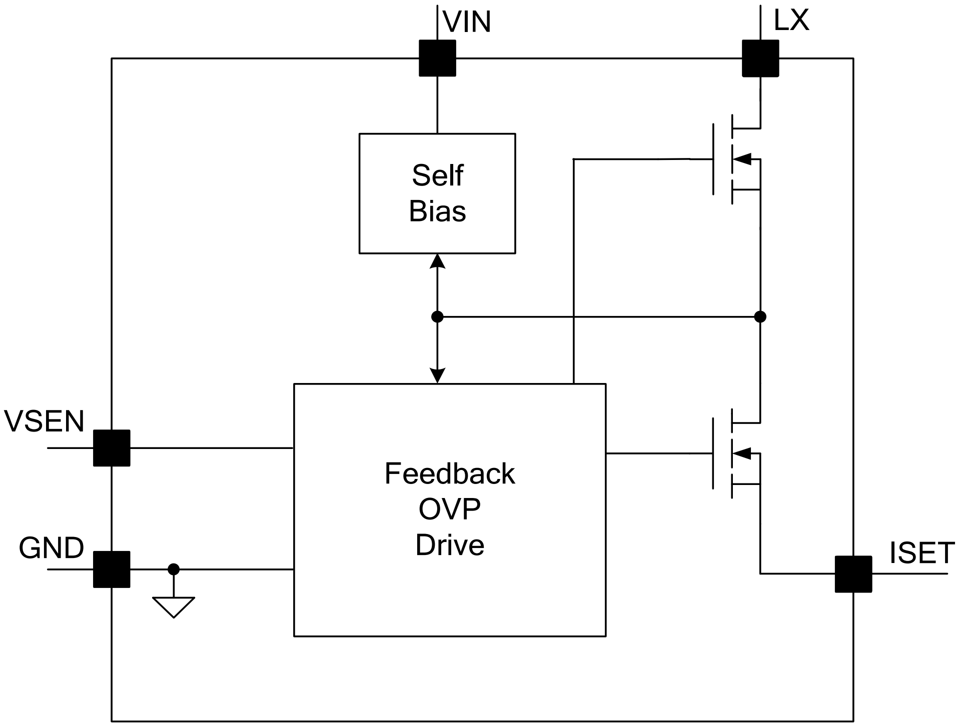
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}		13.5	14.6	16	V
VIN Turn-off Threshold	V_{VIN_OFF}		6.3	7	7.8	V
Startup Current	I_{ST}			15	18	μA
VSEN Pin Section						
VSEN Pin Over Voltage	V_{VSEN_OVP}			V_{VSEN_REF} × 1.03		V
VSEN Pin Reference Voltage	V_{VSEN_REF}		1.215	1.25	1.285	V
Driver Section						
Min ON Time	T_{ON_MIN}			300		ns
Max ON Time	T_{ON_MAX}			25		μs
Min OFF Time	T_{OFF_MIN}			1.8		μs
Max OFF Time	T_{OFF_MAX}			150		μs
Minimum Switching Period	T_{PERIOD_MIN}			22		μs
ISET Pin Section						
Current Reference	V_{REF}		620	675	710	mV
Integrated MOSFET Section						
BV of HV MOSFET	V_{BV}	V_{GS}=0V,I_{DS}=250μA	500			V
Static Drain-Source On-Resistance	R_{DSON}	V_{GS}=12V,I_{DS}=0.1A		7	8.5	Ω
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25 ℃ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3:Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

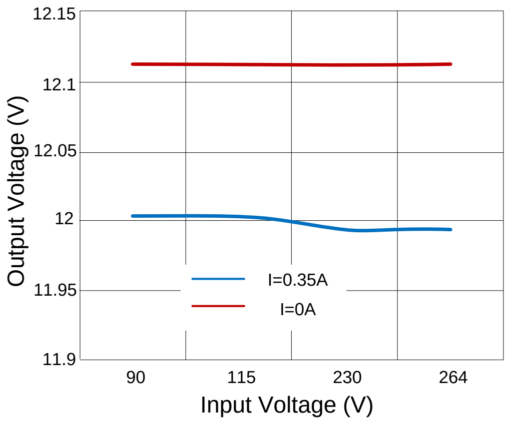
Block Diagram



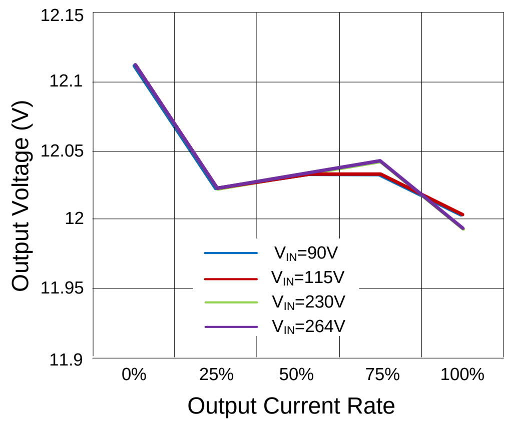
Typical Performance Characteristics

(Test condition: input voltage: 90~264Vac; output spec: 12Vdc_0.35A; Ambient temperature: 25±5 ℃; Ambient humidity:65±25%.)

Line Regulation

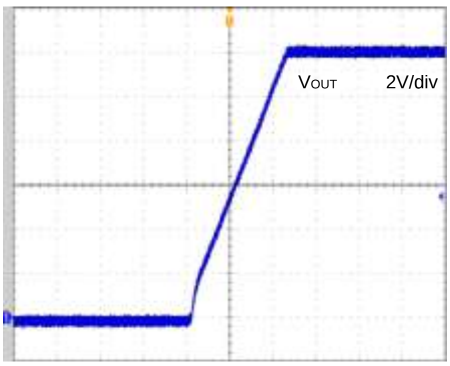


Load Regulation



Startup

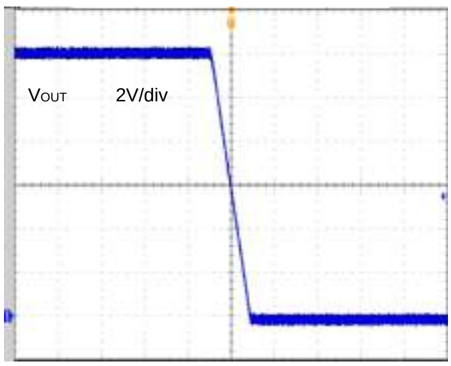
(V_{IN}=115$V_{(AC)}$)



Time (20ms/div)

Shutdown

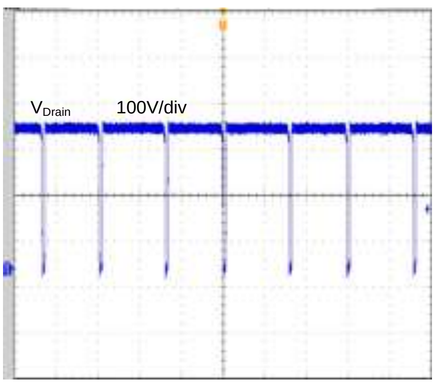
(V_{IN}=115$V_{(AC)}$)



Time (20ms/div)

Steady States

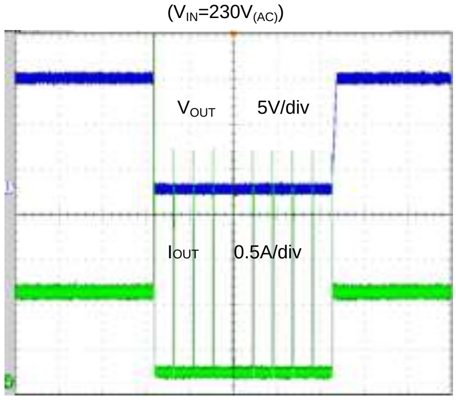
(V_{IN}=230$V_{(AC)}$)



Time (4μs/div)

Short Circuit Protection

(V_{IN}=230$V_{(AC)}$)



Time (400ms/div)

Operation Principles

Start-up Operation

After AC supply or DC BUS is powered on, the rectified BUS voltage will ramp up. The capacitor across VIN and GND pins, C_{VIN}, is charged up by the BUS voltage through a startup resistor R_{ST}. When V_{VIN} rises to V_{VIN_ON}, the internal blocks will start the operation. V_{VIN} will subsequently be pulled down by the power consumption of the circuitry until the auxiliary winding of Flyback transformer can supply sufficient energy to maintain V_{VIN} above V_{VIN_OFF}.

The start-up procedure is divided into two sections, as shown in Fig.1: t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The startup time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

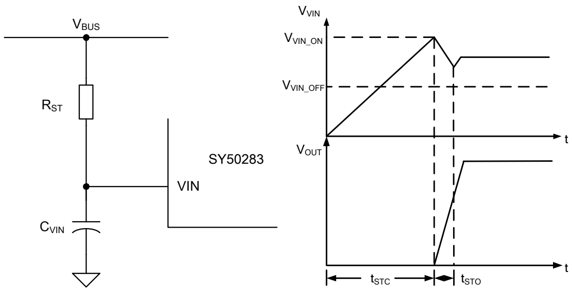


Fig.1 Start up

The startup resistor R_{ST} and C_{VIN} are designed by the following rules:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If R_{ST} and C_{VIN} are chosen to a very small startup time, SCP and OVP power loss will be large. Then C_{VIN} and R_{ST} time constant should be increased.

Proprietary self-bias technique allows C_{VIN} to be charged every switching cycle. There is no need to add auxiliary winding for power supply. C_{VIN} can be chosen with small value and small package to save cost

Shut-down Operation

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of Flyback transformer cannot supply enough energy to the VIN pin, V_{VIN} will decrease. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working.

Quasi-Resonant Operation (Valley Detection)

The Quasi-Resonant switching mode is applied, which means to turn on the integrated MOSFET at voltage valley. QR mode operation provides the low turn-on switching losses for Flyback converter.

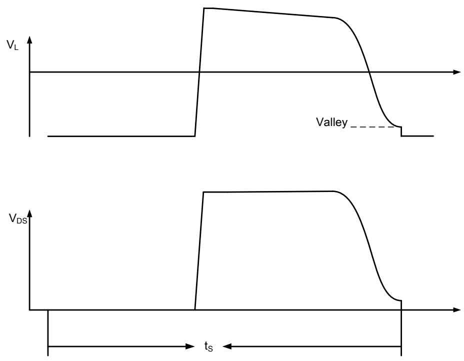


Fig.2 QR mode operation

VSEN pin detects the inductor voltage by a resistor divider. When the voltage across drain and source of the integrated MOSFET is at voltage valley, the MOSFET would be turned on.

Output voltage control (CV Control)

In order to achieve primary side constant voltage control, the output voltage is sensed by the inductor voltage.

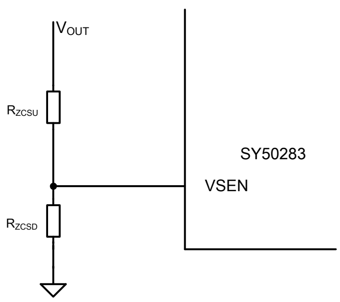


Fig.3 VSEN pin connection

As shown in Fig.4, during OFF time, the voltage across the inductor is

$$V_L = V_{OUT} + V_{D\_F} \quad (3)$$

V_{D_F} is the forward voltage of the power diode; V_L is the voltage across the inductor.

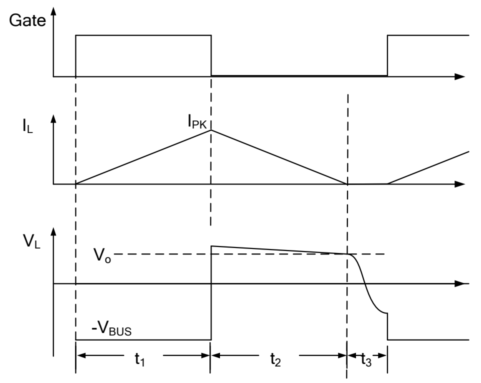


Fig.4 inductor voltage waveforms

At the current zero-crossing point, V_{D_F} is zero, so V_{OUT} is proportional to V_{AUX}. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by.

$$\frac{V_{VSEN\_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \quad (4)$$

Where V_{VSEN_REF} is the internal voltage reference.

Output Current Control (CC control)

The switching waveforms are shown in Fig.5. the maximum output current I_{OUT_LIM} can be set by

,

$$I_{OUT\_LIM} = \frac{I_{PK}}{2} \times \frac{t_{EFF}}{t_S} \quad (5)$$

Where I_{PK} is the peak current of the inductor; t_{EFF} is the effective time of inductor current rising and falling: t_S is the switching period.

I_{PK} and t_{EFF} can be detected by ISET and VSEN pin, which is shown in Fig.5. These signals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.

$$V_{REF} = I_{PK} \times R_{ISET} \times K \times \frac{t_{EFF}}{t_S} \quad (6)$$

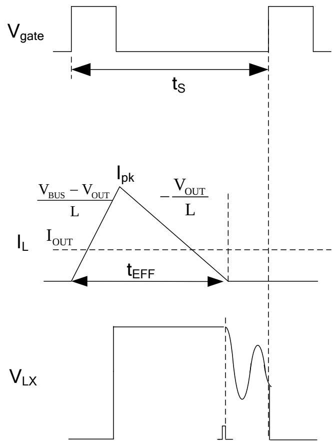


Fig.5 switching waveforms

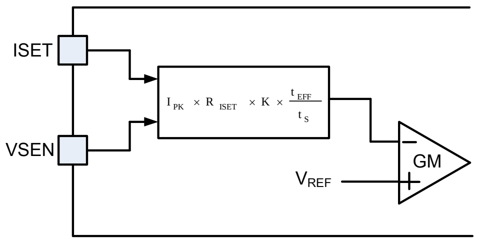


Fig.6 Output current detection diagram

Finally, the output limit current I_{OUT_LIM} can represented by

$$I_{OUT\_LIM} = \frac{V_{REF}}{2R_{ISET}} \quad (7)$$

Where V_{REF} is the internal reference voltage; R_{ISET} is the current set resistor. I_{OUT_LIM} can be programmed by R_{ISET}.

$$R_{ISET} = \frac{V_{REF}}{2I_{OUT\_LIM}} \quad (8)$$

When the over current operation or short circuit operation takes place, the output current will be limited at I_{OUT_LIM}. The V-I curve is shown as Fig.7.

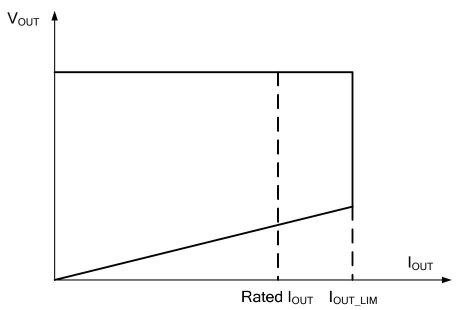


Fig.7 V-I curve

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Line Regulation Modification

The IC provides line regulation modification function to improve line regulation performance.

Due to the sample delay of ISET pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISET_C} is added to ISET pin during ON time to improve such performance. This ΔV_{ISET_C} is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISET\_C} = (V_{BUS} - V_{OUT}) \times \frac{k_1}{R_{VSENU}} \times R_{ISET} \quad (8)$$

Where R_{VSENU} is the upper resistor of the divider; k_1 is an internal constant as the modification coefficient.

The compensation is mainly related with R_{VSENU}, larger compensation is achieved with smaller R_{VSENU}.

Fault Protection modes

Over Temperature Protection (OTP)

SY50283 includes over-temperature protection (OTP) circuitry to prevent the overheating due to the excessive power dissipation. It will shut down the switching operation when the junction temperature exceeds the OTP threshold, about 150℃. In OTP mode, if the junction temperature decreases by approximately 20℃, the IC will resume the normal operation. For a continuous normal operation, provide an adequate cooling so that the junction temperature does not exceed the OTP threshold.

Short Circuit Protection (SCP)

When the output is shorted, demagnetizing voltage of inductor is zero, T_{OFF} will be clamped at T_{OFF_MAX}. When T_{OFF_MAX} shows up for 64 times, SCP is triggered and the IC will discharge V_{VIN} by an internal current source I_{VIN_SCP}. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by BUS voltage through start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

Power Supply Design Considerations

Power Rating

A few applications are shown as below.

Products	Input range	Output		Temperature rise
SY50283	90Vac~264Vac	3.6W	12V/0.3A	45℃
	90Vac~264Vac	4.2W	12V/0.35A	50℃

The test is conducted in a natural cooling condition at 25℃ ambient temperature.

MOSFET and Diode

When the operation condition is with the maximum input voltage and full load, the voltage stress of the integrated MOSFET and output power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2} V_{AC\_MAX} \quad (9)$$

$$V_{D\_R\_MAX} = \sqrt{2} V_{AC\_MAX} \quad (10)$$

Where $V_{AC,MAX}$ is maximum input AC RMS voltage. When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

Inductor (L)

In Quasi-Resonant mode, each switching period cycle, t_S, consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.8.

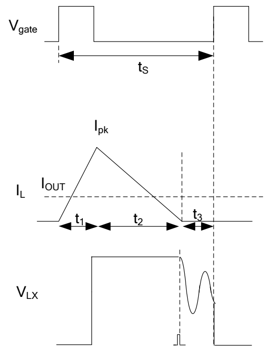


Fig.8 switching waveforms

Under the conditions of the minimum input AC RMS voltage and full load, the switching frequency is the minimum while the peak current through integrated MOSFET is the maximum.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be designed. The design flow is shown below:

(a) Preset the minimum frequency f_{S_MIN}

(b) Compute relative t_S, t_1

$$t_S = \frac{1}{f_{S\_MIN}} \quad (11)$$

$$t_1 = \frac{t_2 \times (V_{OUT} + V_{D\_F})}{(\sqrt{2} \times V_{AC\_MIN} - V_{OUT})} \quad (12)$$

$$t_2 = t_S - t_1 \quad (13)$$

Where V_{D_F} is the forward voltage of the diode

(c) Compute the maximum peak current $I_{L\_PK\_MAX}$ and inductor L.

$$I_{L\_PK\_MAX} = \frac{2 \times V_{OUT} \times I_{OUT}}{\sqrt{2} \times V_{AC\_MIN} \times \frac{t_1}{t_s} \times \eta} \quad (14)$$

$$L = \frac{(\sqrt{2}V_{AC\_MIN} - V_{OUT}) \times t_1}{I_{L\_PK\_MAX}} \quad (15)$$

(f) Compute RMS current of the inductor

$$I_{L\_RMS\_MAX} = \frac{I_{L\_PK\_MAX}}{\sqrt{3}} \quad (16)$$

(g) Compute RMS current of the MOSFET

$$I_{MOS\_RMS\_MAX} = I_{L\_PK\_MAX} \times \sqrt{\frac{t_1}{3t_S}} \quad (17)$$

Inductor Design Considerations

The key transformer parameters are shown below:

Necessary parameters	
Inductance	L
inductor maximum current	$I_{L\_PK\_MAX}$
inductor maximum RMS current	$I_{L\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

$\Delta B = 0.22 \sim 0.26T$

(c) Compute inductor turn N

$$N = \frac{L \times I_{L\_PK\_MAX}}{\Delta B \times A_e} \quad (18)$$

(d) Select an appropriate wire diameter

With $I_{L\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from $4A/mm^2$ to $10A/mm^2$.

(c) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Input capacitor C_{BUS}

Generally, the input capacitor C_{BUS} is selected by

$C_{BUS} = 4\mu F/W$ (Half bridge rectifier), or

$C_{BUS} = 2\mu F/W$ (Full bridge rectifier)

Or more accurately by (Full bridge rectifier)

$$C_{BUS} = \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}}) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2f_{IN}V_{AC\_MIN}^2[1 - (1 - \frac{\Delta V_{BUS}}{\sqrt{2}V_{AC\_MIN}})^2]} \quad (19)$$

Where ΔV_{BUS} is the voltage ripple of BUS line

Layout Considerations

(a) To achieve a good EMI performance and to reduce the line frequency voltage ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept as small as possible.

(c) Bias supply trace should be connected to the bias supply capacitor first and then to the GND pin. The bias supply capacitor should be put beside the IC.

(d) The loop consisting of ' ISET pin – current sample resistor – GND pin' should be kept as small as possible.

(e) The resistor divider connected to VSEN pin is recommended to be put beside the IC.

(f) The control circuit is recommended to be put outside the power circuit loop.

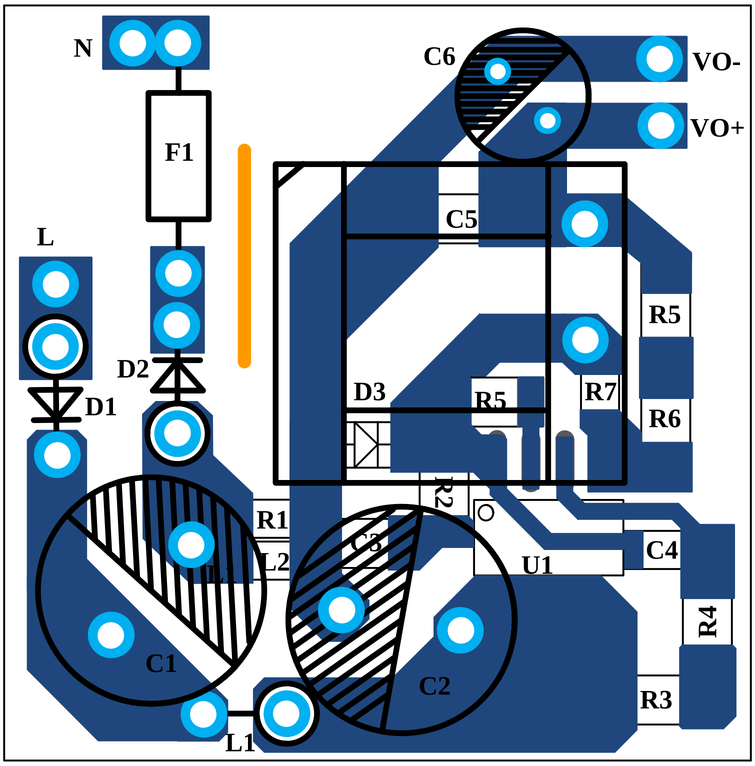


Fig.9 Example Layout

Design Example

A design example of typical application is shown below step by step.

#1. Identify Design Specification

Design Specification			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
V_{OUT}	12V	I_{OUT}	0.35A
η	78%		

#2. Inductor design(L)

Refer to **Inductor (L)**

Design Specification			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
V_{OUT}	12V	I_{OUT}	0.35A
P_{OUT}	4.2W	η	78%
f_{IN_MIN}	35KHz	V_{D_F}	1V

(a) Compute relative t_S, t_1

$$t_S = \frac{1}{f_{S\_MIN}} = \frac{1}{35k} = 28.57\mu s$$

$$t_1 = \frac{(t_s - t_1)\times(V_{OUT}+V_{D\_F})}{\sqrt{2}\times V_{AC\_MIN} - V_{OUT}} = \frac{(28.57\mu s - t_1)\times 13V}{115V} = 2.9\mu s$$

(b) Compute maximum peak current $I_{L\_PK\_MAX}$ and inductor L

$$I_{L\_PK\_MAX} = \frac{2\times V_{OUT}\times I_{OUT}}{\sqrt{2}\times V_{AC\_MIN}\times\frac{t_1}{t_s}\times\eta} = \frac{2\times 12V\times 0.35A}{\sqrt{2}\times 90V\times\frac{2.9\mu s}{28.57\mu s}\times 0.78} = 0.84A$$

$$L = \frac{(\sqrt{2}\times V_{AC\_MIN} - V_{OUT})\times t_1}{I_{L\_PK\_MAX}} = \frac{115V\times 2.9\mu s}{0.84A} = 397uH$$

Set L =400uH

#3. Compute Input capacitor

Refer to **Input capacitor C_{BUS}**

Generally, the input capacitor C_{BUS} is selected by
$C_{BUS} = 4\mu F/W$ (half bridge rectifier), or
$C_{BUS} = 2\mu F/W$ (full bridge rectifier).

Then C_{BUS}=4×4.2W=16.8uF

#4. Set VIN pin

Refer to **Start up**

Conditions			
V_{BUS_MIN}	$90V\times\sqrt{2}$	V_{BUS_MAX}	$264V\times\sqrt{2}$
I_{ST}	18μA (max)	V_{VIN_ON}	14.6V (typical)
t_{ST}	2s (designed by user)		

(a) R_{ST} is preset

$$R_{ST}<\frac{V_{BUS\_MIN}}{I_{ST}}=\frac{90V\times\sqrt{2}}{18\mu A}=7.07M\Omega$$

Set R_{ST}

R_{ST}=4M

(b) Design C_{VIN}

$$C_{VIN}=\frac{(\frac{V_{BUS\_MIN}}{R_{ST}}-I_{ST})\times t_{ST}}{V_{VIN\_ON}}=\frac{(\frac{90V\times\sqrt{2}}{4M\Omega}-18\mu A)\times 2s}{14.6V}=1.89\mu F$$

Set C_{VIN}

C_{VIN}=2.2μF

#5. Set current sense resistor to achieve ideal output current

Refer to **Constant-current control**

Known conditions at this step			
V_{REF}	0.675V	I_{OUT_LIM}	0.525A

The current sense resistor is

$$R_{ISET}=\frac{V_{REF}}{2\times I_{OUT\_LIM}}=\frac{0.675V}{2\times 0.525A}=0.64\Omega$$

Set R_S

R_S=0.68Ω

#6. Set VSEN pin

Refer to **Output Voltage Control**

Conditions			
V_{OUT}	12V	V_{VSEN_REF}	1.25V
R_{VSENU}	38K		

Compute R_{VSEND}

$$R_{VSEND} = \frac{R_{VSENU} \times V_{VSEN\_REF}}{V_{OUT} - V_{VSEN\_REF}} = \frac{38K \times 1.25V}{12V\text{-}1.25V} = 4.418K$$

Set R_{VSEND}

R_{VSEND} =4.3kΩ

Circuit schematic

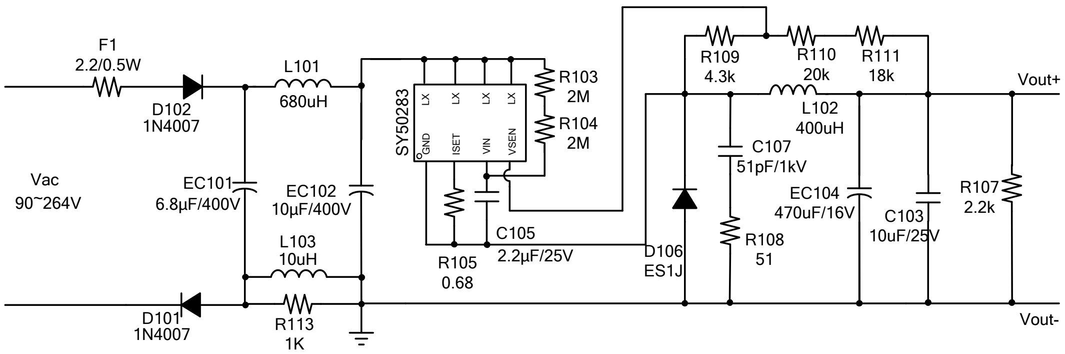
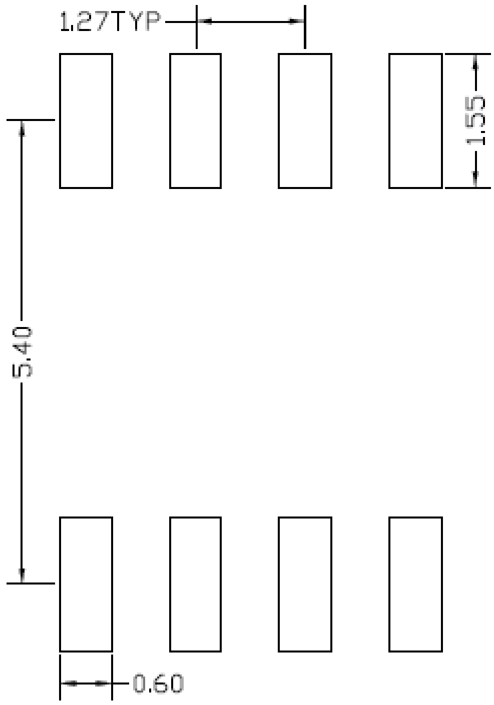
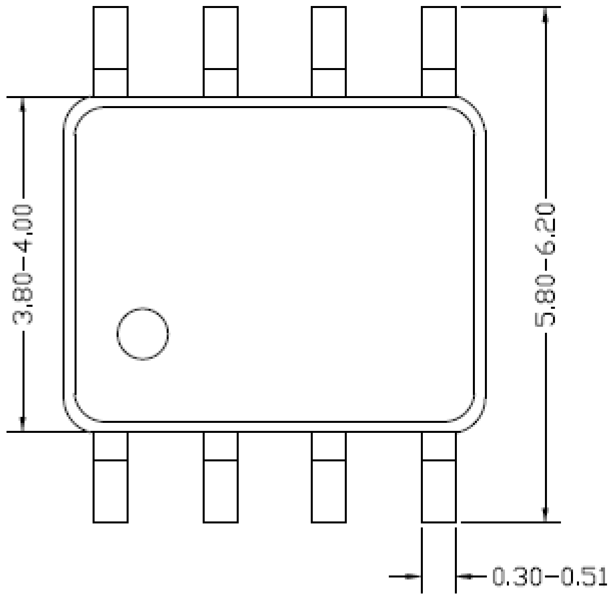


Fig.10 Example for 12V/0.35A

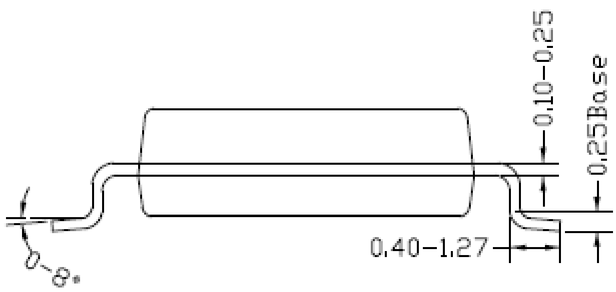
SO8 Package outline & PCB layout design



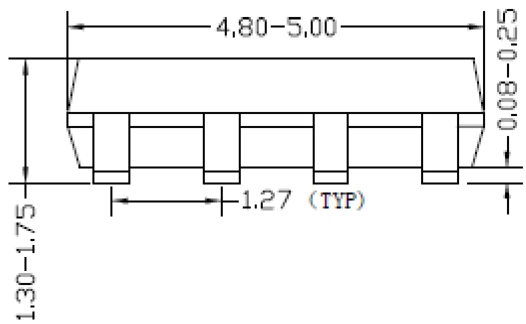
Recommended Pad Layout
(Reference only)



Top view



Side view



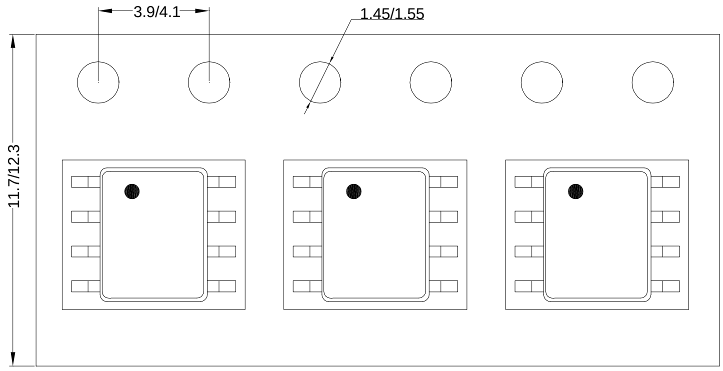
Front view

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

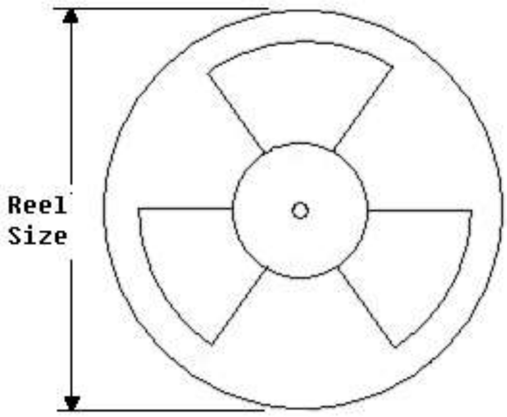
1. Taping orientation

SO8



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500

3. Others: NA

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