Application Note: SY5055A

PFC+LLC Combo Controller

General Description

The SY5055A is a PFC+LLC combo controller, which integrates a Boost PFC controller and a resonant half-bridge controller.

The Boost converter works in CrM/DCM mode to minimize switching losses and get better EMI performance. Proprietary control is adopted to get unity PF and lowest THD. Burst function increases efficiency at low load. Reliable input BO/BI protection, Boost output OVP/UVP, over current protection, Boost feedback protection guarantees safety work.

The LLC converter with proprietary control achieves fast dynamic response and easy loop compensation parameters design. The peripheral devices count is greatly reduced to save BOM cost. The SY5055A also has Output OVP, OTP and OLP for safety operation.

Ordering Information

SY5055□(□□□)

- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5055AHXP	SOP14	----

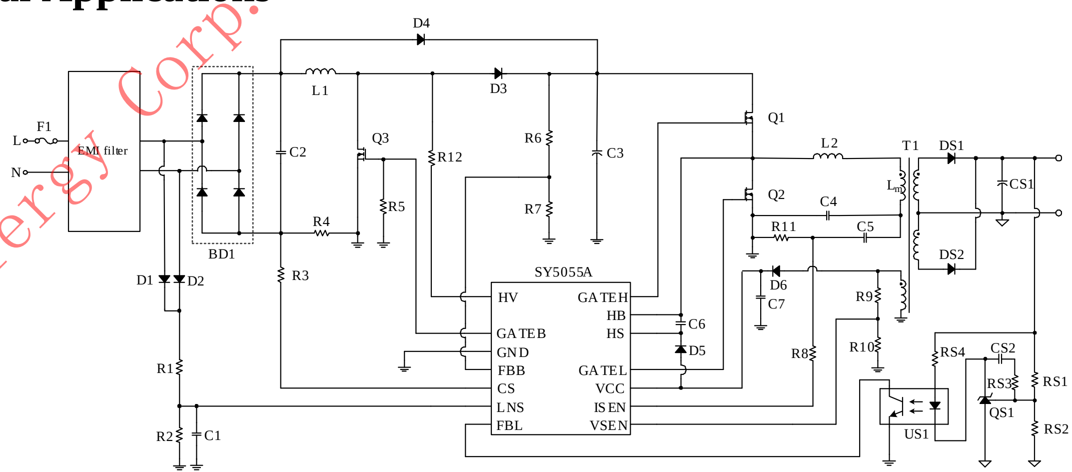
Features

- PF>0.95, THD<5%
- Boost Quasi Resonant (QR) Operation
- Boost Burst Operation at Light Load
- LLC Fast Dynamic Response
- LLC Integrated Half-bridge Driver
- Input BO/BI Protection
- Boost Output, LLC Output OVP
- Cycle by Cycle Peak Current Protection
- Over Temperature Protection
- LLC Capacitive Mode Protection

Applications

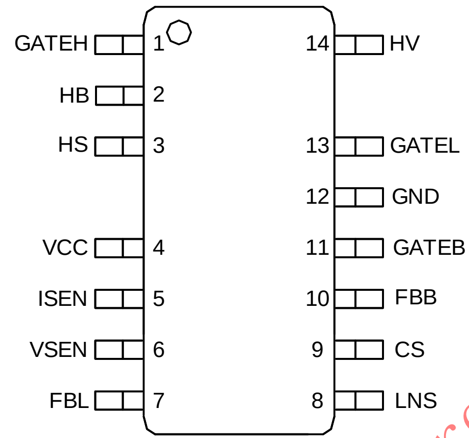
- LCD Television
- Desktop, All in One PC
- Adapter, Charger
- Printer

Typical Applications



Typical Applications

Pinout (top view)

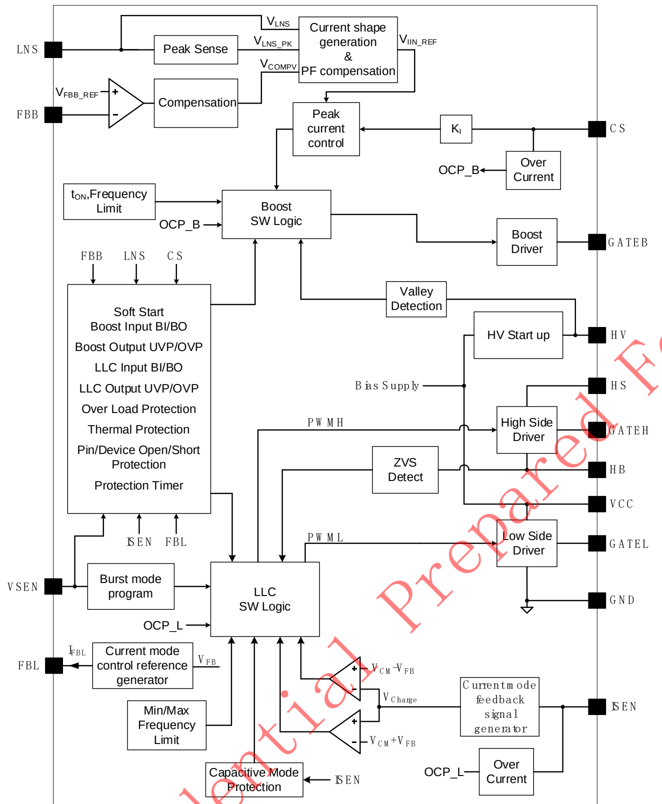


SOP14

Top Mark: GGN*xyz* (device code: GGN, ***x*=year code, *y*=week code, *z*= lot number code**)

Pin number	Pin Name	Pin Description
1	GATEH	Half-bridge controller high side drive pin.
2	HB	Half-bridge controller high side ground pin.
3	HS	Half-bridge controller high side bias supply pin.
4	VCC	Bias supply pin.
5	ISEN	Half-bridge controller resonant current sense pin.
6	VSEN	Half-bridge controller output voltage sense pin.
7	FBL	Half-bridge controller control input pin.
8	LNS	PFC controller input voltage sense pin.
9	CS	PFC controller input current sense pin.
10	FBB	PFC controller output feedback pin.
11	GATEB	PFC controller gate drive pin.
12	GND	Ground pin.
13	GATEL	Half-bridge controller low side drive pin.
14	HV	HV start-up pin.

Block Diagram



Block Diagram

Absolute Maximum Ratings (Note 1)

HV --- -0.3V ~ 650V
HB -- -3V ~ 650V
HS --- HB-0.3V ~ HB+30V
GATEH --- HB-0.3V ~ HB+15V
VCC -- -0.3V ~ 30V
I_{CS} (NOTE2) --- -10mA~+20mA
CS, ISEN -- -1.1V~+1.1V
FBB, LNS, FBL, VSEN --- -0.3V~3.6V
GATEB, GATEL -- -0.3V ~ 15V
Power Dissipation, @ T_A = 25°C SOP14--- 1.02W
Package Thermal Resistance (Note 3)

SOP14, θ_{JA}--- 122°C/W
SOP14, θ_{JC}--- 11.5°C/W

Junction Temperature Range -- -45°C~150°C
Lead Temperature (Soldering, 10 sec.) --- 260°C
Storage Temperature Range --- -65°C ~ 150°C

Recommended Operating Conditions

VCC -- 10V~24V
HS-HB -- 9V~24V
Junction Temperature Range -- -40°C ~ 125°C
Ambient Temperature Range --- -40°C ~ 105°C

Electrical Characteristics

(V_{VCC} = 15V (Note 4), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VCC Pin Section						
VCC Turn-on Threshold	V_{VCC_ON}	Voltage rising	23	24	25	V
VCC Turn-off Threshold	V_{VCC_OFF}	Voltage falling	8.5	9	9.5	V
VCC Low for HV Start Threshold	V_{VCC_LO}		8.9	9.5	10	V
VCC Short Circuit Protection	V_{VCC_SCP}		0.6	0.8	1	V
VCC Shunt Voltage Protection	V_{VCC_Shunt}		25.4	26.4	27.4	V
VCC OVP Threshold	V_{VCC_OVP}		V_{VCC_Shunt}+ 0.4	V_{VCC_Shunt}+ 0.75	V_{VCC_Shunt}+ 1.1	V
VCC OVP Trigger Number of Switching Cycles	N_{VCC_OVP}			4		
Quiescent Current	I_Q		1.3	1.6	1.9	mA
Standby Current	I_{SDY}		300	400	500	µA
Enable Off Current	I_{ENOFF}			200	280	µA
VCC Max Shunt Current	I_{Shunt}	VCC>26V (Note5)	8	11	14.5	mA
VCC Fault Restart Timer	$T_{VCC\_timeout}$		0.69	1	1.1	s
HV Pin Section						
HV Start-up Current at VCC SCP	I_{ST_L}	VCC<0.7V	0.4	0.5	0.6	mA
HV Start-up Current at Normal State	I_{ST_N}		5.2	6	7	mA
Maximum Charge Time	T_{VCC_charge}		44	63	84	ms
Boost 2nd OVP Threshold	V_{HV_OVPTH}		480	505	530	V
HV OVP Number of Consecutive off Time for Trigger	N_{HV_OVP}			4		
QR dV/dt Sense Threshold	V_{HV_TH}	(Note 5)	24	40	56	V/µs
QR Time Out Time	T_{ZCS}		2.2	3.3	4.4	µs
FBB Pin Section						
Boost Output Regulation Reference	V_{FBB_REF}		1.18	1.2	1.22	V
Boost Output UVP Threshold	V_{FBB_UVP}	16.7% of Boost V_{out}	170	200	230	mV
Boost Output OVP Threshold	V_{FBB_OVP}	107.5% of Boost V_{out}	1.255	1.29	1.325	V
Boost & LLC Disable Threshold	V_{FBB_ENB}		2.05	2.3	2.5	V
LLC Input BO Threshold	V_{FBB_BO}		690	740	790	mV
LLC Input BI Threshold	V_{FBB_BI}		900	940	980	mV
Pin Open Detection Source Current	I_{FBB_OPEN}	For open pin	50	100	200	nA
CS Pin Section						

Boost Peak Current Limit	V_{CS_LIMIT}		-740	-700	-660	mV
Inductor Saturation or Short-circuit Protection Limit	V_{LS_LIMIT}		-900	-850	-800	mV
Inductor Saturation or Short-circuit Protection Trigger Number	$N_{LStimer}$			4		
Boost Current Sense Resistor Short Circuit Protection Threshold	V_{CS_RSCP}		-65	-50	-35	mV
Boost Current Sense Resistor Short Circuit Protection Timer	T_{CS_RSCP}			4		μs
Voltage Threshold at Boost Over Power Protection	V_{COMPV_OPP}			1.33		V
Calculate Coefficient of Boost Over Power Protection	K_{PFCOPP}			0.073		
Boost over Power Protection Timer	T_{COMPV_OPP}		180	256	290	ms
LNS Pin Section						
X-cap Maximum Discharge Time	T_{X_MAX}		44	63	82	ms
X-cap Discharge Debounce Time	T_{XDIS_DBT}		44	63	82	ms
Boost Input Brown Out Timer	$T_{PROT\_LNS\_BO}$		44	63	82	ms
Boost Input Brown Out Threshold	V_{LNS_BO}		374	395	425	mV
Boost Input Brown in Threshold	V_{LNS_BI}		450	472	495	mV
Pin Open Detection Source Current	I_{LNS_OPEN}		50	100	200	nA
GATEB Pin Section						
Drive Limit Voltage	V_{GATEB_DRV}		10.1	10.9	11.6	V
Drive Voltage within $T_{on,min.B}$	V_{GATEB_TH}			8.5		V
Source Current	I_{SOURCE_GATEB}	V_{GATEB}=8.5V	400	600	800	mA
Sink Current	I_{SINK_GATEB}	V_{GATEB}=2V	0.3			A
		V_{GATEB}=11V (Note 5)	1	1.4	1.8	A
Boost Minimum ON Time	$T_{ON\_MIN\_B}$		200	300	400	ns
Boost Maximum ON Time	$T_{ON\_MAX\_B}$		20	30	40	μs
Boost Minimum OFF Time	$T_{OFF\_MIN\_B}$		0.7	1	1.5	μs
Boost Maximum OFF Time	$T_{OFF\_MAX\_B}$		20	30	40	μs
Toffmax if CS<-850mV and within $T_{LLC,delay}$	T_{offmax}		70	100	130	μs
Boost Minimum Switching Period	$T_{SW\_MIN\_B}$		2	2.9	4	μs
FBL Pin Section						

Open Loop Protection Threshold Current	$I_{FBL\_225\%}$		12	23	33	μA
Open Loop Protection Trigger Time	T_{OLP}		46	63	89	ms
Overpower Protection Trigger Time	T_{OPP}		179	256	290	ms
Max off Time for DCM Mode	T_{offmax_DCM}	$R_{ISENSE}+R_{ISEN}$=82Ω		1.67		μs
		$R_{ISENSET}+R_{ISEN}$=160Ω		2.5		μs
		$R_{ISENSET}+R_{ISEN}$=285Ω		3.3		μs
		$R_{ISENSET}+R_{ISEN}$=475Ω		5		μs
Regulated Burst Frequency for Burst Mode	F_{Burst}		0.85	1	1.4	kHz
ISEN Pin Section						
Resonant Current Sample Resistor Calculate Coefficient	k	$R_{ISENSET}+R_{ISEN}$=82Ω		4.1×10^{-7}		
		$R_{ISENSET}+R_{ISEN}$=160Ω		6.15×10^{-7}		
		$R_{ISENSET}+R_{ISEN}$=285Ω		8.21×10^{-7}		
		$R_{ISENSET}+R_{ISEN}$=475Ω		1.23×10^{-6}		
ISEN Zero Current Sense Threshold		Detect as≥0	-60	-40	-25	mV
		Detect as≤0	25	40	60	mV
LLC Current Sense Resistor Short Circuit Protection Threshold	V_{ISEN_RSCP}		30	50	80	mV
LLC Current Sense Resistor Short Circuit Protection Timer	T_{ISEN_RSCP}			4		μs
ISEN Max Current Limit	V_{ISEN_L}	R_{GATEB}=30kΩ	±600	±660	±720	mV
		R_{GATEB}=18kΩ	±700	±760	±820	mV
		R_{GATEB}=10kΩ	±8000	±860	±920	mV
ISEN Max Current Limit Protection Timer	$T_{IL\_protect}$		20	32	44	ms
VSEN Pin Section						
LLC Output OVP Counter	N_{OVP_COUNT}			4		
LLC Output OVP Reference	V_{VSEN_OVP}		1.42	1.47	1.54	V
LLC Disable Threshold	V_{VSEN_ENB}		1.8	2.2	2.5	V
LLC Output UVP Reference	V_{VSEN_UVP}		370	397	425	mV
LLC Output UVP Timer	T_{VSEN_UVP}		22	32	44	ms
Pin Open Detection Source Current	I_{VSEN_OPEN}		50	100	200	nA
GATEL Pin Section						
Drive Limit Voltage	V_{GATEL_DRV}		10.5	11.5	12.5	V
Source Current	I_{SOURCE_GATEL}	V_{GATEL}=4V	200	350	500	mA
Sink Current	I_{SINK_GATEL}	V_{GATEL}=2V	0.3			A
		V_{GATEL}=11V	1	1.4	1.8	A
LLC Minimum on Time	$T_{ON\_MIN\_L}$		250	400	550	ns
LLC Maximum on Time	$T_{ON\_MAX\_L}$		12	20	28	μs
Bootstrap Charge Time	T_{BST}		3	5	7	μs

HB Pin Section						
dV/dt Threshold for HB ZVS	dV/dt_{ZVS}		52	80	108	V/μs
Minimum Dead Time for ZVS	T_{D_MIN}		120	185	250	ns
Maximum Dead Time for ZVS	T_{D_MAX}		0.8	1	1.2	μs
HS Pin Section (Signal Refer to HB)						
HS Turn-on Threshold	V_{HS_ON}		6.5	7.5	8.5	V
HS Turn-off Threshold	V_{HS_OFF}		5.8	6.4	7.1	V
HS Quiescent Current	I_{Q_HS}		10	20	50	μA
GATEH Pin Section (Signal Refer to HB)						
Drive Limit Voltage	V_{GATEH_DRV}		10.5	11.5	12.6	V
Source Current	I_{SOURCE_GATEH}	V_{GATEH}-V_{HB}=4V	200	350	500	mA
Sink Current	I_{SINK_GATEH}	V_{GATEH}-V_{HB} =2V	0.3			A
		V_{GATEH}-V_{HB} =11V	1	1.4	1.8	A
Thermal Section						
Thermal Shut Down Temperature	T_{SD}			150		°C
Thermal Shut Down Temperature Hysteresis	T_{SD_HSY}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The IC internal diode will clamp the voltage of CS pin. During the IC operating, Ics should not exceed -10mA if Vcs reaches -1.1V.

Note 3: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4: Increase VCC pin voltage gradually higher than V_{VCC_ON} voltage then turn down to 15V.

Note 5: Guaranteed by design.

Introduction

The SY5055A is a PFC+LLC combo controller; it integrates a Boost PFC controller and a resonant half-bridge LLC controller.

The Boost converter works in CrM/DCM mode to minimize switching losses and get better EMI performance. Average current control is adopted to get unity PF and the lowest THD. Burst function increases efficiency at low load. Reliable input BO/BI protection, Boost output OVP/UVP, over current protection, Boost feedback protection guarantees safety work.

The LLC converter adopts integrated current mode control to get fast dynamic response and easy loop compensation parameters design, also peripheral capacitor sense circuit is eliminated. In contrast to traditional LLC control scheme, the SY5055A shows a high efficiency at low load due to DCM mode. This mode operates in the power region between CCM mode and Burst mode. Four level Burst point can be set simply and Burst period can be well regulated. Within the whole load range, from full load to no load, high efficiency and low audio noise can be achieved.

Function Description

PFC Section

PFC Operation Overview

The PFC operates in Quasi-Resonant (QR) or Discontinuous Conduction Mode (DCM) using valley detection to reduce the switch-on losses. The PFC is designed as a Boost converter with a fixed output voltage. An advantage of a fixed Boost converter is that the LLC can be designed to a high input voltage, making the LLC design easier. Another advantage of the fixed Boost converter is the option to use a smaller Boost capacitor value or to have a significant longer hold-up time. To improve efficiency at low output load, the system can be operated in Burst mode.

Boost PFC Basic Control Principle

The average current mode is adopted which can automatically compensate parasitic parameters to achieve the best PF/THD. The average current control block is shown as below:

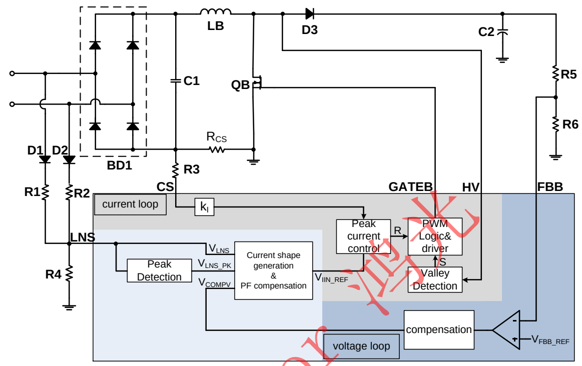


Fig. 1 PFC Control Block

In the block, voltage loop generates compensation signal V_{COMPV}. Current shape circuit generates current reference with PF compensation. The current loop regulates the input current to sine reference.

Power Curve and Modes of Operation

At heavy load, the PFC works at CrM. The duty cycle D_{SW} is 100%. In order to increase efficiency at light load, the Boost works in DCM mode. When PFC output power decreases, the V_{COMPV} which is generated by PFC output voltage control loop will drop. When it drops to below V_{COMPV_D}, DCM time increases with the decrease of V_{COMPV}. The circuit controls the time that inductor with current (T_L) to be a partial of switching period (T_{SW}). If Rcs is designed in typical value which is shown in peak current control section. The duty cycle D_{SW} drops from 100% to 10% with PFC output power Pout drops from 25% to 5%.

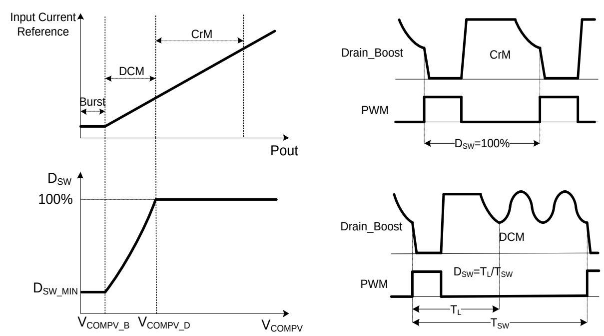


Fig. 2 Power Curve and Modes of Operation

At extremely low load, the Burst mode works to stabilize output voltage. When the PFC output power drops lower than 5% nominal power, the Boost switching soft will stop, when PFC output power is higher than 5% nominal power plus a hysteresis, Boost will switch again.

Valley Detection

The Boost stage works in quasi resonant mode to decrease switching power loss. The power MOSFET QB will turn on at resonant valley which is detected by sensing Drain voltage via HV pin. To prevent SY5055A damaged when surge energy input, a resistor is connected in series between HV pin and MOSFET Drain. The resistance value is recommended from 1kΩ to 5kΩ; V_{Drain} slope detection circuit is integrated inside the IC. When zero crossing of PFC inductor current (ZCS) is detected, then after a fixed delay time t_{QR_delay}(300ns), MOSFET QB turns on.

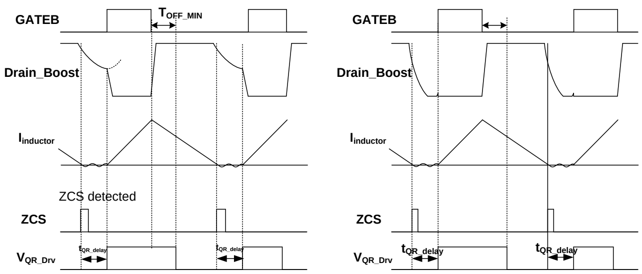


Fig.3 Valley Detection

AC Mains Sensing

AC mains sensing is through LNS pin. The LNS pin both sensing the constant value of the AC mains and the peak value of the AC mains. The AC mains peak value is worked as feed forward to change input current reference. Normally, the AC mains peak value is detected every half line cycle.

Typically, 100us filter time should be added to LNS pin considering noise immunity.

The AC mains sensing circuit is shown as below:

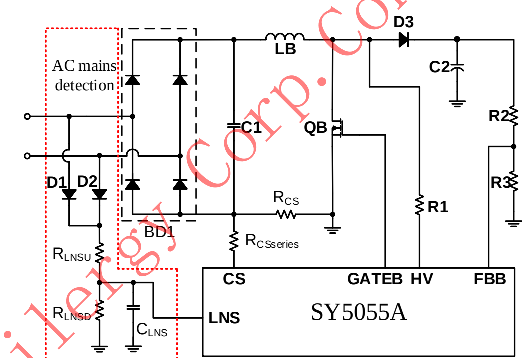


Fig.4 AC Mains Sensing Circuit

PFC Output Voltage Regulation

A resistive divider between the PFC output voltage, the FBB and GND pin sets the Boost output voltage value. When in regulation, the voltage on the FBB pin is regulated at 1.2V.

The regulated Boost PFC output voltage can be calculated as followed:

$$V_{PFC} = \frac{R_{FBBU} + R_{FBBD}}{R_{FBBD}} \times V_{FBB\_REF}$$

Typically, the system values are:

R_{FBBU}=6MΩ~12MΩ

V_{FBB_REF}=1.2V

200us filter time is suggested to add to FBB pin for noise immunity consideration.

For example, to obtain a nominal PFC output at 390V and R_{FBBU} is set at 6MΩ, the R_{FBBD} should be 18.5kΩ, and the C_{FBB} is suggested to be 10nF~22nF and the C_{FBB} should be close to FBB pin.

PFC Current Sensing

To get a unity PF, the input current should follow the input voltage shape. To minimize the input current distortion due to V_{COMPV} ripple under high line input, the peak input voltage information (V_{LNS_PK}) is fed forward to current reference. The input voltage is sensed via the resistor divider as V_{LNS}, the peak input voltage V_{LNS_PK} detection is also integrated, Ki is an internal transfer coefficient, so the input current reference V_{IIN_REF} is:

$$V_{IIN\_REF} = \frac{V_{COMPV} \times V_{LNS}}{Ki \times V_{LNS\_PK}^2}$$

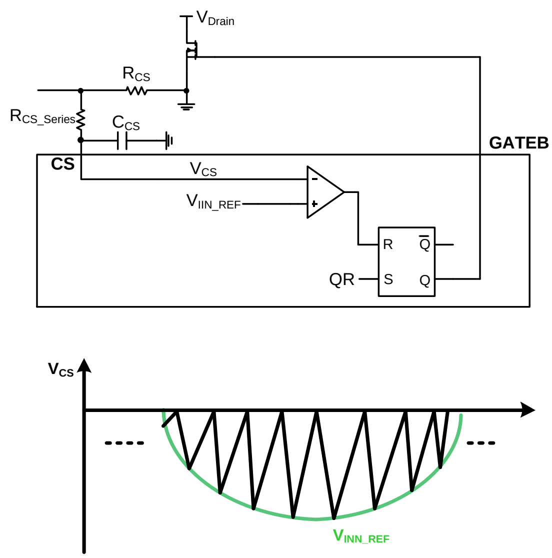


Fig.5 Peak Current Control

V_{CS} is compared with V_{IIN_REF}, when the peak current is touched, then MOSFET will be turned off. After inductor current decreases to 0, QR signal begins next switching cycle.

To design the lowest AC input and full load， the PFC works at CrM mode，the R_{CS} can be decided by:

$$R_{CS} \approx \frac{V_{CS\_LIMIT} \times V_{AC\_MIN}}{2\sqrt{2} \times P_{IN}}$$

Where the V_{CS_LIMIT} is the current limit point of PFC.

The SY5055A provides the over power protection at the PFC stage to improve the system reliability; When the

V_{COMPV} exceeds V_{COMPV_OPP} lasting for T_{COMPV_OPP} (256ms), the PFC OPP will be triggered. Normally, consider the efficiency of the LLC stage, the PFC over power protection value will be set to $\frac{P_{OUT\_MAX}}{\eta_{\_LLC}}$. To ensure the PFC OPP cannot be triggered during normal operation range, the R_{CS} should follow the formula as below:

$$R_{CS} < \frac{V_{COMPV\_OPP} \times k_{PFCOPP}}{\frac{P_{OUT\_MAX}}{\eta_{\_LLC}} \times \frac{R_{LNSD}}{R_{LNSU} + R_{LNSD}}}$$

Where V_{COMPV_OPP} is an internal voltage threshold (1.33V), and k_{PFCOPP} is a calculate coefficient (0.073). The PFC OPP value will be calculated by formula above at the minimum input voltage.

For example, $R_{LNSD} = 25k\Omega$, $R_{LNSU} = 6M\Omega$, $P_{OUT\_MAX} = 120W$, $\eta_{\_LLC} = 95\%$,

then $R_{CS} < 185m\Omega$.

Because of the PFC gate turn-off delay, the PFC OPP value will increase as input voltage increase. Normally, PFC OPP value at 264Vac input is 1.2~1.4 times of 90Vac input.

If there is no NTC in the AC input loop, during the start-up stage, there is usually a large surge current above 100A, which may cause a large voltage drop on the R_{CS}. The R_{CS_Series} is used to protect the CS pin from the surge current. The circuit is shown as below:

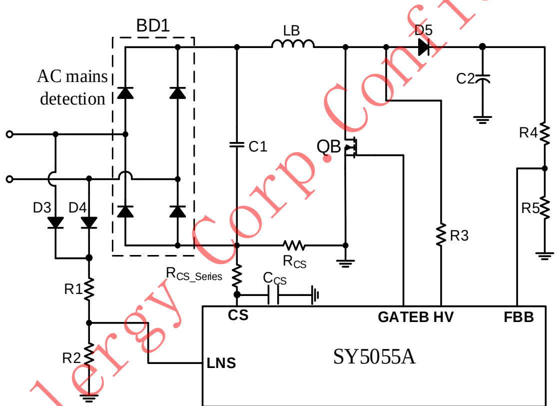


Fig.6 VR_{CS} Limit Circuit

CS series resistor R_{CS_Series} is suggested within the range of 200Ω~680Ω. In application, for some protections (PFC_OPP, FBL_OPP, FBL_OLP, VSEN_OVP, VSEN_UVP, ISEN limit), the protection action of SY5055A can be selected: If R_{CS_Series} is 220Ω, IC will stop switching and restart after $T_{VCC\_timeout}$; If R_{CS_Series} is 620Ω, IC will stop switching and latch.

For noise immunity consideration and signal delay trade off, a 100pF~470pF capacitor C_{CS} is suggested to use and close to the CS pin.

PFC Driver

In order to have good EMI performance, an optimized two-section gate driver method is adopted. In the first section, the GATEB rises to V_{GATEB_TH} (8.5V), and in the second section, after the minimum on time $t_{ON\_MIN\_B}$ has arrived, GATEB rises from V_{GATEB_TH} to V_{GATEB_DRV}(11V), The gate voltage is shown in the figure below.

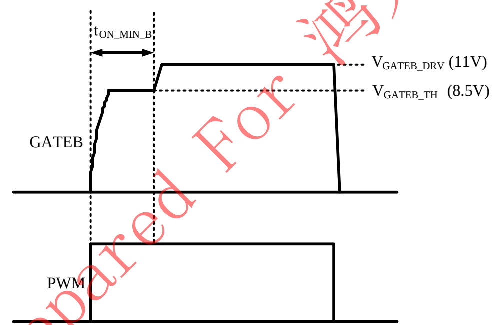


Fig.7 GATEB Waveform

Brown In and Brown Out

To prevent the Boost working in a very low input voltage (which cause too much heat and very low efficiency), the input brown out (BO) is sensed by LNS pin. When V_{LNS_PK}<V_{LNS_BO} continuously for $t_{PROT\_LNS\_BO}$, input BO is detected. So, the protected minimum input voltage $V_{AC\_MIN(RMS)}$ is,

$$V_{AC\_MIN} = \frac{V_{LNS\_BO}}{\sqrt{2}} \times \frac{R_{LNSU} + R_{LNSD}}{R_{LNSD}}$$

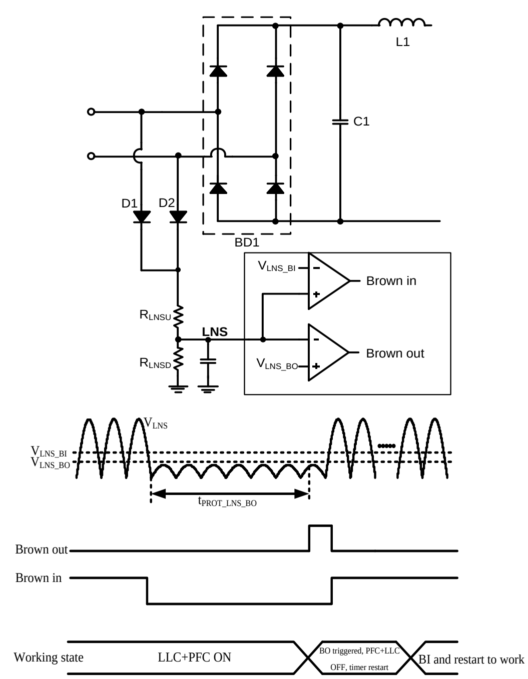


Fig.8 Brown Out Protection

After the input BO protection triggered, both two stages will stop switching and enter error timer restart. After the BO is triggered, HV will start to draw current to prevent LNS from floating high. After error timer restart is done and if $V_{LNS\_PK}>V_{LNS\_BI}$, the Boost will work with soft start again.

Typically, the R_{LNSU} is recommended within the range of 5MΩ to 12MΩ.

For example, if the Brown out point is set at 70V (AC RMS), the R_{LNSU} is set at 6MΩ, then the R_{LNSD} can be calculated as 24.3kΩ. A 1nF capacitor is suggested to be added between LNS pin and GND for the noise immunity consideration.

X-cap Discharge

When no rising edge is detected on LNS pin and last for X-cap discharge debounce time T_{XDIS_DBT}, X-cap discharge protection will be enabled. In X-cap discharge protection, both stages stop working, and HV pin sinks current to VCC to discharge all input caps. VCC is clamped high in discharge time. If input caps are all discharged, VCC slowly drops to UVLO. If AC plug in before caps all discharged, X-cap discharge protection exits immediately and system restarts to work after VCC has been charged to V_{VCC_ON}. The maximum discharge time is also T_{X_MAX} to protect HV discharge circuit. If maximum discharge time has been arrived, it stops discharging for T_{X_MAX} and then restarts to discharge.

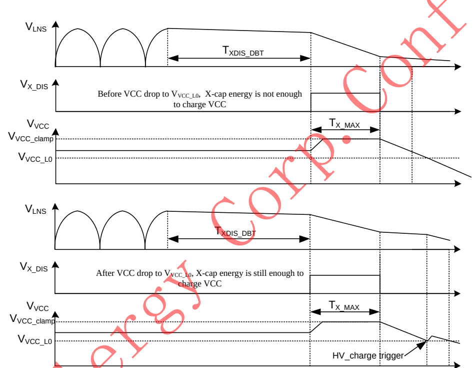


Fig.9 AC Plug Out

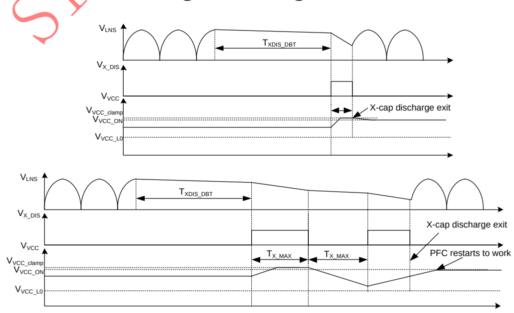


Fig.10 AC Plug Out and Then Plug in before X-cap Has Been All Discharged

PFC Output UVP and OVP

PFC output under voltage protection (UVP) protects output under voltage, FBB low side resistor or FBB pin short-circuit.

If $V_{FBB}<V_{FBB\_UVP}$, Boost stage stops switching unless $V_{FBB}>V_{FBB\_UVP}$ plus a hysteresis voltage.

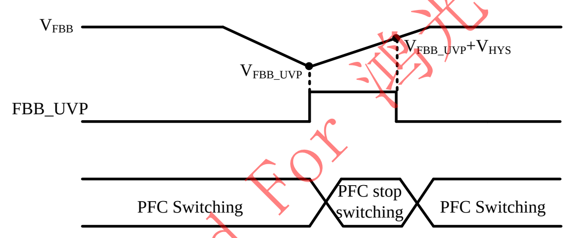


Fig.11 FBB UVP

PFC output over voltage protection (FBB OVP) protects (1) output voltage overshot due to slow loop response or fast load step, (2) input over voltage due to line voltage jitter, wrong line voltage plugs in or surge test, (3) FBB low side resistor or FBB pin open circuit.

If $V_{FBB}>V_{FBB\_OVP}$, Boost stage stops switching unless $V_{FBB}<V_{FBB\_OVP}$ minus a hysteresis voltage.

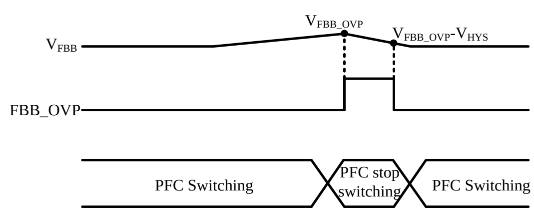


Fig.12 FBB OVP

PFC HV OVP

To prevent the output overvoltage of the PFC due to a FBB feedback loop failure, an additional PFC output overvoltage protection is available, named HV OVP. This overvoltage protection is integrated in the HV pin. If $V_{HV\_SENSE}>V_{HV\_OVPTH}$, and meanwhile the PFC output over voltage protection is not triggered, both two stage will stop switching and the IC timeout will restart. If the PFC output over voltage protection is well triggered, the HV OVP will be blanked and only will stop the PFC stage. In order to avoid the noise interference, only during the 4 PFC consecutive off period $V_{HV\_SENSE}>V_{HV\_OVPTH}$ and the PFC output overvoltage protection is not triggered, the HV_OVP can finally be triggered.

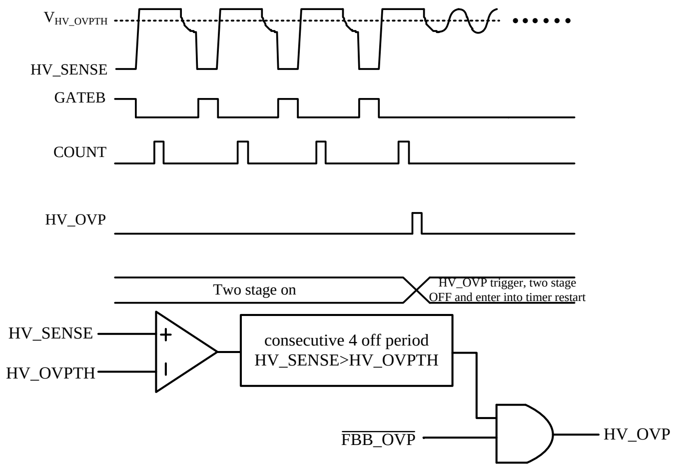


Fig.13 HV OVP

PFC Inductor Short Circuit or Saturation Protection

In order to prevent the damage of IC and MOS, the inductor short circuit protection is added. If at every PFC switching cycle V_{CS} continuously 4 times reaches to -850mV limit, it triggers inductor short circuit protection and both two stages will stop working and the IC timeout restart.

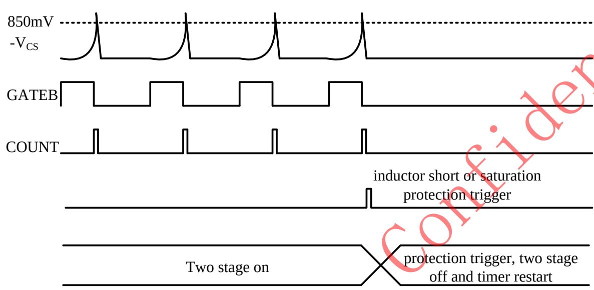


Fig.14 Inductor Short or Saturation Protection

PFC+LLC Two Stage Disable Function

For extremely low standby power requirement, the PFC and the LLC stage can be both disabled by applying a voltage over 2.3V on FBB pin.

LLC Section

Current Mode Control

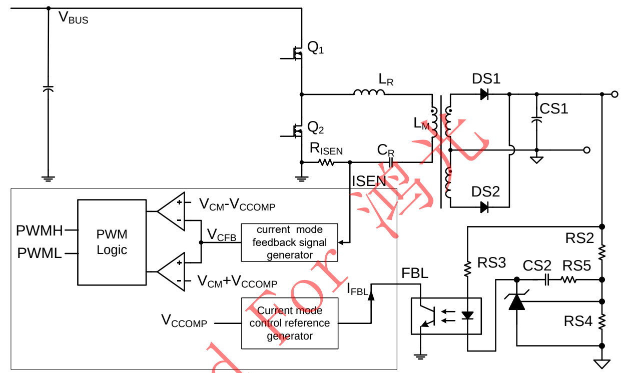


Fig.15 Control Mode Control Block

A certain current mode control is adopted in the LLC stage inner loop to achieve the fast dynamic response.

The outer loop controls output voltage via the amplifier or TL431 regulator in different applications. Via compensation circuit and opto-coupler, the compensation information will be transferred to primary side via to get I_{FBL}. The V_{CCOMP} is compensation voltage inside IC.

V_{CFB} inside the IC demonstrates current loop feedback signal. V_{CFB} has a linear relationship with the output power. The voltage changes of V_{CFB} are a result of the primary current that drives the power conversion.

V_{CFB} is compared with V_{CM}-V_{CCOMP} and V_{CM}+V_{CCOMP}.

If V_{CFB}<V_{CM}-V_{CCOMP}, PWMH=1, PWML=0, high side MOS turned on.

If V_{CFB}>V_{CM}+V_{CCOMP} PWMH=0, PWML=1, low side MOS turned on.

The typical waveforms are shown as below, when load increases, V_{CCOMP} increases. Otherwise, V_{CCOMP} decreases.

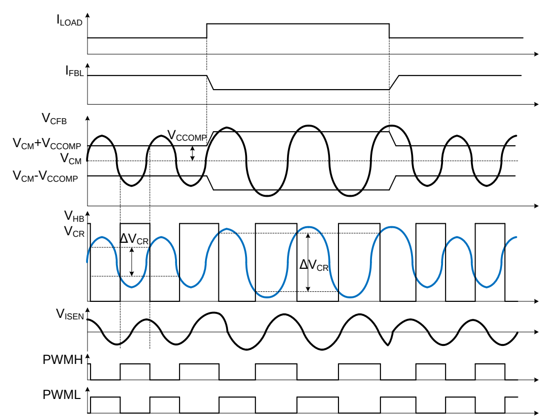


Fig.16 Current Mode Control Waveform

R_{ISEN} Design Principle

The parameters design in this charge control is shown as follows,

$$P_{IN} = V_{BUS} \times C_R \times \Delta V_{CR} \times f_{SW} + C_j \times {V_{BUS}}^2 \times f_{SW}$$

C_j is the total junction capacitance. P_{IN} is the LLC input power. The C_R is the resonant capacitor, the ΔC_R is the voltage change on the C_R at PWMH=1 stage.

$$\Delta V_{CR} = \frac{P_{IN} - C_j \times {V_{BUS}}^2 \times f_{SW}}{V_{BUS} \times C_R \times f_{SW}}$$

The relationship between V_{CCOMP} and ΔV_{CR} is,

$$\Delta V_{CR} = V_{CCOMP} \times \frac{2 \times k}{C_R \times R_{ISEN}}$$

And the current sense resistor R_{ISEN} could be chose to,

$$R_{ISEN} = \frac{2 \times V_{CCOMP\_OPP} \times k \times V_{BUS} \times f_{SW}}{P_{IN} - C_j \times {V_{BUS}}^2 \times f_{SW}}$$

Where k is the R_{ISEN} calculation coefficient. k can be set suitable for different working frequency application. V_{CCOMP_OPP} is the IC internal voltage threshold. Its typical value is 500mV. The setting principle will be demonstrated in external setting principal section. For typical application, there is a preferable resonant current sensing method as shown below.

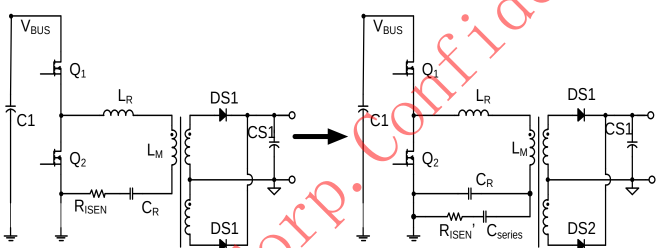


Fig.17 Resonant Current Sense Circuit

$$R'_{ISEN} = \frac{C_R}{C_{series}} R_{ISEN}$$

In this way, the loss of sensing resistor can be decreased.

For example, if the designed operating frequency fsw=100kHz, the input voltage V_{BUS}=400V, the Maximum input power P_{IN_OPP}=120W, the resonant capacitor C_R=33nF, current split capacitor C_{series}=200pF, C_j=200pF, V_{CCOMP_OPP}=500mV,

$$R_{ISEN} = \frac{2 \times V_{CCOMP\_OPP} \times k \times V_{BUS} \times f_{SW}}{P_{IN} - C_j \times {V_{BUS}}^2 \times f_{SW}} = 0.281\Omega$$

Thus, R_{ISEN}'= (33/0.2)*R_{ISEN}=68Ω

Power Curve and Operation Modes

The power curve is shown as below.

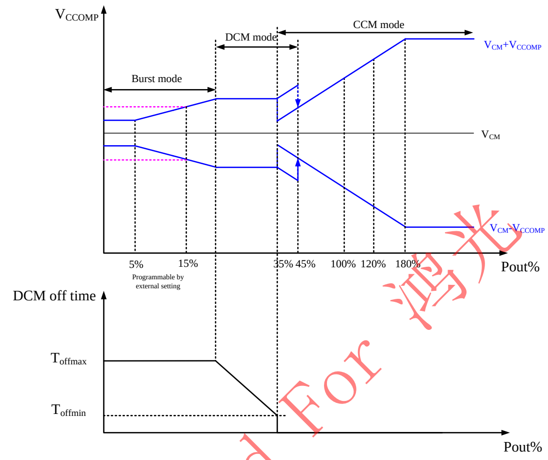


Fig.18 Power Curve and Modes of Operation

There are three operation modes from heavy load to light load: (1) CCM mode; (2) DCM mode; (3) Burst mode.

In CCM mode, the CCM mode operates in continuous switching with a 50 % duty cycle, which is like the traditional LLC operation via frequency control. In all operation modes, the current mode control is adopted and the adaptive non-overlap function based on the HB end-of-slope detection switches on the gate driver.

The DCM mode is a kind of Burst mode at high repetition frequency. In this mode, the energy in each pulse is kept relatively high to provide better conversion efficiency. During the not-switching period, the losses are low. To avoid audible noise, the repetition frequency of the complete DCM cycle is higher than 25 kHz.

In the Burst mode, each Burst cycle consists of a series of DCM cycles and sleep time. The Burst mode frequency is well regulated at most 1 kHz to avoid audible noise. The transition level of entering Burst mode can be preset using the VSEN pin. This preset principle will be demonstrated in the external setting principal section.

DCM Mode Switching

One the DCM cycle consists of five PWM pulses which follow Low-High-Low-High-Low sequence and sleep time which is controlled by the internal power curve. At every first time of entering DCM mode, LLC first turns on low side to make sure high side power supply is enough even after a long time of sleep. Low side will turn off after V_{CFB} reach V_{CM}-V_{CCOMP}, the following 3 switching cycles are the same as CCM mode. The last switch low side will turn off when the resonant current cross is zero. Then LLC will stop switching and the DCM off time will be decided by the power curve. After the first DCM cycle ends, the next DCM cycle will begin with detecting falling slope end of HB for QR. And the following logic as the same of the previous the DCM cycle.

The working principle of the DCM mode is shown as below:

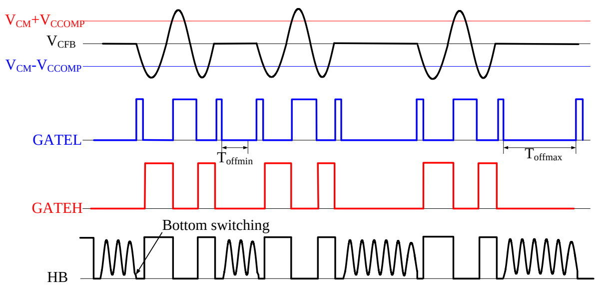


Fig.19 DCM Modes Working Principle

There are two parts of operation in the DCM mode. In the first part, the V_{CCOMP} for the DCM mode is not changed and the DCM off-time increases from T_{offmin} to T_{offmax} as load decreasing. Once the load decreased to a certain level and the sleep time has arrived the T_{offmax}, the DCM mode will enter to the second part. In the second part, the DCM off-time stays at T_{offmax} and the V_{CCOMP} will begin to decrease gradually to a certain level with load decreasing further.

Burst Mode Operation

As the output power decreasing, when the I_{FBL} rises to over the Burst mode entry threshold which can be set through VSEN pin external resistor, the IC enters sleep mode and the LLC stops switching.

When compensation voltage at secondary side rises, the I_{FBL} drops to be lower than the Burst on threshold, the LLC wakes up to work. The number of the DCM cycle is adjusted through detecting the Burst frequency. If at the current Burst cycle, the time of Burst cycle is lower than T_{Burst_ref}, in the next Burst cycle, the number of DCM cycles adds one, whereas if at current Burst cycle, the time of Burst cycle is higher than T_{Burst_ref}, in the next Burst cycle, the number of DCM cycles minus one. Each Burst cycle only changes once of number of DCM cycles. When output power increase and the I_{FBL} is lower than Burst mode entry level minus a certain level of hysteresis, the LLC exits the Burst mode and back to the DCM mode. Taking load increase for example, the Burst mode operation principle is shown below.

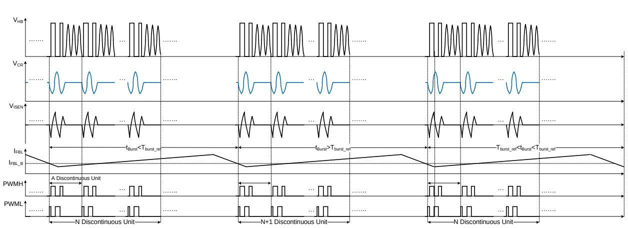


Fig.20 Burst Modes Working Principle

Adaptive Non-overlap ZVS Operation

To minimize the switching power loss, the adaptive zero voltage switching (ZVS) is adopted in every switching period. If the low side MOS turned off, V_{ISEN} must be less than V_{ISEN_0+} to enable high side ZVS; if the high side MOS turned off, V_{ISEN} must be greater than V_{ISEN_0-} to enable the low side ZVS, these constraints guarantee soft switching.

HB rising/falling slope will be detected via a slope detection circuit.

When ZVS is enabled, the dead time will begin. If HB rising or falling slope end is detected after minimum dead time T_{D_MIN}, the high side or low side MOS is turned on again. If T_{D_MAX} expires with no slope end detected, the MOS will be turned on directly.

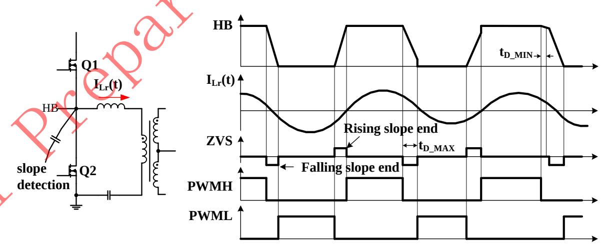


Fig.21 Adaptive Non-overlap ZVS Operation

External Setting Principle

There are three pins which are used to preset the LLC working characteristics. The GATEB pin is used to set the current limit point of the LLC. The ISEN pin is used to set the LLC working frequency range. The VSEN pin is used to set the Burst entry level.

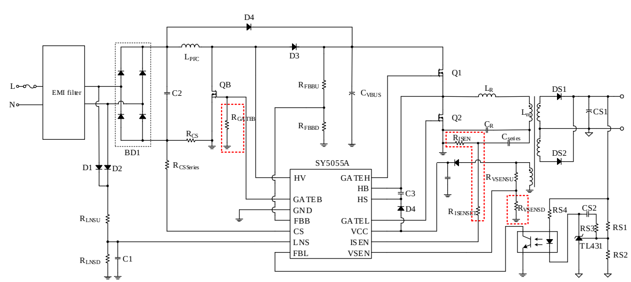


Fig.22 External Setting Circuit

LLC resonant current limit point set principle:

R_{GATEB}	Current limit point
10kΩ	±850mV
18kΩ	±750mV
30kΩ	±650mV

LLC working frequency range set principle:

$R_{ISENSET}+R_{ISEN}$	Application working frequency*	R_{ISEN} calculation coefficient k
$70\Omega < R_{ISENSET}+R_{ISEN} < 100\Omega$	300kHz	4.1×10^{-7}
$150\Omega < R_{ISENSET}+R_{ISEN} < 180\Omega$	200kHz	6.15×10^{-7}
$269\Omega < R_{ISENSET}+R_{ISEN} < 300\Omega$	150kHz	8.21×10^{-7}
$450\Omega < R_{ISENSET}+R_{ISEN} < 520\Omega$	100kHz	1.23×10^{-6}

NOTE： * Customers need set the resistance value according to the actual application working frequency range.

Burst entry level set principle:

R_{VSEND}	Burst entry point*
$3.9k\Omega < R_{VSEND} < 5.1k\Omega$	5%
$9.1k\Omega < R_{VSEND} < 11k\Omega$	15%

*Means the percentage of designed 100% load

Capacitive Mode Protection

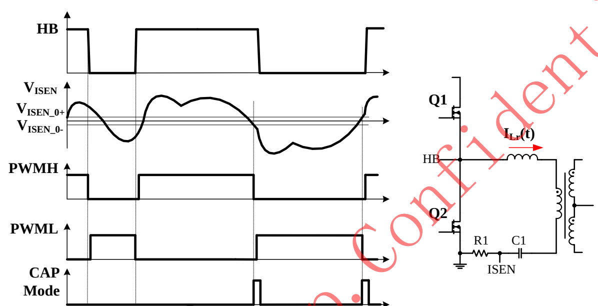


Fig.23 Capacitive Mode Operation

Capacitive mode should be prevented to avoid high switching loss and control logic error. Improved adaptive non-overlap ZVS logic is used to avoid capacitive mode switching.

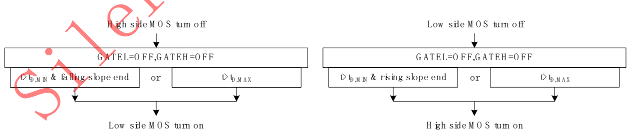


Fig.24 PWM Logic

When high side MOS turns on, if $V_{ISEN}<V_{ISEN\_0-}$, capacitive mode will be triggered and PWMH will turn off. After T_{D_MAX} expires or ZVS detected after T_{D_MIN}, the low side MOS will turn on. The resonant current is close to 0, the hard switching and shoot through of low side MOS are avoided.

The logic works the same when low side MOS turns off.

LLC Input Brown In and Brown Out

The LLC input voltage is also sensed via FBB pin.

If $V_{FBB}<V_{FBB\_BO}$, the LLC stops switching.

If $V_{FBB}>V_{FBB\_BI}$, the LLC begins to switch.

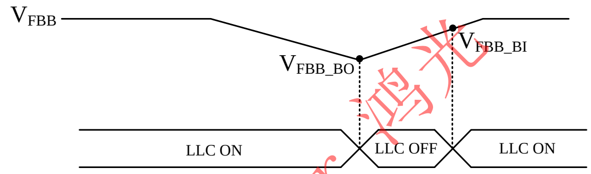


Fig.25 LLC BO and BI

LLC Output OVP

The LLC output OVP is sensed via the VSEN pin. The circuit on VSEN pin is shown as below:

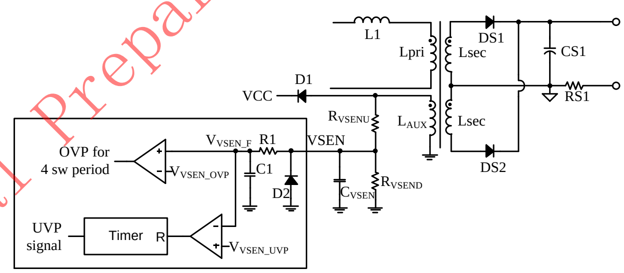


Fig.26 Output OVP and UVP Sensing Directly from AUX Winding

If $V_{VSEN\_F}>V_{VSEN\_OVP}$ for consecutive 4 LLC switching cycle, LLC output OVP is triggered.

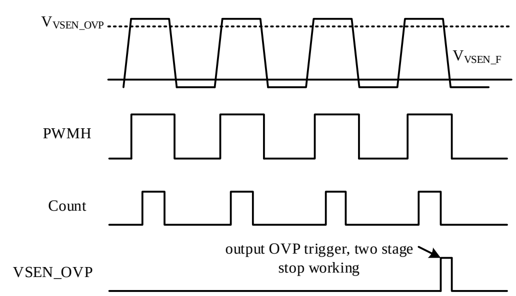


Fig.27 LLC Output OVP Logic

For example, if output voltage is regulated at Vo, and 20% over voltage range is acceptable. R_{VSEND} has been decided for Burst entry level. The R_{VSENU} can be calculated by the following equation.

$$R_{VSENU} = R_{VSEND} \times \left(\frac{120\% \times N_{AUX} \times Vo}{V_{VSEN\_OVP} \times N_{sec}} - 1 \right)$$

For noise immunity consideration, a 100pF~200pF capacitor is suggested to be applied between the VSEN pin and GND. And the capacitor should be close to the IC.

Another kind of VSEN circuit can also be adopted which is shown below. The voltage across AUX winding firstly be rectified to the DC component and then resistor divided into the VSEN pin. R_{VSEND}, R_{EVSEU} and C_{VSEN} can be chosen the same as descript above. The C_{REC} is suggested to set at 1uF.

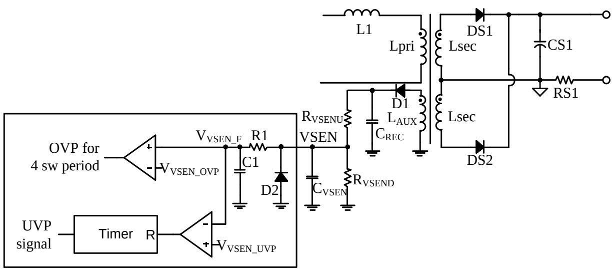


Fig.28 Output OVP and UVP Sensing Via Rectified Voltage of AUX Winding

LLC Output UVP

The LLC output UVP is also sensed via the VSEN pin. If V_{VSEN_F}<V_{VSEN_UVP} for continuous T_{VSEN_UVP}, the LLC output UVP is triggered.

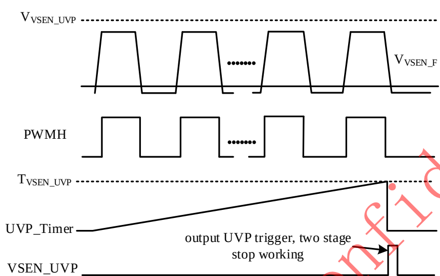


Fig.29 LLC Output UVP Logic

LLC Cycle by Cycle Current Limit Protection

V_{ISEN_L}(+) and V_{ISEN_L}(-) are the maximum current limit for LLC stage.

When $V_{ISEN\_L(+)}$ is touched, the high side MOS will be turned off immediately, the low side MOS will be turned on after dead time; When $V_{ISEN\_L(-)}$ is touched, the low side MOS will be turned off immediately, the high side MOS will be turned on after dead time.

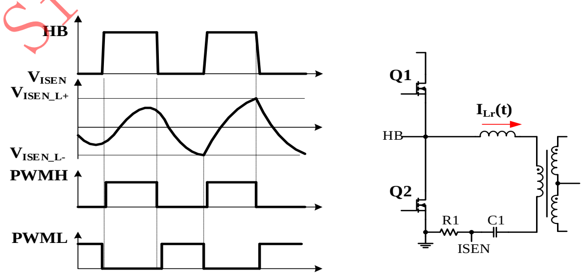


Fig.30 LLC Cycle by Cycle Current Limit Protection

When the output of LLC is short circuit, and V_{ISEN_L} has been touched cycle by cycle and last for $T_{ILL\_protect}$, output short circuit protection will be triggered.

LLC Over Power Protection (OPP)

When the output power has been over maximum value, an internal counter will be started. When this counter exceeds T_{OPP} (256ms), the LLC OPP will be triggered.

LLC Open Loop Protection (OLP)

If the secondary side feedback loop is damaged, such as the short circuited of opto-couple, to make I_{FBL} to be lower than $I_{FBL\_200\%}$ (30uA) for continuous T_{OLP} (64ms), the opening loop protection will be triggered.

VCC Over Voltage Protection (VCC OVP)

Before VCC rises to V_{VCC_OVP}, if VCC is once over V_{VCC_shunt}, the VCC shunt current I_{VCC_Shunt} will take action to pull down VCC, if VCC cannot be pulled down and continually rises to V_{VCC_OVP}, when V_{VCC}>V_{VCC_OVP} and lasts for continuous 4 LLC switching cycles, VCC OVP will be triggered.

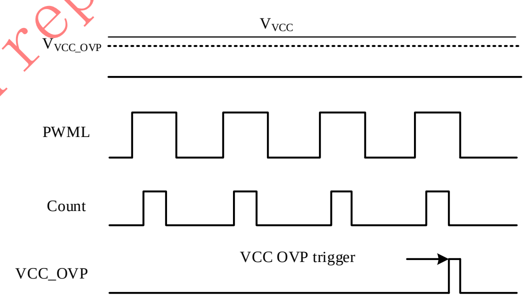


Fig.31 VCC OVP

In the LLC transformer design, the output voltage is to be regulated at Vo. So, the following design should be satisfied:

$$\frac{N_{AUX}}{N_{sec}} Vo < V_{VCC\_shunt}$$

Over Temperature Protection

The internal thermal protection works by sensing junction temperature T_J. If T_J reaches T_{SD}, all switching will stop and the IC timeout restart. Then the IC starts again, when T_J is lower than T_{SD}-T_{hys}, switching will be enabled.

Start Up and Power Supply

High Voltage Charge and VCC Management

The SY5055A controller features a HV startup current source that allows fast startup time and extremely low standby power consumption. Two startup current levels (I_{ST_L} and I_{ST_N}) are provided by the system for safety in case of short circuit between the VCC and GND pins. The HV startup current source charges the VCC capacitor before IC starts up.

VCC start-up sequence:

1） $V_{VCC}<V_{VCC\_SCP}$, the star-tup current is limited to I_{ST_L}, this logic prevents the IC over heat if the VCC is short circuit to GND (VCC cap short circuit).

2) $V_{VCC\_SCP}<V_{VCC}<V_{VCC\_ON}$, startup current is I_{ST_N}, V_{VCC} rises quickly to V_{VCC_ON} to satisfy start-up time.

3) $V_{VCC}>V_{VCC\_ON}$, the HV charge current pauses, then other logic work (sense external parameter, Boost starting switching, LLC starts switching). If VCC drops below V_{VCC_LO}, charge current works again to charge VCC. The maximum charge time after VCC start is T_{VCC_charge} to prevent over heat. This logic guarantee V_{VCC} between V_{VCC_LO} and V_{VCC_ON} before load voltage rises.

4) When V_{OUT} rises enough, the VCC will be supplied by auxiliary winding and not drop below V_{VCC_LO}, start-up current will stop. If output short circuit or other errors occur, the auxiliary winding supply will stop, then the HV start-up may works again to guarantee VCC above V_{VCC_LO}.

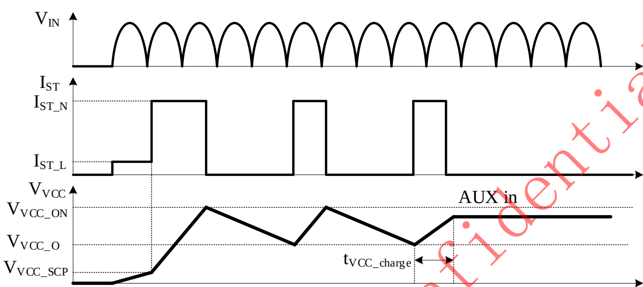


Fig.32 HV Charge Logic

High Side Driver Power Supply

An external bootstrap buffer capacitor supplies the high-side driver. The bootstrap capacitor is connected between the high-side reference HB pin and the HS pin of the high-side driver supply input. When HB is low, an external diode charges this capacitor from the VCC pin charges this capacitor.

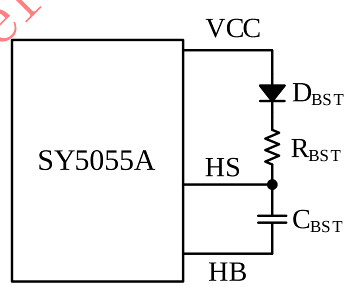


Fig.33 High Side Driver Power Supply Circuit

The external diode D_{BST} is suggested to be fast recovery and low voltage drop diode. The series resistor R_{BST} is used to limit the charge current to protect D_{BST}. Typically, the R_{BST}=1Ω~10Ω.

Capacitor Values on VCC Pin and HS Pin

Generally, two types of capacitors are used on the VCC pin. An SMD ceramic type with a smaller value located close to the IC to the filter noise and an electrolytic capacitance to supply IC operation power.

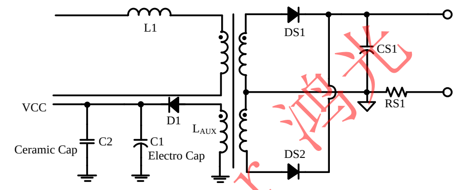


Fig.34 VCC Power Supply Circuit

Typical values are:

$C_{VCC\_electrolytical}$ = 47μF and $C_{VCC\_ceramic}$ = 1uF

The VCC capacitor must be sufficient to handle the start-up during the period when the LLC starts until the auxiliary winding takes over the supply of the VCC pin.

For example, during start-up, suppose the consumption current of IC is i_{oper}=25mA, and the time of aux winding begins to take over VCC supply is Δt=15ms, allowable VCC drop during start-up is V_{VCC_ON}-V_{VCC_Lo} which is ΔU=15V.

Then the VCC capacitor should be

$$C_{VCC} > \frac{i_{oper} \times \Delta t}{\Delta U} = 25\mu F$$

To support charging the gate of the high-side MOSFET, the HS capacitor value must be much higher than the gate capacitance. It prevents a significant decrease in voltage on the HS due to gate charges. Typically, the suggested capacitor across HS and HB is 100nF~470nF.

Protection Action Summary

PFC Protection Action		LLC Protection Action	
Item	Action	Item	Action
AC BI/BO	Two stages stop switching, restart after $T_{VCC\_timeout}$;	LLC BI/BO	LLC stop switching
PFC Output 2nd OVP		Output SCP	Two stages stop switching, restart after $T_{VCC\_timeout}$ or Latch;(Decided by CS series resistor)
PFC Inductor SCP		Output UVP	
CS resistor SCP		Output OPP	
PFC OPP	Two stages stop switching, restart after $T_{VCC\_timeout}$ or Latch;(Decided by CS series resistor)	Output OVP	
PFC Output UVP	PFC not work, all variables reset to initial value;	Opto-couple OLP	
PFC Output OVP	PFC stops switching;	ISEN current limit	
OTP	Two stages stop switching;	ISEN resistor SCP	

PCB Layout Design Rules

FBL Track Shielded by GND Tracks or Plane

Because the FBL function works on the low current levels to minimize energy consumption at no load, this signal is more sensitive to disturbance.

Disturbance by the capacitive coupling to converter switching tracks (HB or PFC DRAIN) can make regulation unstable. To avoid disturbance in FBL:

The FBL track must be placed at a relatively large distance from the power part of the converters (LLC and PFC).

Tracks along the FBL track must be grounded for shielding (and a ground plane if the design is a double-sided copper design). FBL track also should be as short as possible.

Separate GND Connections for LLC and PFC

To avoid mutual disturbances, the grounding of the PFC and LLC controller must be separated in the PCB layout structure. The current pulses through ground tracks can lead to a wrong value or a signal on a pin that uses the ground level as a reference. The main potential sources of disturbance are the significant energy switching of the PFC and LLC converters and the MOSFET gate drive currents generated by the controllers.

Figure below shows these energy flows. It also shows that, to avoid disturbances, a special ground structure can keep them separated.

Keep these energy flow loops for each converter as small as possible, concerning track length and surface area. The track length of A and B marked in the figure below should be as short as possible. By connecting the IC to the shared bulk capacitor function via a separate ground track, disturbances caused by converter current can be minimized.

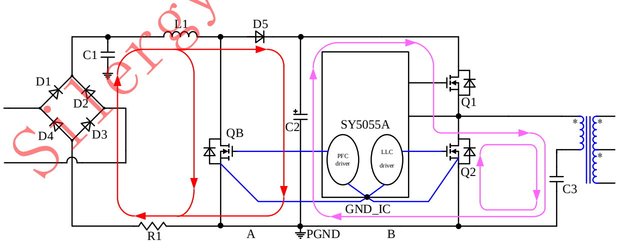
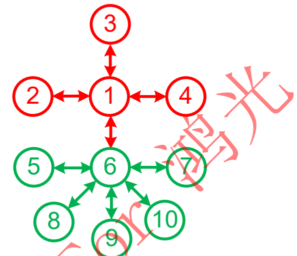


Fig35 PFC and LLC Energy Flow Loops

The connection of primary ground is recommended as:



①: Ground node of PFC bulk capacitor

②: Ground node of CS resistor and source of PFC MOS

③: Ground node of LLC resonant capacitor and source of LLC low side MOS

④: Ground node of transformer auxiliary winding

⑤: Ground node of IC GND

⑥: Ground node of VCC capacitor

⑦: Ground node of opto-coupler

⑧: Ground node of FBB pin lower resistor

⑨: Ground node of VSEN pin lower resistor

⑩: Ground node of LNS pin lower resistor

The recommendation of ground connection is shown in Fig36. The ground traces marked in red should be as short and wide as possible.

FBB, LNS, CS, ISEN, VSEN sensing resistor should be close to IC

For all the input sensing pins, the sensing resistors should be close to IC to minimize disturbance by capacitive coupling.

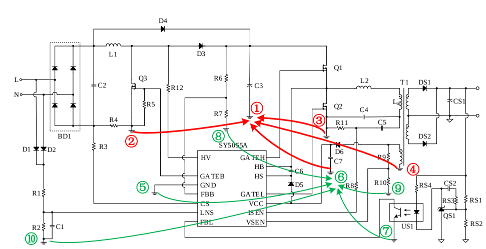
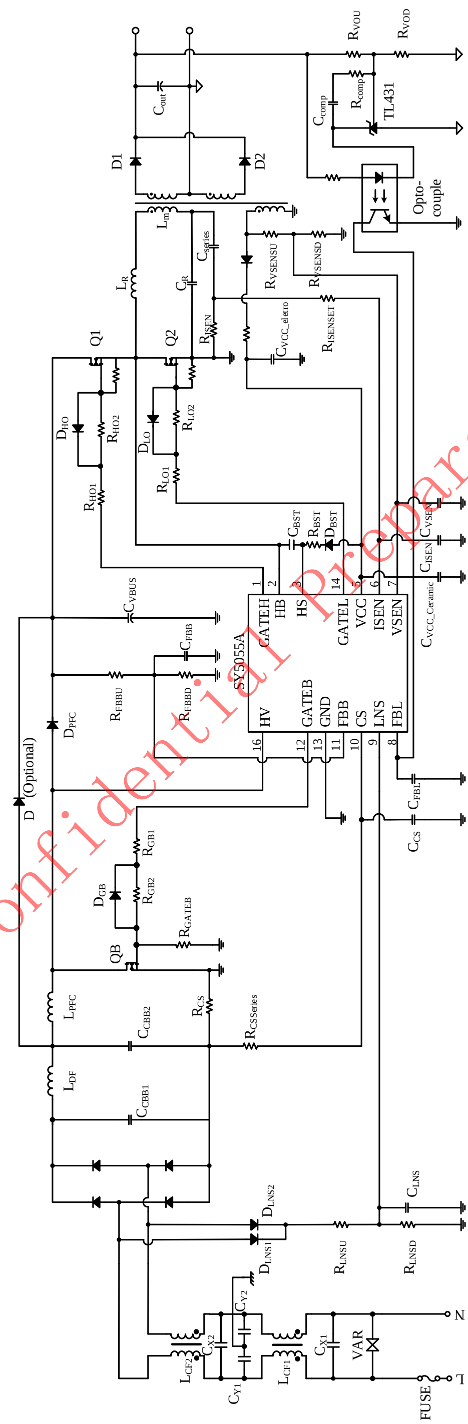
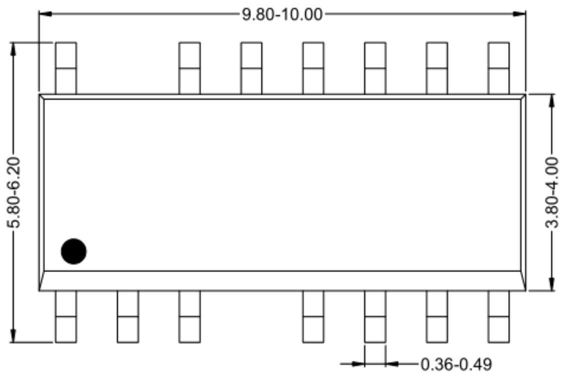


Fig36 Recommendation of Ground Connection

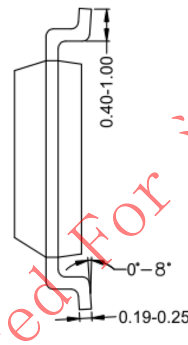
Application Circuit



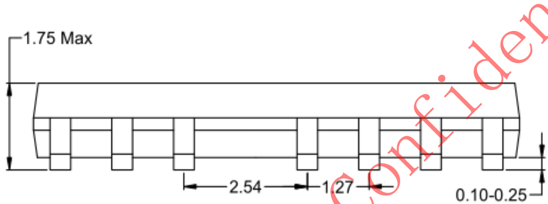
SOP14 Package Outline Drawing & PCB Layout



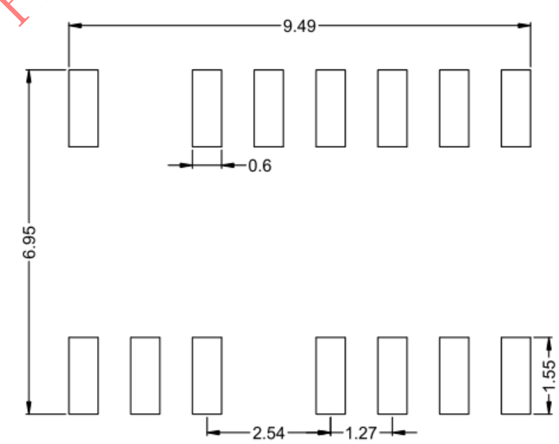
Top view



Side view



Front view



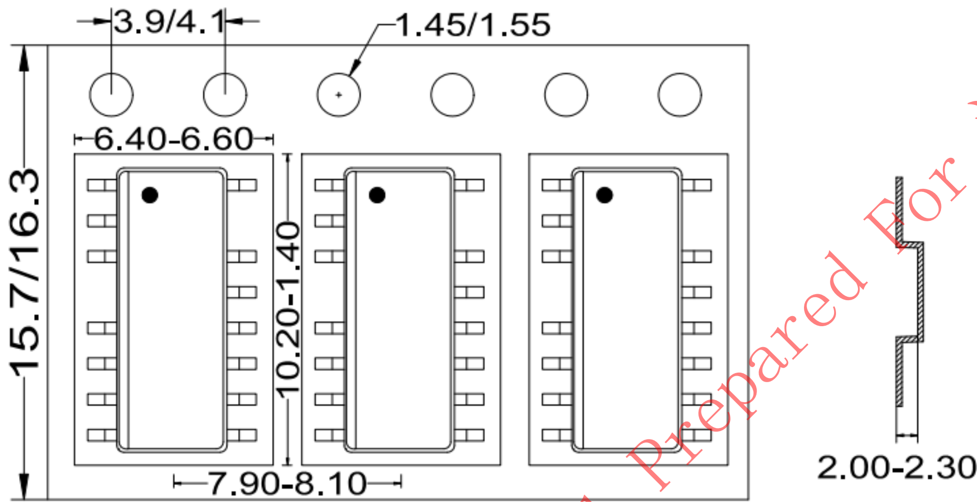
PCB layout (Recommended)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

Taping & Reel Specification

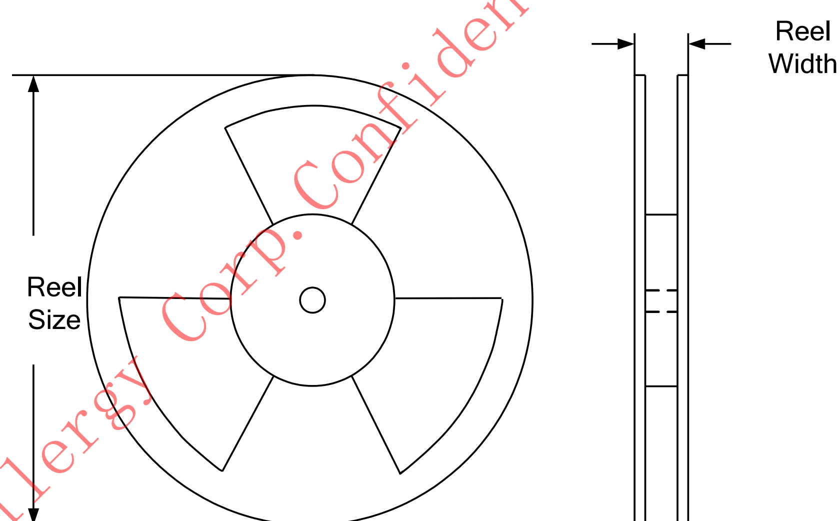
1. Taping orientation

SOP14



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SOP14	16	8	13"	400	400	2500

3. Others: NA

Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
August 18, 2023	Revision 0.9	Initial Release

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