Application Note: SY50583

Buck Regulator
with CC/CV control

General Description

The SY50583 is a PWM controller with several features to enhance performance of Buck converters. It integrates a MOSFET with 700V breakdown voltage to decrease physical volume. Both current and voltage regulation are achieved by the controller. It drives the Buck converter in the quasi-resonant mode to achieve higher efficiency and better EMI performance.

Ordering Information

SY50583□(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY50583FAC	SO8	----

Features

- Integrated 700V MOSFET
- CC/CV control eliminates Aux-winding
- Quasi-Resonant (QR) mode to achieve low switching losses
- Low start up current: 15µA typical
- Maximum frequency limit: 45kHz
- Compact package: SO8

Applications

- Power supply for small appliance

Recommended operating output power @V_{OUT}=12V	
Products	90~264Vac
SY50583	4.2W

Typical Applications

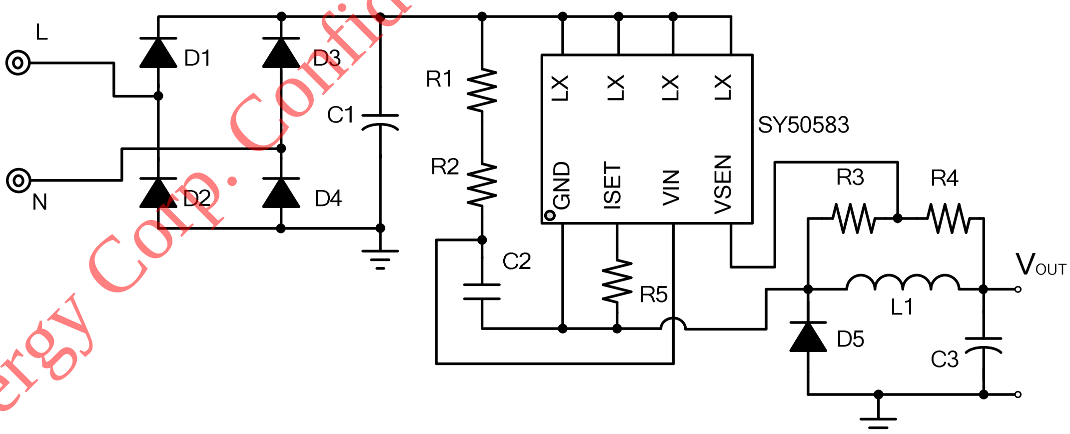
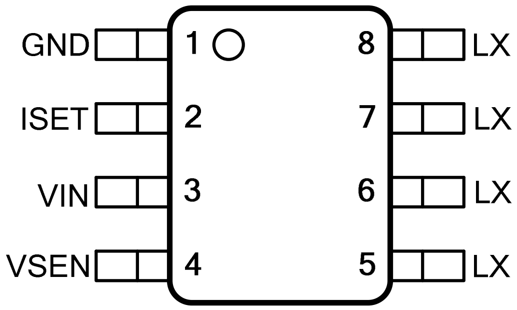


Figure 1. Schematic Diagram

Pinout (top view)



(SO8)

Top Mark: ASE*xyz* (device code: ASE, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin number	Pin Description
GND	1	Ground Pin.
ISET	2	Current set pin. Connect a resistor to program the output limit current.
VIN	3	Power supply pin.
VSEN	4	Voltage sense pin. Connect to a resistor divider of inductor or auxiliary winding to sense output voltage.
LX	5,6,7,8	Internal HV MOSFET drain pin.

Block Diagram

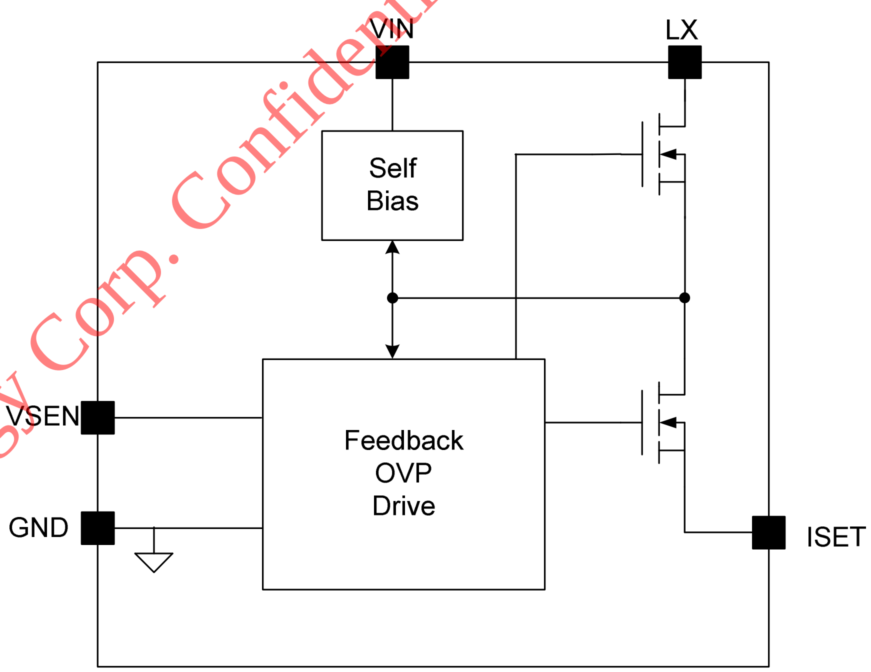


Figure2. Block Diagram

Absolute Maximum Ratings (Note 1)

ISET -- -0.3V~3.6V
VIN, VSEN -- -0.3V~17V
I_{VIN}--10mA
I_{LX}--1.4A
LX--700V
Power Dissipation, @ TA = 25°C SO8--1.1W
Package Thermal Resistance (Note 2)
SO8, θ_{JA}--125°C/W
SO8, θ_{JC}--60°C/W
Junction Temperature Range -- -45°C to 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range -- -65°C to 150°C

Recommended Operating Conditions

VIN -- 9V~16V
Junction Temperature Range -- -40°C to 125°C

Electrical Characteristics

(V_{VIN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN turn-on threshold	V_{VIN_ON}		13.5	14.6	16	V
VIN turn-off threshold	V_{VIN_OFF}		6.3	7	7.8	V
Start up current	I_{ST}			15	18	μA
VSEN Pin Section						
VSEN pin over voltage	V_{VSEN_OVP}			V_{VSEN_REF} ×1.03		V
VSEN pin reference voltage	V_{VSEN_REF}		1.215	1.25	1.285	V
Driver Section						
Min ON Time	T_{ON_MIN}			300		ns
Max ON Time	T_{ON_MAX}			25		μs
Min OFF Time	T_{OFF_MIN}			1.8		μs
Max OFF Time	T_{OFF_MAX}			150		μs
Minimum switching period	T_{PERIOD_MIN}			22		μs
ISET Pin Section						
Current reference	V_{REF}		620	675	710	mV
Integrated MOSFET Section						
BV of HV MOSFET	V_{BV}	V_{GS}=0V,I_{DS}=250μA	700			V
Static Drain-Source On-Resistance	R_{DSON}	V_{GS}=12V,I_{DS}=0.1A		7	8.5	Ω
Thermal Section						
Thermal Shutdown Temperature	T_{SD}			150		C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal via to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

Operation

The SY50583 is a high performance controller with constant current and constant voltage.

It integrates a 700V MOSFET to decrease physical volume.

In order to reduce the switching losses and improve EMI performance, Quasi-Resonant switching mode is applied, which means to turn on the power MOSFET at valley of drain voltage; the start up current of SY50583 is rather small (15μA typically) to reduce the standby power loss further; the maximum switching frequency is clamped to 45kHz to reduce switching losses and improve EMI performance when the converter is operated at light load condition.

SY50583 provides reliable protections such as Short Circuit Protection (SCP), Over Voltage Protection (OVP), Over Temperature Protection (OTP), etc.

SY50583 is available with SO8 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} across VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to V_{VIN_ON}, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the Buck inductor could supply enough energy to maintain V_{VIN} above V_{VIN_OFF}.

The whole start up procedure is divided into two sections shown in Fig.3. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage built-up section. The start up time t_{ST} composes of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.

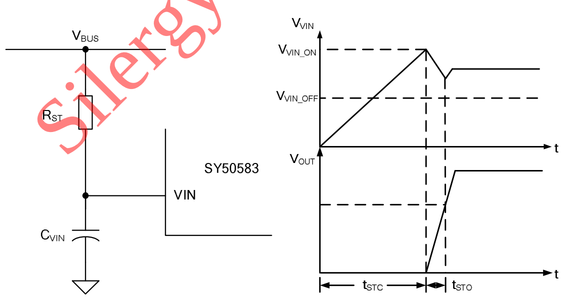


Fig.3 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage.

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(c) If R_{ST} and C_{VIN} are chosen to a very small start up time, SCP and OVP power loss will be large. Then C_{VIN} and R_{ST} time constant should be increased.

Proprietary self-bias technique allows C_{VIN} to be charged every switching cycle. There is no need to add auxiliary winding for power supply. C_{VIN} can be chosen with small value and small package to save cost

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When power supply for IC is not enough, V_{VIN} will drop down. Once V_{VIN} is below V_{VIN_OFF}, the IC will stop working.

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for Buck converter.

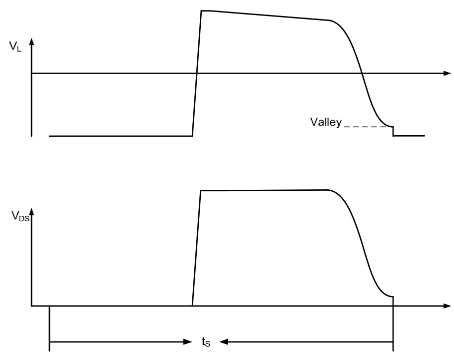


Fig.4 QR mode operation

VSEN pin detects the inductor voltage by a resistor divider. When the voltage across drain and source of the integrated MOSFET is at voltage valley, the MOSFET would be turned on.

Output Voltage Control

In order to achieve constant voltage control. The output voltage is sampled by detecting the inductor voltage.

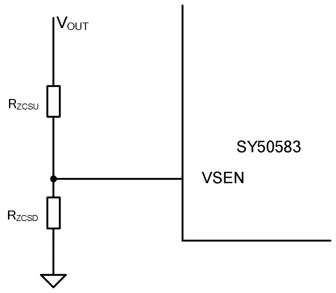


Fig.5 VSEN pin connection

As shown in Fig.6, during OFF time, the voltage across the inductor is

$V_L = V_{OUT} + V_{D\_F}$ (3)

V_{D_F} is the forward voltage of the power diode; V_L is the voltage across the inductor.

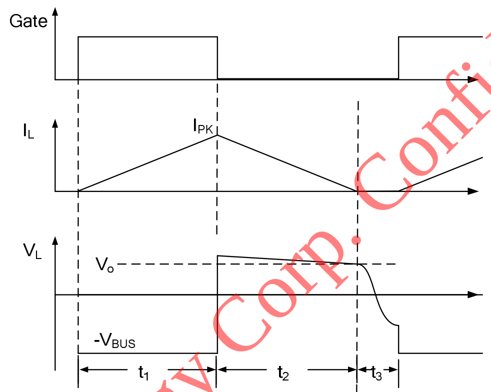


Fig.6 inductor voltage waveforms

At the current zero-crossing point, V_{D_F} is nearly zero, so V_{OUT} is proportional with V_L exactly. The voltage of this point is sampled by the IC as the feedback of output voltage. The resistor divider is designed by.

$$\frac{V_{VSEN\_REF}}{V_{OUT}} = \frac{R_{VSEND}}{R_{VSENU} + R_{VSEND}} \quad (4)$$

Where V_{VSEN_REF} is the internal voltage reference.

Constant-current control

The switching waveforms are shown in Fig.7. The output limit current I_{OUT_LIM} can be represented by,

$$I_{OUT\_LIM} = \frac{I_{PK}}{2} \times \frac{t_{EFF}}{t_S} \quad (5)$$

Where I_{PK} is the peak current of the inductor; t_{EFF} is the effective time of inductor current rising and falling; t_S is the switching period.

I_{PK} and t_{EFF} can be detected by ISET and VSEN pin, which is shown in Fig.7. These signals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.

$$V_{REF} = I_{PK} \times R_{ISET} \times K \times \frac{t_{EFF}}{t_S} \quad (6)$$

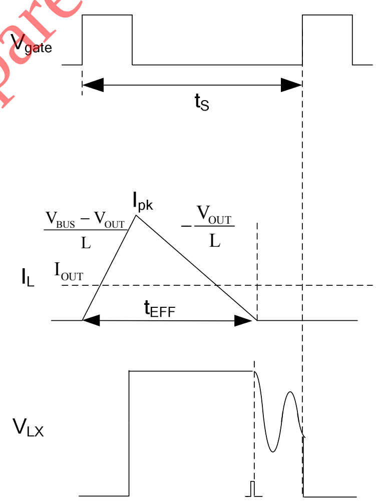


Fig.7 switching waveforms

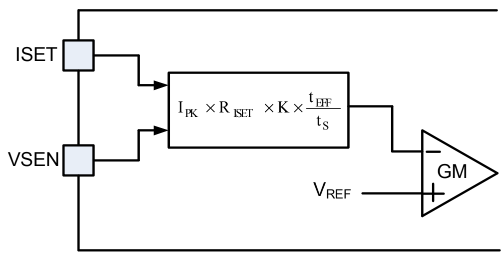


Fig.8 Output current detection diagram

Finally, the output limit current I_{OUT_LIM} can represented by

$$I_{OUT\_LIM}=\frac{V_{REF}}{2R_{ISET}} \quad (7)$$

Where V_{REF} is the internal reference voltage; R_{ISET} is the current set resistor. I_{OUT_LIM} can be programmed by R_{ISET}.

$$R_{ISET}=\frac{V_{REF}}{2I_{OUT\_LIM}} \quad (8)$$

When over current operation or short circuit operation happens, the output current will be limited at I_{OUT_LIM}. The V-I curve is shown as Fig.9.

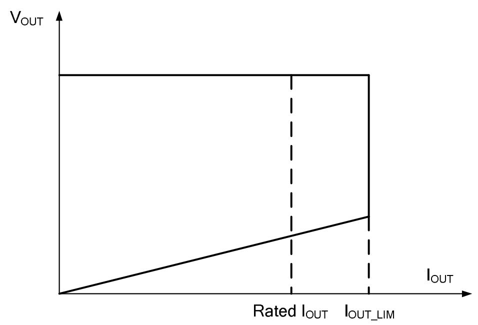


Fig.9 V-I curve

Line regulation modification

The IC provides line regulation modification function to improve line regulation performance.

Due to the sample delay of ISET pin and other internal delay, the output current increases with increasing input BUS line voltage. A small compensation voltage ΔV_{ISET_C} is added to ISET pin during ON time to improve such performance. This ΔV_{ISET_C} is adjusted by the upper resistor of the divider connected to VSEN pin.

$$\Delta V_{ISET\_C}=(V_{BUS}-V_{OUT})\times\frac{k_1}{R_{VSENU}}\times R_{ISET} \quad (8)$$

Where R_{VSENU} is the upper resistor of the divider; k_1 is an internal constant as the modification coefficient.

The compensation is mainly related with R_{VSENU}, larger compensation is achieved with smaller R_{VSENU}.

Short Circuit Protection (SCP)

When the output is shorted, demagnetizing voltage of inductor is zero, so T_{OFF} will be clamped at T_{OFF_MAX}, when T_{OFF_MAX} shows up for 64 times, SCP is triggered and the IC will discharge V_{VIN} by an internal current source I_{VIN_SCP}. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by BUS voltage through start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

Power design

A few applications are shown as below.

Input range	Output	
90Vac~264Vac	4.2W	12V/0.35A

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of the integrated MOSFET and output power diode is maximized;

$$V_{MOS\_DS\_MAX}=\sqrt{2}V_{AC\_MAX} \quad (9)$$

$$V_{D\_R\_MAX}=\sqrt{2}V_{AC\_MAX} \quad (10)$$

Where V_{AC_MAX} is maximum input AC RMS voltage. When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

Inductor (L)

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 shown in Fig.11.

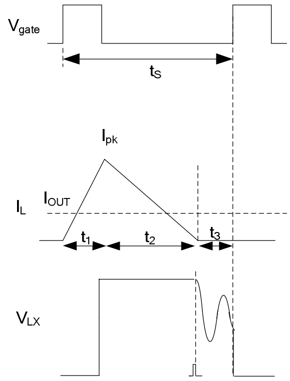


Fig.11 switching waveforms

When the operation condition is with minimum input AC RMS voltage and full load, the switching frequency is minimum frequency, the maximum peak current through integrated MOSFET and the transformer happens.

Once the minimum frequency f_{S_MIN} is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Preset minimum frequency f_{S_MIN}

(b) Compute relative t_S, t_1

$$t_S = \frac{1}{f_{S\_MIN}} \quad (11)$$

$$t_1 = \frac{t_2 \times (V_{OUT} + V_{D\_F})}{(\sqrt{2} \times V_{AC\_MIN} - V_{OUT})} \quad (12)$$

$$t_2 = t_S - t_1 \quad (13)$$

Where V_{D_F} is the forward voltage of the diode

(c) Compute maximum peak current $I_{L\_PK\_MAX}$ and inductor L.

$$I_{L\_PK\_MAX} = \frac{2 \times V_{OUT} \times I_{OUT}}{\sqrt{2} \times V_{AC\_MIN} \times \frac{t_1}{t_s} \times \eta} \quad (14)$$

$$L = \frac{(\sqrt{2} V_{AC\_MIN} - V_{OUT}) \times t_1}{I_{L\_PK\_MAX}} \quad (15)$$

(f) Compute RMS current of the inductor

$$I_{L\_RMS\_MAX} = \frac{I_{L\_PK\_MAX}}{\sqrt{3}} \quad (16)$$

(g) Compute RMS current of the MOSFET

$$I_{MOS\_RMS\_MAX} = I_{L\_PK\_MAX} \times \sqrt{\frac{t_1}{3t_S}} \quad (17)$$

inductor design (N)

the parameters below are necessary:

Necessary parameters	
Inductance	L
inductor maximum current	$I_{L\_PK\_MAX}$
inductor maximum RMS current	$I_{L\_RMS\_MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute inductor turn N

$$N = \frac{L \times I_{L\_PK\_MAX}}{\Delta B \times A_e} \quad (18)$$

(d) Select an appropriate wire diameter

With $I_{L\_RMS\_MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(e) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Input capacitor C_{BUS}

Generally, the input capacitor C_{BUS} is selected by
$C_{BUS} = 4\mu F / W$ (half bridge rectifier), or
$C_{BUS} = 2\mu F / W$ (full bridge rectifier)

Or more accurately by(full bridge rectifier)

$$C_{BUS} = \frac{\arcsin(1 - \frac{\Delta V_{BUS}}{\sqrt{2} V_{AC\_MIN}}) + \frac{\pi}{2}}{\pi} \times \frac{P_{OUT}}{\eta} \times \frac{1}{2 f_{IN} V_{AC\_MIN}^2 [1 - (1 - \frac{\Delta V_{BUS}}{\sqrt{2} V_{AC\_MIN}})^2]} \quad (19)$$

Where ΔV_{BUS} is the voltage ripple of BUS line.

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

(b) The circuit loop of all switching circuit should be kept small.

(c) bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(d) Loop of 'Source pin – current sample resistor – GND pin' should be kept as small as possible.

(e) The resistor divider connected to VSEN pin is recommended to be put beside the IC.

(f) The control circuit is recommended to be put outside the power circuit loop.

Design Example

A design example of typical application is shown below step by step.

#1. Identify Design Specification

Design Specification			
V_{AC_MIN}	90V	V_{AC_MAX}	264V
V_{OUT}	12V	I_{OUT}	0.35A
P_{OUT}	4.2W	η	78%
f_{IN_MIN}	35KHz		

#2. Compute relative t_S, t_1

$$t_S = \frac{1}{f_{S\_MIN}} = \frac{1}{35k} = 28.57\mu s$$

$$t_1 = \frac{(t_s - t_1)\times(V_{OUT}+V_{DF})}{\sqrt{2}\times V_{AC\_MIN}\text{-}V_{OUT}} = \frac{(28.57uS\text{-}t_1)\times 13V}{115V} = 2.9\mu s$$

#3. Compute maximum peak current $I_{L\_PK\_MAX}$ and inductor L

$$I_{L\_PK\_MAX} = \frac{2\times V_{OUT}\times I_{OUT}}{\sqrt{2}\times V_{AC\_MIN}\times\frac{t_1}{t_s}\times\eta} = \frac{2\times 12V\times 0.35A}{\sqrt{2}\times 90V\times\frac{2.9u}{28.57u}\times 0.78} = 0.84A$$

$$L = \frac{(\sqrt{2}\times V_{AC\_MIN}\text{-}V_{OUT})\times t_1}{I_{L\_PK\_MAX}} = \frac{115V\times 2.9uS}{0.84A} = 397u$$

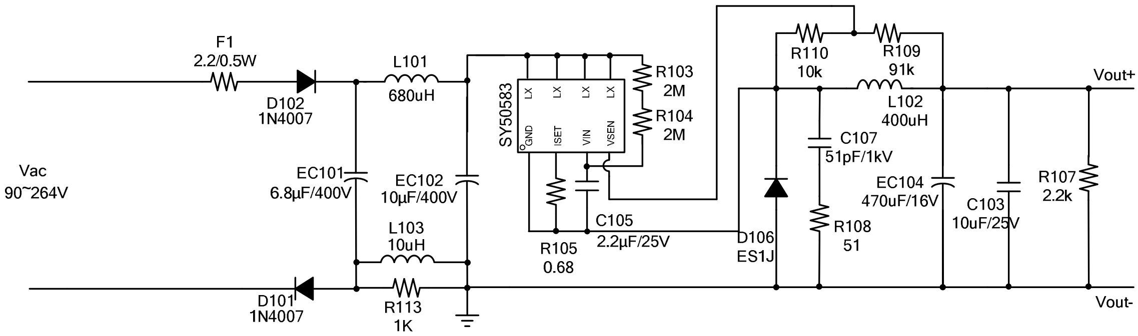
Set L =400uH

#4. Compute Input capacitor

Generally, the input capacitor C_{BUS} is selected by
C_{BUS} = 4μF / W (half bridge rectifier), or
C_{BUS} = 2μF / W (full bridge rectifier).

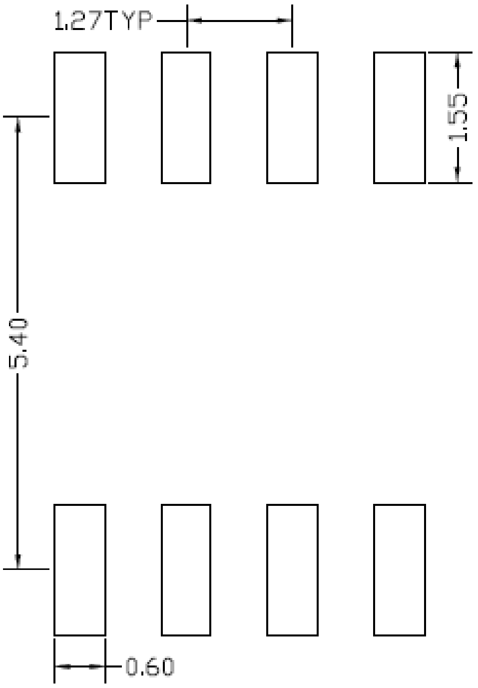
Then C_{BUS}=4×4.2W=16.8uF

Circuit schematic

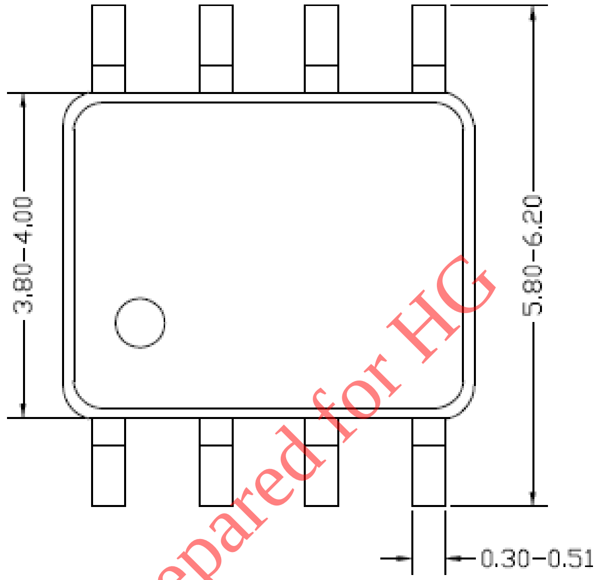


Example for 12V/0.35A

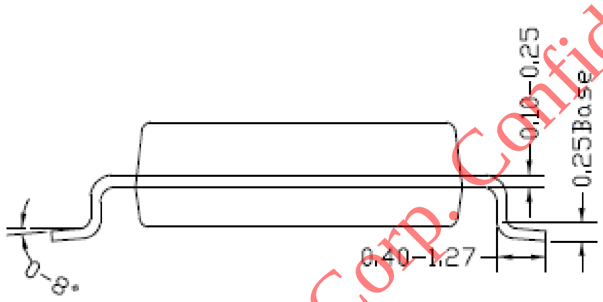
SO8 Package Outline & PCB Layout Design



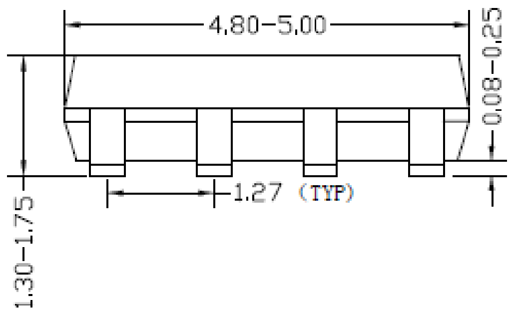
Recommended Pad Layout
(Reference only)



Top view



Side view



Front view

Notes: All dimension in millimeter and exclude mold flash & metal burr.