General Description

SY5238 is a Flyback SR controller compatible with QR IC to achieve ZVS operation. The primary side PWM IC must work in quasi resonant mode. SY5238 adopts proprietary operation mode to achieve flyback ZVS turn on, which greatly improves Flyback efficiency and power density. SY5238 also adopts adaptive gate voltage control for safe operation.

Ordering Information

SY5238 □(□□□)

Package Code
Optional Spec Code

Ordering Number	Package type	Note
SY5238DGD	DFN2*3-8	----

Features

• Proprietary Operation Mode for Flyback ZVS
• High Efficiency, High Power Density
• Adaptive Gate Voltage Control
• Slope Detection to Prevent SR False Trigger
• 130V DSEN Pin to Directly Sense DRAIN Voltage of SR MOS
• Power Saving Mode to Improve Light Load Efficiency
• Dual Channel Supply for Applications with very Low Output Voltage

Applications

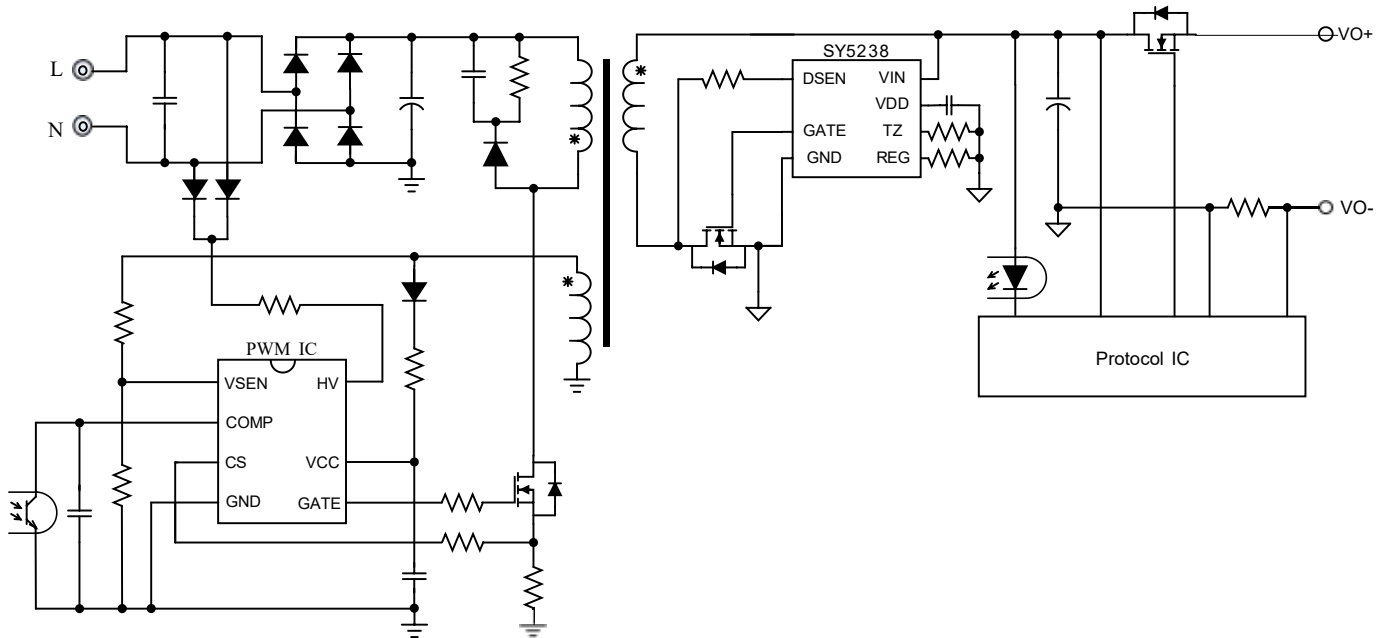• USB PD, Fast Charger
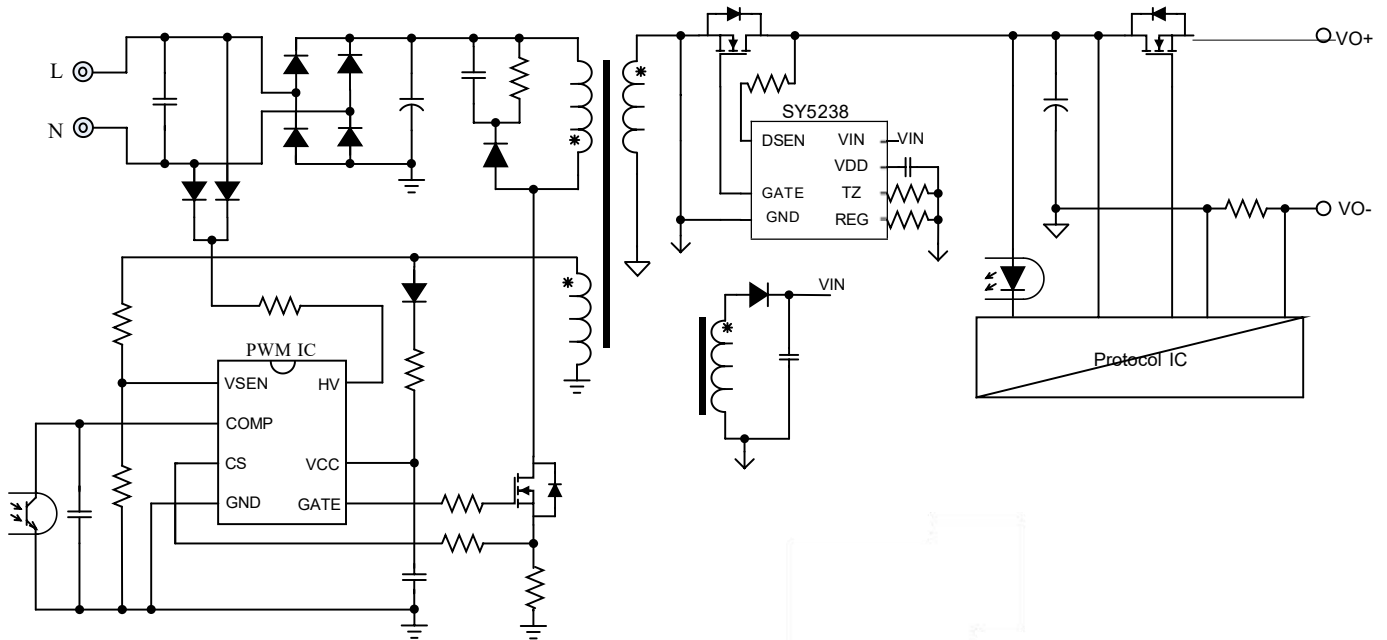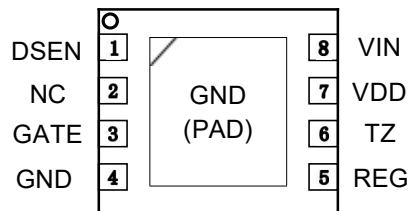• Adaptor

Typical Applications

Figure 1. (a) Low side

Figure 1. (b) High side

Pinout (top view)

(DFN2*3-8)
Top Mark: W7 *xyz* (**device code: W7,** *x=year code, y=week code, z= lot number code*)

Pin number	Pin Name	Pin Description
1	DSEN	drain sense input
2	NC	Not connected
3	GATE	Gate drive pin
4	GND	Ground pin
5	REG	Turn on slope threshold set for SR operation
6	TZ	Connect a resistor to program ZVS coefficient.
7	VDD	Power supply pin
8	VIN	Low voltage power supply input
9	GND	Ground pin

Absolute Maximum Ratings (Note1)

DSEN --- 0.3V ~ 130V
VIN -- 0.3V ~ 30V
VDD --- 0.3V ~ 20V
GATE -- -0.3V ~ VDD+0.3V
TZ, REG --- 0.3V ~ 4V
Power Dissipation, @ T_A = 25°C DFN2x3 --- 1W
Package Thermal Resistance (Note 2)
      DFN2x3, θ_{JA} -- 46°C/W
      DFN2x3, θ_{JC}-- 28°C/W
Maximum Junction Temperature --- 150°C
Lead Temperature (Soldering, 10 sec.) -- 260°C
Storage Temperature Range --- -65°C to 150°C

Electrical Characteristics

(V_{IN} = 12V (Note 3), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDD Pin						
VDD ON Threshold	V_{DD_ON}			3		V
UVLO Hysteresis	V_{DD_HYS}			160		mV
VDD Regulation Voltage when VIN Pin is Active to Supply IC	$V_{DD\_REG\_VIN}$			9		V
VDD Regulation Voltage when DSEN Pin is Active to Supply IC	$V_{DD\_REG\_DSEN}$	V_{DSEN}=100V		5		V
Operating Current	I_{DD_OP}	V_{DD}=9V, C_{GATE}=2.2nF,		4.9		mA
		V_{SDWD}=250V,C_{GATE}=2.2nF, Fsw=200kHz		3.1		mA
Quiescent Current	I_{DD_STBY}	Under Standby Mode		160		uA
VIN Pin						
Threshold of Switching to VIN Supply Channel	V_{IN_INSPY}	V_{IN} is rising		4.8		V
Threshold of Switching to DSEN Supply Channel	$V_{IN\_DSENSPY}$	V_{IN} is falling		4.7		V
REG Pin						
Resistor to Program Drain Falling Slope to enable SR	R_{REG}	R_{REG}=50k		80		ns
		R_{REG}=300k		155		ns
TZ Pin						
ZVS Time Program Coefficient	k_{TZ}			4.5		10^{-9}
Operating Voltage Range						
DSEN Pin	V_{DSEN_OP}				110	V
SR Turn on Threshold	V_{DS_ON}			- 100		mV
V_{DSEN} Regulation Voltage	V_{DS_REG}			-35		mV
SR Turn off Threshold	V_{OFF_TH}			10		mV
Time Threshold to Trigger Sleep Mode	T_{TH_SLP}			70		us

GATE pin

Max. Source Current	I_{SOURCE_MAX}	C_{LOAD}=2.2nF,Vgs from 1V to 6V	0.5			A
Max. Sink Current	I_{SINK_MAX}	C_{LOAD}=2.2nF,Vgs from 6V to 1V	1.3			A
SR Minimum ON Time	T_{ON_MIN}			600		ns
SR Minimum OFF Time	T_{OFF_MIN}			600		ns
Turn on Delay	T_{DELAY_ON}	C_{GATE}=2.2nF		20		ns
Turn off Delay	T_{DELAY_OFF}	C_{GATE}=2.2nF		20		ns

OTP

Thermal Shutdown Temperature	T_{SD}			150		°C
Hysteresis to Resume Operating	T_{OTP_HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause perm anent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: $θ_{JA}$ is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Operation Principles

Introduction

The SY5238 is a Flyback SR with proprietary operation mode to achieve flyback ZVS. It supports primary side PWM IC with QR mode, and the maximum valley numbers to turn on must >6. To ensure safety operation, SR control includes turn on/off control, Vds regulation, slope program, etc. The ZVS control logic helps primary side FET turning on at ~0V to reducing switching losses to maximize system efficiency and achieve high power density.
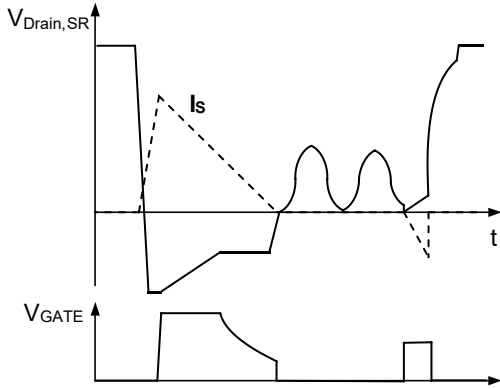

Fig. 1 SR operation diagram

SR Turn On

Traditional method is to set a SR MOSFET turn on threshold V_{ON_TH}, when DSEN voltage is falling and down to V_{ON_TH}, then turn on SR MOSFET after a short delay as shown. However, under DCM or QR operating mode, after secondary current decrease to ZERO, a resonant waveform will appear. Sometimes, the amplitude of this resonant waveform can be large enough, which will cause DSEN voltage drops below turn on threshold V_{ON_TH}, SR MOSFET may be falsely turned on by parasitic resonant.

To solve the above issue, V_{DSEN} falling slope rate is detected. When primary MOSFET is turned off, V_{DSEN} falling slope rate is very high, SR will turn on; while during resonant phase, V_{DSEN} falling slope rate is relatively low, SR will not turn on.

SY5238 use resistor divide circuit to sense the DSEN voltage, the V_{PVS} is 0.02 times of V_{DSEN}. It set 2 thresholds to indirectly sense V_{PVS} falling slope rate, the V_{PVS} is the time duration ($\triangle t$) when V_{PVS} is falling between high-level threshold V_{PVS_HTH} and low-level

threshold V_{DSEN_LTH} (0mV) is measured, and the falling time duration ($\triangle t$) will be compared with a falling slope ref time threshold T_{REF} .

To prevent external noise (for example: ESD noise) false turn on SR MOSFET by making fast V_{DSEN} falling slope rate, the DSEN blanking time is adopt. V_{PVS} is the resistor divide voltage of V_{DSEN}. If V_{PVS} is above V_{PVS_HTH} and lasting for T_{PVS_BLK} (200nS) and falling slope time $\triangle t < T_{REF}$, IC considers this action as primary MOSFET turn off event and then turn on SR MOSFET after a short delay. Otherwise, IC will not turn on SR MOSFET.
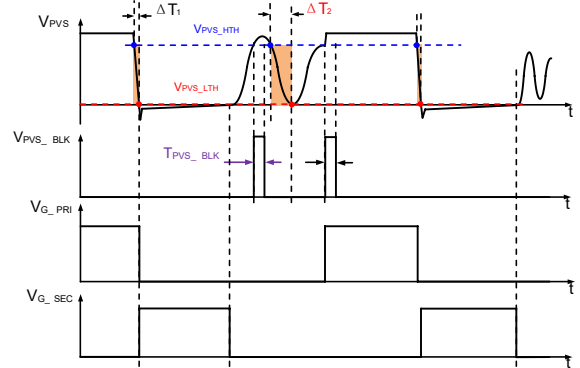

Fig. 2 Time diagram of SR enable strategy

V_{PVS_HTH} is a dynamically adjusted value, it is 0.85 times of DSEN high-level voltage value. The falling slope ref time threshold T_{REF} is controlled by REG resistor as below.

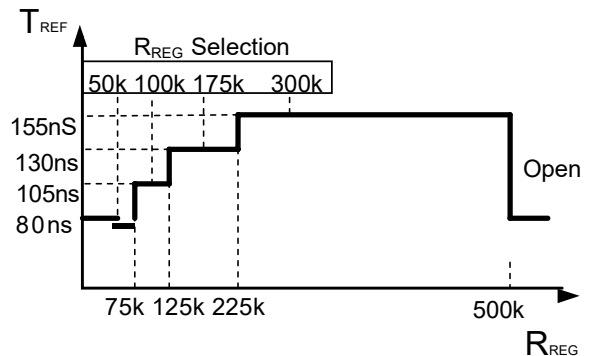| T_{REF} setting has 4 steps:		
Step	T_{REF}	R_{REG} (kΩ)
1	80ns	50
2	105ns	100
3	130ns	175
4	155ns	300

Fig. 3 Programmable curve of falling slope ref

SR Gate Control

After primary side FET turn off, the inductor current freewheels in SR, the current decreases linearly. When V_{DS} drops to V_{DS_REG}(-35mV), the closed loop V_{DS} regulation circuit will gradually decrease V_{GATE} to maintain the V_{DS} above V_{DS_REG}. As SR current becomes smaller, V_{GATE} drops near the SR MOSFET turn off threshold, $I_D * R_{DSON}$ cannot be regulated to V_{DS_REG} anymore, V_{DS} will increase higher than V_{DS_REG}. If V_{DS} rises and cross V_{OFF_TH}, after a short delay time T_{OFF_DLY}, GATE voltage will be pulled down to 0V by a large sink current to turn off SR MOSFET.
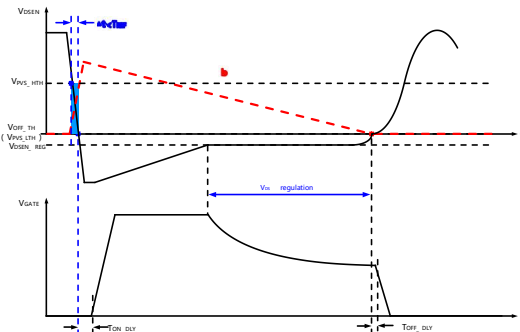
Fig. 4 SR gate control diagram

Min ON time& min OFF time
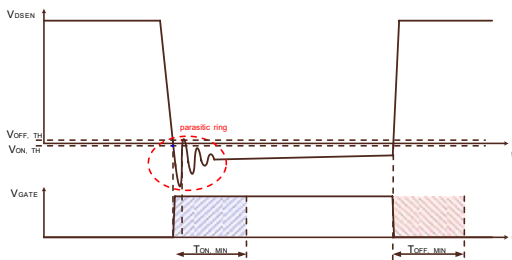
internal logic circuit false action, a blanking time T_{OFF_MIN} is also applied. During T_{OFF_MIN}, the SR logic can't begin a new switching cycle and the normal gate drive not allowed turning on.

ZVS Operation

The key function of SY5238 is achieving primary MOS ZVS turn on for high efficiency and high power density. SY5238 is compatible with primary side QR IC to achieve this function.

SY5238 adopts proprietary drive method to increase resonation magnitude of switching node, which pulls $V_{Drain, P}$ to approximately $\sim 50\,V$ to achieve primary side MOSFET ZVS turns on. The ZVS PWM only active in QR mode within 6 valleys, beyond this range, the ZVS is disabled.
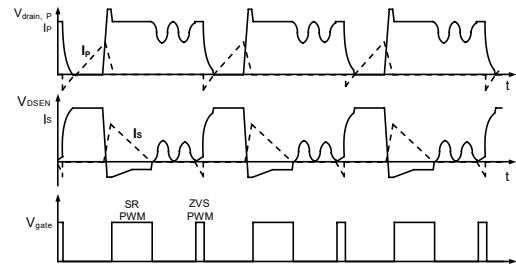
Fig. 6 ZVS control diagram

ZVS coefficient R_TZ setting

The ZVS performance is affected by transformer's magnetizing inductance (Lm) and the total equivalent capacitance (Csw) of switching node. To tune the best operation efficiency, the resistor value of TZ pin to GND can be adjusted. The resistor set ZVS PWM turn on time coefficient; it is chose as follows.

$$R_{TZ} = \frac{\sqrt{C_{SW} \times L_m}}{4.5 \times 10^{-9}} \text{ (k}\Omega)$$

method 1, calculate coefficient base on magnetizing inductance and equivalent switching node capacitance capacitor.

T_{DCM}:DCM resonance period time
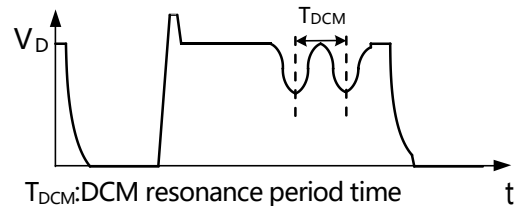
$$R_{TZ} = \frac{T_{DCM}}{2\pi} \frac{1}{4.5 \times 10^{-9}}(\text{k}\Omega)$$

method 2, calculate coefficient base on DCM resonance period time

The resistor can be adjusted slightly around the calculated value. The resistance range is preferred to be 20kΩ-60kΩ, if it is <10kΩ or >100kΩ range, the ZVS function is disabled.

ZVS enable condition

1. Power supply: when VIN supply is active, ZVS is enabled. When DSEN supply is active, the ZVS is disabled. (DSEN pin supply power loss is much higher, the extra driving loss may be greater than ZVS affect)

2. Input voltage condition: at low line input, the ZVS has little efficiency improvement. So the input voltage range is limited to maximize ZVS effect. Input voltage condition calculation is shown as below with hysteresis:

ZVS enable: $VIN > N(0.333 \cdot V_{OUT} + 26.5V)$
ZVS disable: $VIN < N(0.333 \cdot V_{OUT} + 21.5V)$

ZVS protection

To guarantee ZVS logic working correctly, the maximum ZVS on time is limited to 2.5us, so the primary side IC QR detecting timeout time must be greater than 2.5us+Treso. (Treso is the DCM resonating period).
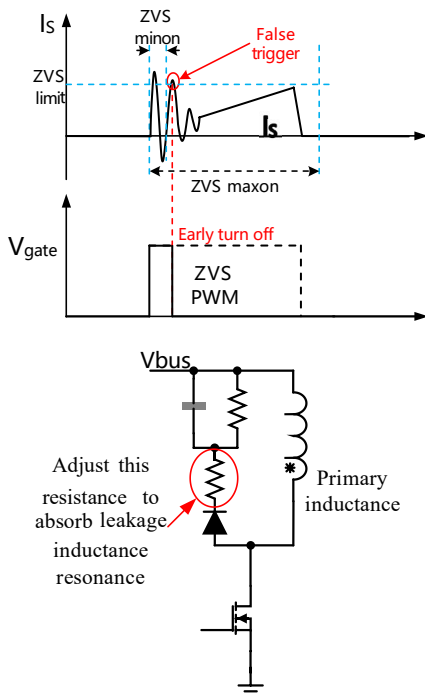
Fig. 7 ZVS limit protection

To prevent ZVS current is to big or primary false turn on, secondary current is limited during ZVS. But primary leakage inductance resonance may trigger ZVS limit, cause ZVS PWM turn off early, add primary inductance resonance absorb resistance is recommend.

ZVS performance adjust
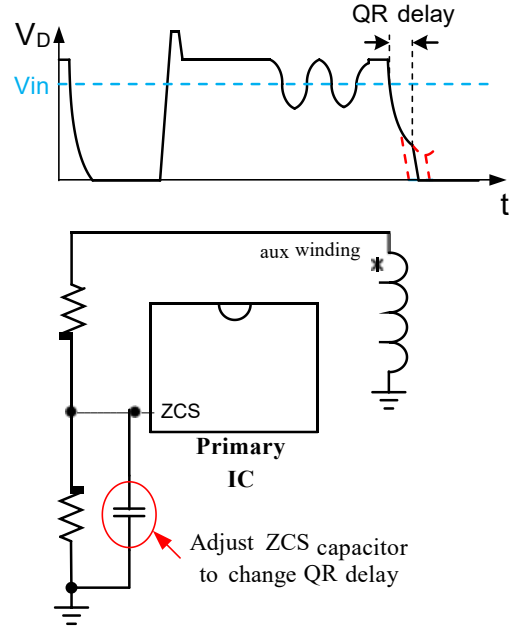
Fig. 8 adjust ZVS performance

To achieve best ZVS performance, primary IC QR delay need slightly adjust. Consider primary IC turn on at DCM resonance valley is the best.

Dual Channel Power Supply

When the output voltage is as low as 3V, which is not high enough to drive the SR MOSFET, the DSEN pin supply is preferred. When the output voltage is high, the power supply efficiency of DSEN pin is lower than VIN pin, the VIN pin supply is preferred.
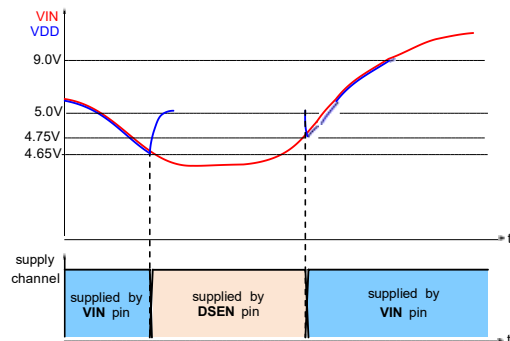

Fig.9 Timing diagram of dual channel supply

SY5238 adopts dual channel power supply. Before VDD voltage reaches ON threshold V_{VDD_ON}, SY5238

is supplied by DSEN pin. As V_{DD} rises and reach ON threshold, VIN pin voltage will be monitored. If VIN voltage is higher than V_{IN_INSPY}, then power supply channel will switch to VIN pin. As VIN increase higher, VDD will follow V_{IN} (with about 0.5V voltage drop), finally VDD will be clamped to 9V. As VIN is decreasing and crossing V_{DSEN_VINSPY}, then the power supply channel will switch to DSEN pin and V_{DD} will be regulated to 5V. Timing diagram is shown inFig.9.

Power Saving Mode

Under light load conditions, SY5238 will enter power saving mode to improve light load efficiency.

During each switching cycle, after SR MOSFET is turned off, a timer will start to count, if the timer has counted to 70us before next SR turn on instant, IC will enter power saving mode, and reduce the power consumption. IC will exit power saving mode by SR MOSFET turn on event.
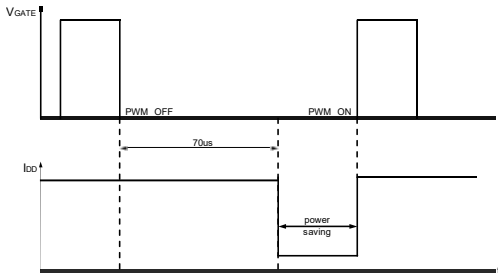
Fig. 10 timing diagram of power saving mode

OTP

IC die temperature is always monitored, if the die temperature rises above 150℃, IC will stop driving SR MOS and keep GATE voltage to 0V. When temperature drops below 130℃, IC die will resume normal operating again.

Application Information
Typical System Implementations
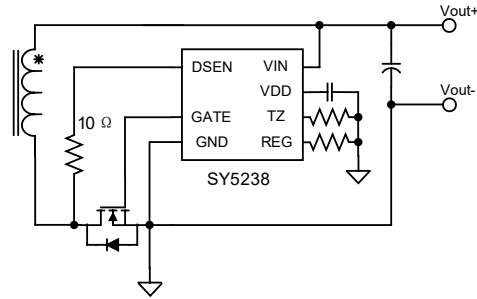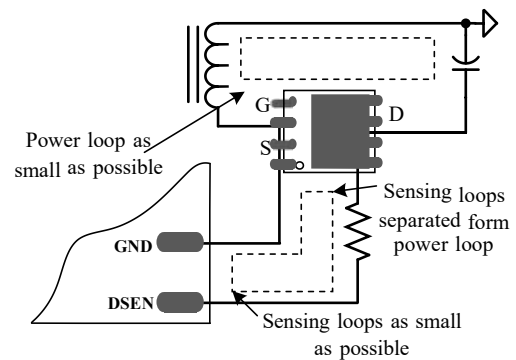

Low side Rectification with Vout supply power
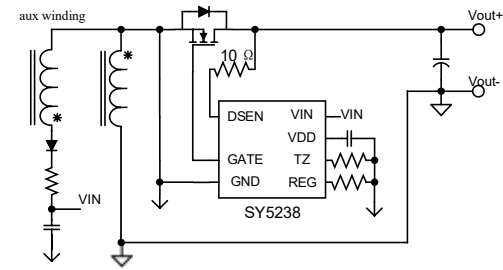
High side Rectification with aux winding supply power

Layout Guideline
Sensing for DSEN/GND

1. Make the sensing connection (DSEN/GND) as close as possible to the MOSFET (drain/source).

2. Keep the IC out of the power loop to prevent the sensing loop and power loop from interrupting each other


(a) To achieve better EMI and Efficiency performance, the output connector should be connected to the output cap first, then to the SR Power pin.

(b) The circuit loop of all switching circuit should be kept small: secondary power loop, secondary RC snubber circuit loop and IC power supply loop.

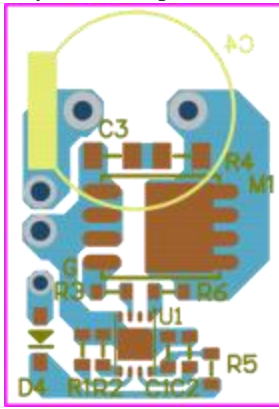The layer close to R$_{REG}$, R$_{TZ}$ loop better connected to IC GND
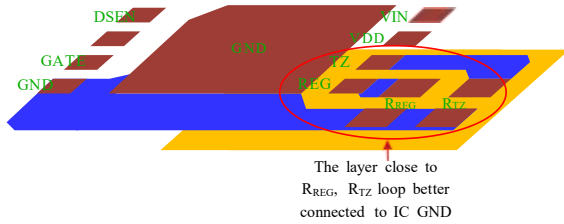
(c) Due to the high resistance on REG and TZ pin, the layout size and length of each loop should be as small as possible. Meanwhile, the layer directly under these two loops better connected to IC GND to shield switching noise.

Layout Example

High side SR layout @bottom view
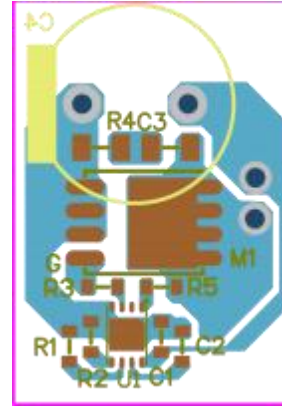

Low side SR layout @bottom view

Design Notice

1. To achieve better EMI performance and reduce secondary rectifier loss, the circuit loop of secondary winding terminal, the output cap and SR MOSFET should be short.
2. GND pin should be connected to Source of SR MOSFET shortly.
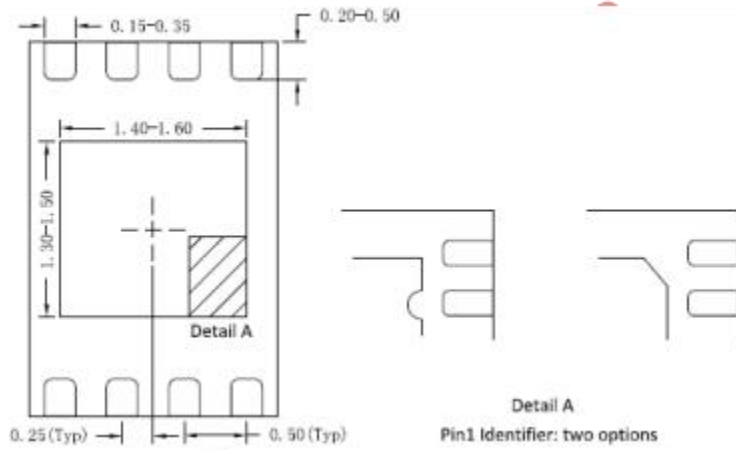3. DSEN pin should be connected to Drain of SR MOSFET shortly.
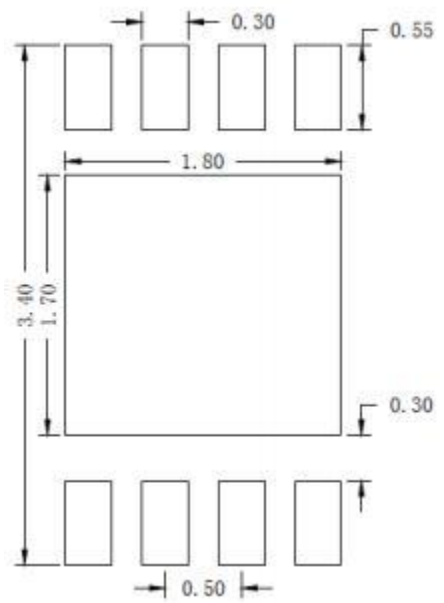
DFN2x3-8 Package Outline
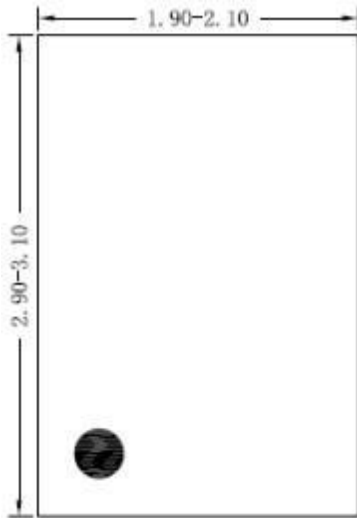
Top View

Side View

Bottom View

Detail A
Pin1 Identifier: two options
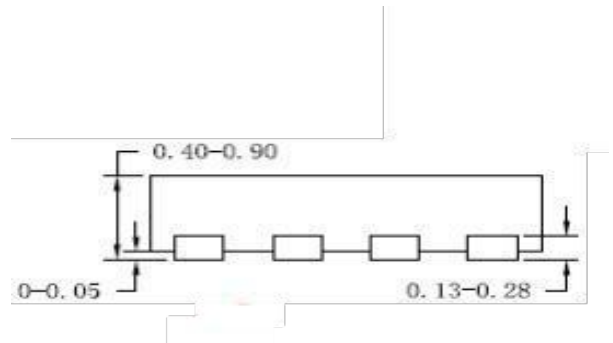
Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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