Applications Note: SY5867

Dimming Interface Converter
Compatible With 0/1~10V Dimming
Resistor Dimming And PWM Dimming

General Description

SY5867 is a dimming interface converter whose input signal can be a 0/1~10V dimming signal, resistor, or PWM signal. It recognizes the signal automatically. The final output of SY5867 is a PWM signal which is used to control a dimmable CC regulator or drive an opto-coupler to achieve isolated dimming. The frequency of output PWM signal and the source current to drive passive 0~10V dimmer/Resistor can be set by external capacitor and resistor.

Ordering Information

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SY5867 □(□□)□
        |  |  └ Temperature Code
        |  └─── Package Code
        └────── Optional Spec Code
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Ordering Number	Package type	Note
SY5867FAC	SO8	----

Features

- Compatible with 0/1~10V Dimming, Resistor Dimming and PWM Dimming.
- Recognize Different Dimming Dignal Automatically.
- Integrate 60V LDO Module to Simplify External Circuit.
- The Source Current for Passive 0/1~10V Dimmer Can Be Set.
- The Frequency of Output Can Be Set.
- Compact Package: SO8

Applications

- LED Lighting

Typical Applications

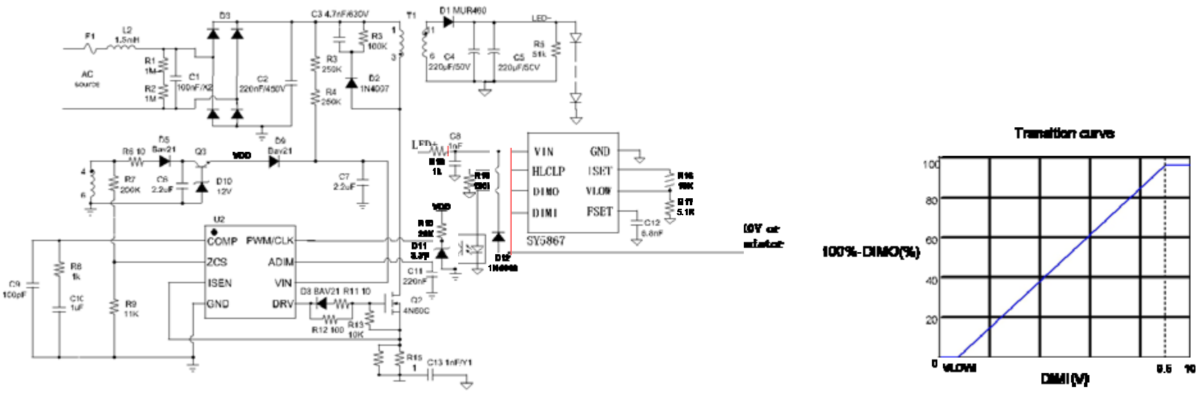


Fig.1 High clamp mode application Schematic

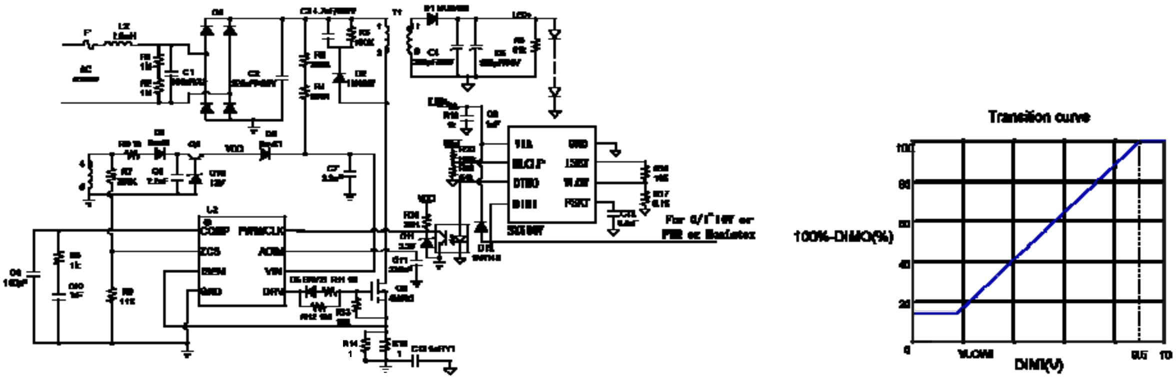
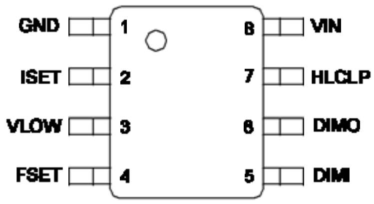


Fig.2 Low clamp mode application Schematic

Pinout (top view)



(SO8)

Top Mark: **BKR*xyz*, (**Device code: BKR; ***x=year code, y=week code, z= lot number code*)**

Pin Name	Pin number	Pin Description
GND	1	Ground pin
ISET	2	Source current setting pin. V_{ISET} is a 1.5V voltage source. This pin is used to set the source current of DIMI pin for passive dimmer or resistor. $I_{DIMI} = \frac{5 \times 1.5}{R_{ISET}}$
VLOW	3	The zero coordinate setting pin. This pin is used to set the lowest input voltage which corresponds to 0% duty. The real minimum 0~10V input is $V_{LOWI} = 1.55 \cdot K1 \cdot V_{LOW} - K1 \cdot 0.926 + 0.2$ $K1 = 1$; (Low clamp mode) $K1 = \frac{14.58}{52.85 + 14.58} \cdot \frac{52.85 + (14.58 // R_{HLCLPD})}{14.58 // R_{HLCLPD}}$; (High clamp mode)
FSET	4	Dimming frequency setting pin. This pin is used o set the frequency of DIMO pin. $F_{DIM} = \frac{30 \cdot 10^{-6}}{(6.6 - V_{LOW}) \cdot C_{FSET}}$
DIMI	5	Dimm ng input pin. Dimming signal is connected to this pin. It maybe is a 0/1~10V analog sig al, resistor or a PWM signal.
DIMO	6	Dimming output pin. This pin will output a PWM signal to driver opto-coupler for separation dimming.
HLCLP	7	High clamp and low clamp mode setting pin. If the voltage of HLCLP pin is larger than 100mV during IC start-up, it enters into low clamp mode, else it works in high clamp mode. In low clamp mode, if V_{DIMI} is less than the setting value, it is clamped internally. $V_{LCLP} = \frac{9.3}{2} \cdot (V_{HLCLP} - 0.2) + 0.2$ In High clamp mode, the clamp voltage is 9.5V fixedly, and the resistor connected to HLCLP is used to adjust the max duty. $D_{MAX} = \frac{67.79 \cdot R_{HLCLPD}}{67.43 \cdot R_{HLCLPD} + 770.59}$ For Example R_{HCLP}=510k ohm $D_{MAX} = \frac{67.79 \cdot 510}{67.43 \cdot 510 + 770.59} = 98.3\%$
VIN	8	Power supply pin. This pin provides power supply for IC.

Block Diagram

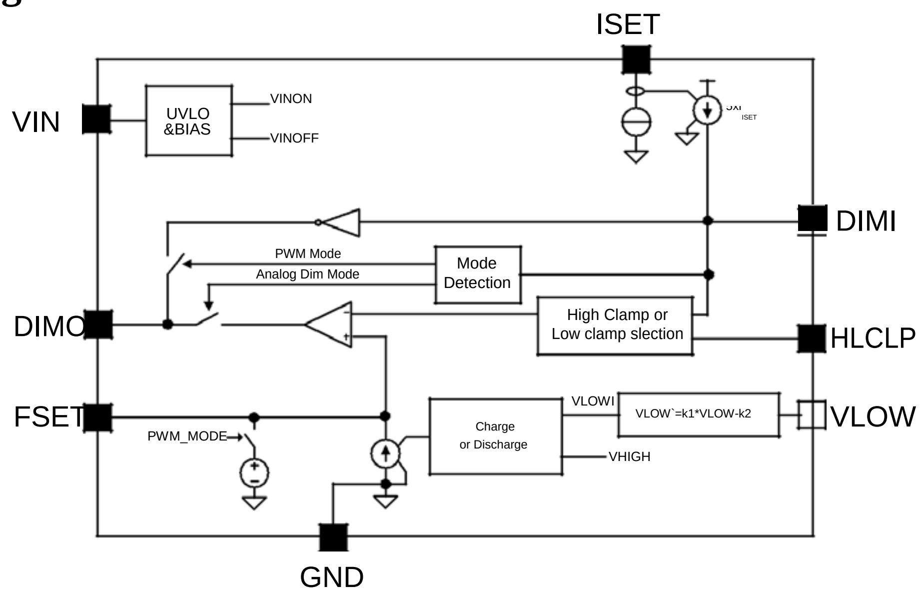


Fig.3 Block Diagram

Absolute Maximum Ratings (Note 1)

VIN	-0.3V~58V
IIN	10mA
ISET, FSET, VLOW	-0.3V~3.6V
DIMI,DIMO	0.3V~20V
Power Dissipation, @ TA = 25°C SO8	0.8W
Package Thermal Resistance (Note 2)	
SO8,θ_{JA}	88°C/W
SO8, θ_{JC}	45°C/W
Maximum Junction Temperature	125°C
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	-65°C to 150°C

Recommended Ope ating Conditions

VIN	$V_{VIN,ON}$~55V
Junction Temperature Range	-40°C to 125°C

Electrical Characteristics

(V_{IN} = 15V, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Voltage Range	V_{VIN}		V_{VIN_ON}		55	V
VIN Turn-on Threshold	V_{VIN_ON}		8.4	9.2	10.2	V
VIN Turn-off Threshold	V_{VIN_OFF}			V_{IN_ON}-1.7		V
VIN Over Voltage Protection	V_{VIN_OVP}		52	55	59	V
DIMI Section						
Range of Minimum Dimming voltage	V_{LOW_Range}		0		V_{ISET}	V
Ref Voltage of ISET	V_{ISET}		1.45	1.5	1.55	V
MAX DIMI Source Current	I_{SR_MAX}	ISET=3.75K	1.85	2.0	2.15	mA
Maximum Dimming Voltage	V_{HIGH}		9.2	9.5	9.8	V
Max Duty of PWM	D_{PWM_MAX}			99(note 3)		%
PWM ON Voltage Threshold	V_{PWM_ON}		2.3			V
PWM OFF Voltage Threshold	V_{PWM_OFF}				0.8	V
PWM Frequency Range	f_{PWM}		400		10k	Hz
Thermal Section						
Thermal Shut Down Temperature	T_{SD}			145		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not mpl ed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: f_{JA} is measured in the natural c nvection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: Increase VIN pin voltage gradually higher than V_{VIN_ON} voltage then turn down to 12V.

Operation

SY5867 is a dimming interface converter whose input signal can be a 0/1~10V dimming signal, resistor, or PWM signal. It recognizes the signal automatically.

When input signal is 0/1~10V dimming signal, It will be converted into a PWM signal to driver opto-coupler or dimmable IC.

When input signal is a resistor, there is a current flowing out from DIMI pin to produce a voltage at the resistor. Then It works as same as 0/1~10V dimming input.

When input signal is a PWM signal, it is converted into a reverse PWM signal.

There are two working modes.

Low-clamp is used to clamp the minimum duty cycle.
High-clamp is used to clamp the maximum duty cycle.
More detail information is discussed below.

Applications Information

Start up

Supposing DIMI is floating.
DIMO follow VIN before VIN reach V_{IN_ON}. After reaching V_{IN_ON}, IC begin to work and DIMO is regulated by DIMI.

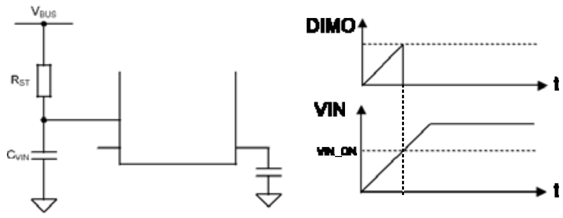


Fig.4 Start up

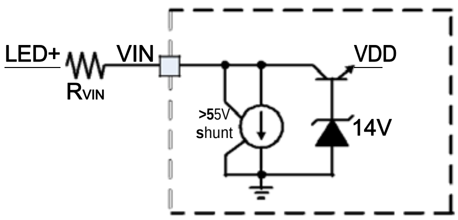


Fig.5 internal LDO

IC integrates a 60V LDO for simplifying peripheral device.

There is a shunt current if VIN voltage is larger than 55V which helps to protect IC when power voltage is high than 55V.

2. Dimming Input

(1) 0/1~10V Dimming

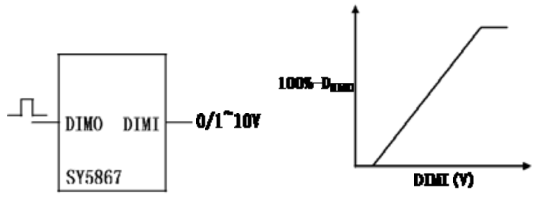


Fig.6 0/1~10V Dimming

If input signal of DIMI pin is 0/1~10V, it is converted into reversed duty signal.

(2) Resistor Dimming

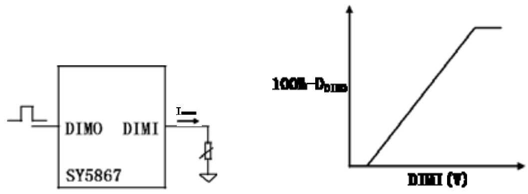


Fig.7 Resistor Dimming

If DIMI is connected with a variable resistor, there is a current flow from DIMI pin to drive the resistor and produce 0~10V signal. Also, the current exists in 0/1~10V dimming application.

(3) PWM Dimming

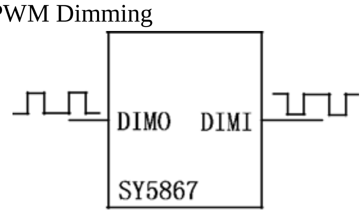


Fig.8 PWM Dimming

If input dimming signal is PWM signal, IC converts it into a reversed PWM signal.

3. Working Mode

(1) High clamp mode

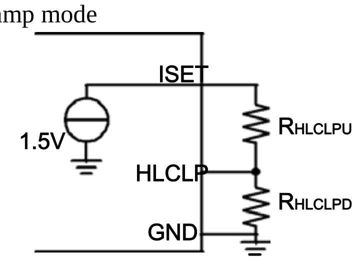


Fig.9 High clamp mode setting

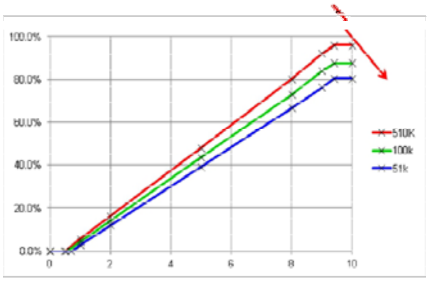


Fig.10 High clamp mode design result

As showed above, High clamp mode is used to set the maximum duty which can regulate the full load current in some special application.

If the voltage of HLCLP pin is less than V_{HLCLP_MODE} when VIN firstly reach V_{VIN_ON}, the high clamp mode is selected. To ensure IC enters into high clamp mode, R_{HLCLPU} should not be connected.

The turning point of DIMI is always 9.5V, and the maximum duty can be calculated by the following formula.

$$D_{MAX} = \frac{1}{2.2-0.2} \cdot \left(\frac{(9.5-0.2)\cdot\frac{14.58\cdot R_{HLCLPD}}{14.58+R_{HLCLPD}}}{\frac{14.58\cdot R_{HLCLPD}}{14.58+R_{HLCLPD}}+52.85} \right)$$

Or

$$D_{MAX} = \frac{67.79\cdot R_{HLCLPD}}{67.43\cdot R_{HLCLPD}+770.59}$$

With different R_{HLCLPD}, the maximum duty is changed. The design result is showed above.

(2) Low Clamp Mode

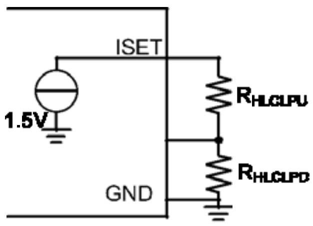


Fig.11 Low clamp mode setting

Fig.12 Low clamp mode design result

Low clamp mode is used to clamp the minimum duty as showed above.

If the voltage of HLCLP pin is larger than V_{HLCLP_MODE} when VIN reach V_{VIN_ON}, the low clamp mode is selected. To ensure IC enters into low clamp mode, please ensure:

$$\frac{V_{ISET}\cdot R_{HLCLPD}}{R_{HLCLPD}+R_{HLCLPU}} > V_{HLCLP,MODE}+0.1$$

The turning point of DIMI pin is set by

$$V_{LCLP} = \frac{9.3}{2}\cdot(V_{HLCLP}-0.2)+0.2 = \frac{9.3}{2}\cdot\left(\frac{V_{ISET}\cdot R_{HLCLPD}}{R_{HLCLPU}+R_{HLCLPD}}-0.2\right)+0.2$$

With different R_{HLCLPU} and R_{HLCLPD}, the minimum duty is set. The design result is showed above.

(3) Special low clamp mode

If there is no need to work in high clamp mode or low clamp mode, It can s t by that:

$$V_{LCLP} = 0.2$$

It means that:

$$\frac{V_{ISET}\cdot R_{HLCLPD}}{R_{HLCLU}+R_{HLCLPD}} = 0.2$$

4. Zero coordinate setting

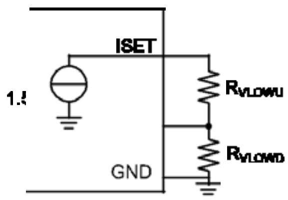


Fig.13 zero coordinate setting

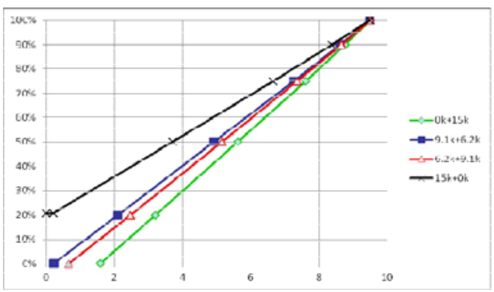


Fig.13 zero coordinate design result

Adjust the zero cross point of the curve by setting the voltage of VLOW. The formula is showed below.

$$V_{LOWI} = 1.55\cdot K1\cdot V_{LOW} - K1\cdot 0.926 + 0.2$$

K1 is a compensation for high clamp mode.

$K1=1$; (Low clamp mode)

$$K1=\frac{14.58}{52.85+14.58}\cdot\frac{52.85+(14.58\,//\,R_{HLCLPD})}{14.58/\,/R_{HLCLPD}}$$; (High clamp mode)

If VLOWI is less than 0.2V, the duty is clamped when DIMI<0.2V.

And the V_{LOW} is set by:

$$V_{LOW}=\frac{V_{ISET}\cdot R_{VLOWD}}{R_{VLOWU}+R_{VLOWD}}$$

The design result is showed above.

5. Curve translation

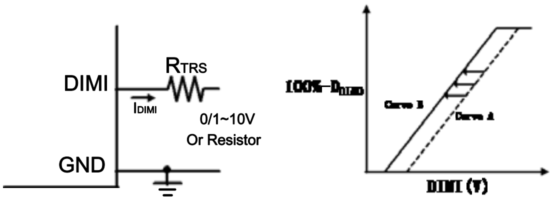


Fig.14 curve translation setting

To translate the converted curve, R_{TRS} is set. With greater R_{TRS}, converted curve is changed from A to B as showed above.

6. DIMI current set

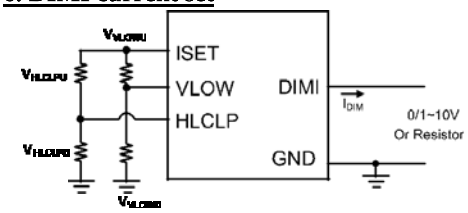


Fig.15 DIMI current setting

If the dimmer is passive device or a resistor, there should be a drive current to power the dimmer.
The current is set by:

$$I_{DIMI}=\frac{5\times 1.5}{R_{ISET}}$$

$$R_{ISET}=(R_{HLCLPU}+R_{HLCLPD})\,/\,/(R_{VLOWU}+R_{VLOWD})$$

7. Frequ ncy setting

There is a 20uA current charge or discharge FSET capacitor to produce a reference triangle wave.
The frequency is set by:

$$F_{DIM}=\frac{20U}{2\cdot(2.2-\frac{1}{3}\cdot V_{LOW})\cdot C_{FSET}}$$

Design Example

A design example of typical application is shown below step by step.

Example A

#1. Identify design specification

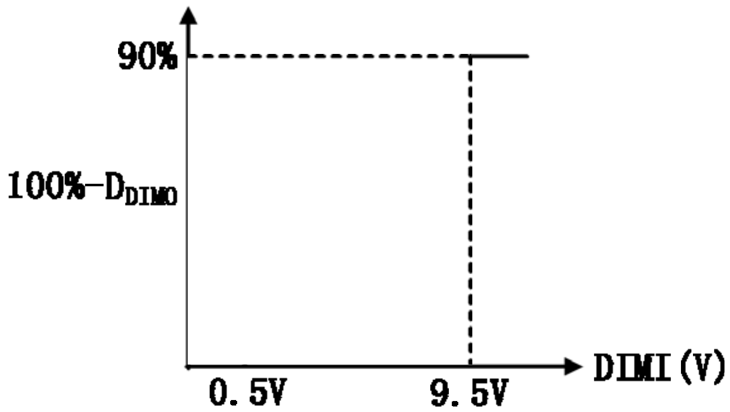


Fig.16 Target Curve

Target parameter			
I_{DIMI}	500uA	Fs	1kHz
V_{LOWI}	0.5	D_{MAX}	90%

(a). Mode Selection

As described above, high clamp mode is selected.

(b). D_{MAX} calculation

$$D_{MAX} = \frac{67.79 \cdot R_{HCLPD}}{67.43 \cdot R_{HCLPD} + 770.59} = 90\%$$

So,

$$R_{HCLPU} = NC$$

$$R_{HCLPD} = 97.6K\ OHM \approx 100K\ OHM$$

(c). VLOWI calculation

$$K1 = \frac{14.58}{52.85 + 14.58} \cdot \frac{52.85 + (14.58 // R_{HLCLPD})}{14.58 // R_{HLCLPD}} = 1.114$$

$$V_{LOWI} = 1.55 \cdot K1 \cdot V_{LOW} - K1 \cdot 0.926 + 0.2 = 0.5$$

$$V_{LOW} = \frac{V_{ISET} \cdot R_{VLOWD}}{R_{VLOWU} + R_{VLOWD}} = 0.771$$

So,

$$R_{VLOWD} = 1.06 \cdot R_{VLOWU}$$

(d). I_{DIMI} calculation

$$I_{DIMI} = \frac{5\times1.5}{R_{ISET}} = 500UA$$

$$R_{ISET} = (R_{HLCLPU} + R_{HLCLPD}) // (R_{VLOWU} + R_{VLOWD}) = 15KOHM$$

So,

$$R_{VLOWU} = 7.28\ KOHM \approx 7.2\ KOHM$$

$$R_{VLOWD} = 7.72\ KOHM \approx 7.8\ KOHM$$

(e). Fs calculation

$$F_{DIM} = \frac{20U}{2\cdot(2.2 - \frac{1}{3}\cdot V_{LOW})\cdot C_{FSET}} = 1KHZ$$

So,

$$C_{FSET} = 5.1NF$$

(f). The design Result

Conditions			
RHLCLPU	NC	RHLCLPD	100k ohm
RVLOWU	7.2k ohm	RVLOWD	7.8k ohm
CFSET	5.1nF		

Example B

#1. Identify design specification

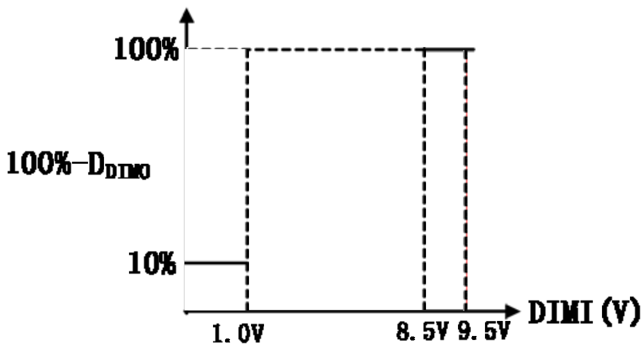


Fig.17 Target Curve

Target pa ameter			
IDIMI	500uA	Fs	1kHz
VLCLP	1.0	DMIN	10%
VHCLP	8.5	DMAX	90%

(a). Mode Selection
As described above, Low clamp mode is selected.

(a). translation calculation

$$R_{TRS} = \frac{V_{HIGH} - V_{HCLP}}{I_{DIMI}} = \frac{9.5-8.5}{0.5} KOHM = 2\,KOHM$$

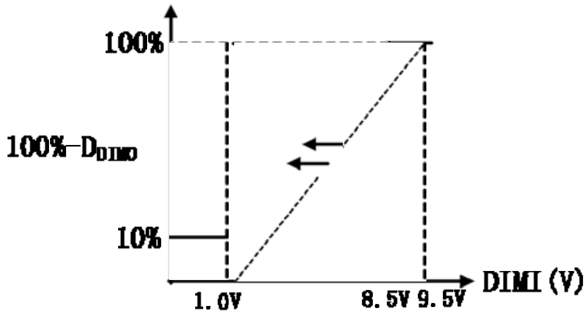


Fig.18 Curve translation

(b). VLOWI calculation
Zero Cross point:

$$V_{LOWI} = \frac{8.5-1.0}{100\%-10\%}(0-10\%) + 1.0 + I_{DIMI} \cdot R_{TRS} = 1.167\ V$$

Due to,

$$V_{LOWI} = 1.55 \cdot V_{LOW} - 0.926 + 0.2 = 1.167$$

$$V_{LOW} = \frac{V_{ISET} \cdot R_{VLOWD}}{R_{VLOWU} + R_{VLOWD}} = 1.22$$

So,

$$R_{VLOWD} = 4.38 \cdot R_{VLOWU}$$

(c).Low clamp mode design

$$V_{LCLP} = \frac{9.3}{2} \cdot (V_{HLCLP} - 0.2) + 0.2$$

$$= \frac{9.3}{2} \cdot (\frac{V_{ISET} \cdot R_{HLCLPD}}{R_{HLCLPU} + R_{HLCLPD}} - 0\ 2) + 0.2 = V_{LCLP} + I_{DIMI} \cdot R_{TRS}$$

So,

$$R_{HLCLPD} = 0.64 \cdot R_{HL\ LPU}$$

If $R_{HLCLPU} + R_{HLCLPD} = 100\ KOHM$

$R_{HLCLPU} = 61.0KOHM \approx 62KOHM$

$R_{HLCLPD} = 39KOHM$

(d).I_{DIMI} calculation

$$I_{DIMI} = \frac{5 \times 1.5}{R_{ISET}} = 500\ UA$$

$$R_{ISET} = (R_{HLCLPU} + R_{HLCLPD}) // (R_{VLOWU} + R_{VLOWD}) = 15\,KOHM$$

So,

$$R_{VLOWU} = 3.3KOHM$$

$$R_{VLOWD} = 14.4KOHM \approx 15KOHM$$

(e). Fs calculation

$$F_{DIM} = \frac{20U}{2\cdot(2.2 - \frac{1}{3}\cdot V_{LOW})\cdot C_{FSET}} = 1KHZ$$

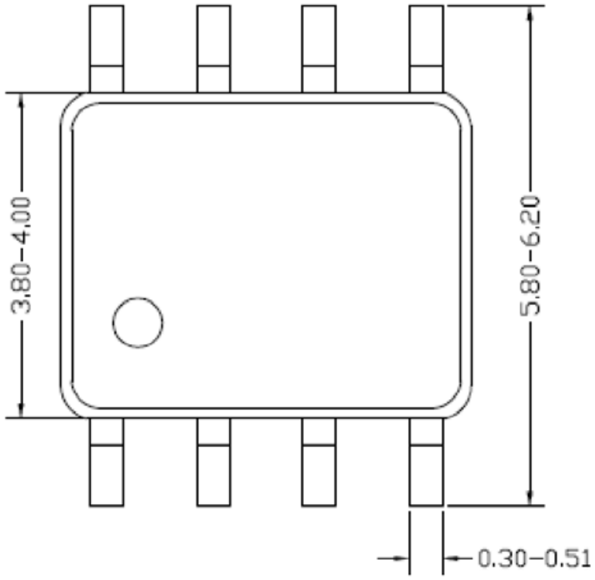
So,

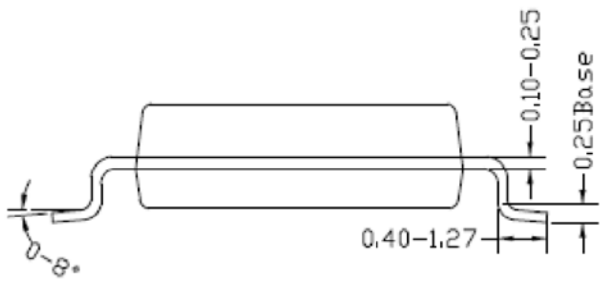
$$C_{FSET} = 5.1NF$$

(f). The design Result

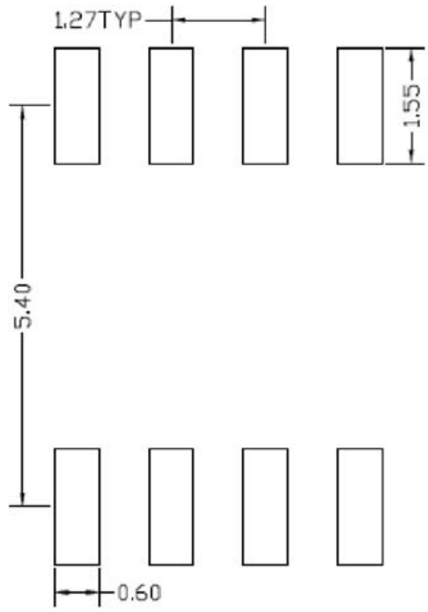
Conditions			
R_{HLCLPU}	62k ohm	R_{HLCLPD}	39k ohm
R_{VLOWU}	3.3k ohm	R_{VLOWD}	15k ohm
R_{TRS}	2.0k ohm	C_{FSET}	5.1nF

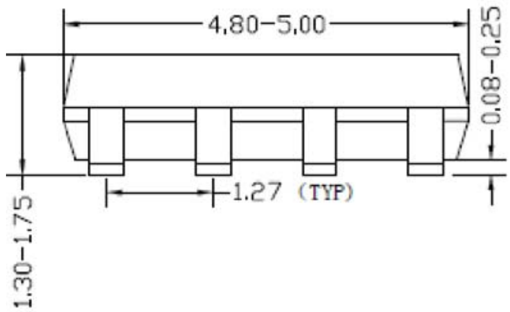
SO8 Package outline & PCB layout design





Top view **Side view**





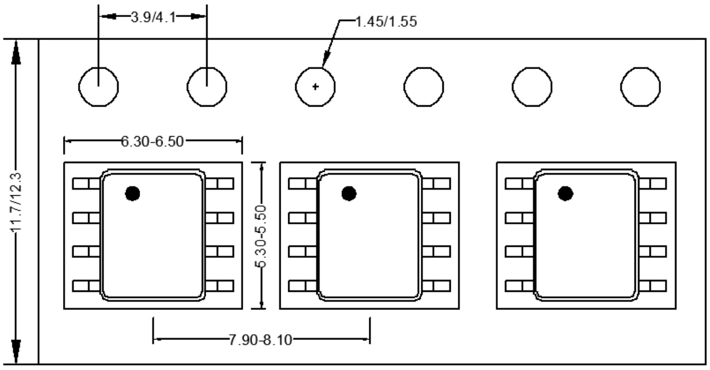
Front view

Recommended Pad Layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

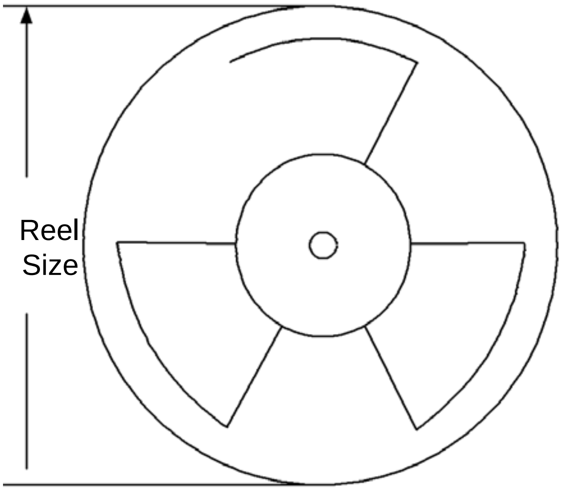
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500