# Application Note: SY6283/SY6283A 

## Low Loss Power Distribution Load Switch <br> 3A continuous, 4A peak current

## General Description

SY6283 and SY6283A are ultra-low $\mathrm{R}_{\mathrm{DS}(\mathrm{ON})}$ switch with current limiting function to protect the power source from over current and short circuit conditions.

## Ordering Information

SY6283


Temperature Code
Package Code
Optional Spec Code

| Ordering Number | Package type | Note |
| :---: | :---: | :---: |
| SY6283DRC | DFN1.2 1.6-4 | 3A/Active High |
| SY6283ADRC | DFN1.2 $1.6-4$ | 3A/Active High |

## Features

- Distribution voltages: 2.5 V to 5.5 V
- Over temperature shutdown and automatic retry
- Reverse blocking (no body diode)
- At shutdown, OUT can be forced higher than IN
- Built-in softstart
- Output discharge function
$\diamond$ SY6283: No output discharge function
$\diamond$ SY6283A: Auto output discharge function
- RoHS Compliant and Halogen Free
- Compact packages minimize board space: DFN1.2x1.6-4


## Typical Application Circuit



Figure 1. Schematic Diagram


Figure 2. Typical Perform Characteristic

## Pin Configurations (Top View)



Top mark: LPxyz for SY6283(Device code: LP, $\boldsymbol{x}=\boldsymbol{y e a r}$ code, $\boldsymbol{y}=\boldsymbol{w e e k}$ code, $\boldsymbol{z}=$ lot number code) MWxyz for SY6283A(Device code: MW, $\boldsymbol{x}=$ year code, $\boldsymbol{y}=\boldsymbol{w e e k}$ code, $\boldsymbol{z}=$ lot number code)

## Functional Pin Description

| Pin Name | Pin number | Pin Description |
| :---: | :---: | :--- |
| IN | 3 | Input pin. Decouple this pin to GND with 4.7uF input <br> Capacitor. |
| GND | 1 | Ground pin. |
| OUT | 4 | Output pin. |
| EN | 2 | ON/OFF control. Do not leave it float. |

Absolute Maximum Ratings (Note 1)
All pins ..... 6 V
Power Dissipation, $\mathrm{PD} @ \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ DFN1.2 $\times 1.6-4$ ..... 0.5 W
Package Thermal Resistance (Note 2)
$\theta_{\text {JA }}$ ..... $200^{\circ} \mathrm{C} / \mathrm{W}$
$\theta$ лс ..... $70^{\circ} \mathrm{C} / \mathrm{W}$
Junction Temperature Range $-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$
Lead Temperature (Soldering, 10 sec .) ..... $-260^{\circ} \mathrm{C}$
Storage Temperature Range ..... $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$
Recommended Operating Conditions (Note 3)
IN- ..... 2.5 V to 5.5 V
EN- ..... -0.3 V to $\mathrm{V}_{\text {IN }}+0.3 \mathrm{~V}$
All other pins$0-5.5 \mathrm{~V}$
Junction Temperature Range ..... $-40^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$
Ambient Temperature Range $-40^{\circ} \mathrm{C}$ to $85^{\circ} \mathrm{C}$

## Electrical Characteristics

( $\mathrm{VIN}_{\mathrm{IN}}=5 \mathrm{~V}, \mathrm{C}_{\mathrm{L}}=1 \mathrm{uF}$, per channel, $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
| :--- | :--- | :--- | :---: | :---: | :---: | :---: |
| Input Voltage Range | $\mathrm{V}_{\mathrm{IN}}$ |  | 2.5 |  | 5.5 | V |
| Shutdown Input Current | IsHDN | Output grounded, switch off |  | 0.1 | 1 | $\mu \mathrm{~A}$ |
| Quiescent Supply Current | $\mathrm{I}_{\mathrm{Q}}$ | Open load switch on |  | 32 |  | $\mu \mathrm{~A}$ |
| FET RON | $\mathrm{R}_{\mathrm{DS}(O \mathrm{ON})}$ |  |  | 60 |  | $\mathrm{~m} \Omega$ |
| Current Limit | $\mathrm{I}_{\mathrm{LIM}}$ |  | 3.0 | 3.85 | 4.7 | A |
| EN Rising Threshold | $\mathrm{V}_{\mathrm{IH}}$ |  | 2 |  |  | V |
| EN Falling Threshold | $\mathrm{V}_{\mathrm{IL}}$ |  |  |  | 0.8 | V |
| IN UVLO Threshold | $\mathrm{V}_{\mathrm{IN}, \text { UvLO }}$ |  |  |  | 2.4 | V |
| IN UVLO Hysteresis | $\mathrm{V}_{\mathrm{IN}, \mathrm{HYS}}$ |  |  | 0.1 |  | V |
| Rising Time | $\mathrm{t}_{\text {Rising }}$ | $\mathrm{R}_{\mathrm{L}}=5 \Omega, \mathrm{C}_{\mathrm{L}}=1 \mathrm{uF}$ |  | 0.75 |  | ms |
| Thermal <br> Temperature Shutdown | $\mathrm{T}_{\mathrm{SD}}$ |  | 150 |  | ${ }^{\circ} \mathrm{C}$ |  |
| Thermal Shutdown Hysteresis |  |  |  | 20 |  | ${ }^{\circ} \mathrm{C}$ |
| Output Discharge Resistor | $\mathrm{R}_{\mathrm{DSC}}$ | SY6283A |  | 10 |  | $\Omega$ |

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: $\theta_{\mathrm{JA}}$ is measured in the natural convection at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

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Time (400us/div)

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Output Fall Time vs. $\mathrm{V}_{\mathrm{IN}}$


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## Block diagram



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## Operation

SY6283 is a current limited P-channel MOSFET power switch with over current and over temperature protections. There is no body diode across the drain and the source of the MOSFET. It prevents the current flow from the output to the input after the chip is disabled.

## Over-current protection

When the over-current condition is detected, the switch is regulated to achieve constant output current. If the over current condition lasts for a long time, and results in a junction temperature over $150^{\circ} \mathrm{C}$, the switch will be shutdown. Once the junction temperature drops to $130^{\circ} \mathrm{C}$, the part will restart.

## PCB Layout Guide

For best performance of the SY6283, the following guidelines must be strictly followed:
$>$ Keep all $\mathrm{V}_{\text {BuS }}$ traces as short and wide as possible and use at least 2 ounce copper for all $\mathrm{V}_{\text {Bus }}$ traces.
> Place a ground plane under all circuitry to lower both resistance and inductance and improve DC and transient performance.
> A low-ESR 150 uF aluminum electrolytic or tantalum capacitor between VOUT and GND is strongly recommended.
$>$ Locate the output capacitor as close to the connectors as possible to lower impedance(mainly inductance) between the port and the capacitor and improve transient performance.
$>$ Input and output capacitors should be placed closed to the IC and connected to ground plane to reduce noise coupling.
> Locate the ceramic bypass capacitors as close as possible to the VIN pins and VOUT pins of SY6283.

## Supply Filter Capacitor

In order to prevent the input voltage from dropping during hot-plug condition, a $10 \mu \mathrm{~F}$ ceramic capacitor from VIN to GND is strongly recommended. However, higher capacitance could help to reduce the voltage drop. Furthermore, an output short will cause ringing on the input without the input capacitor. It could destroy the internal circuitry when the input transient voltage exceeds the absolute maximum supply voltage even for a short duration.


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## PCB Layout Guide



PCB Top Over Layer


PCB Top Layer

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## DFN1.2x1.6-4 Package Outline



Side View

Notes: All dimension in millimeter and exclude mold flash \& metal burr.

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## Taping \& Reel Specification

1. DFN1.2x1.6 taping orientation

2. Carrier Tape \& Reel specification for packages


## 3. Others: NA

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