Application Notes: AN_SY6926

$5V_{IN}$, 5A, Bi-directional Regulator for Single Cell Li-Ion Battery Power Bank Application

General Description

SY6926 is a 4.1-6.5V_{IN} up to 18V_{IN} surge bi-directional regulator designed for single cell Li-Ion battery power bank application. Advanced bi-directional energy flow control with automatic input power source detection is adopted to achieve battery charging mode and battery power supply mode alternately. If the external power supply is present, SY6926 runs in battery charging mode with fully protection function; if the external power supply is absent, SY6926 runs in battery power supply mode with output current capability up to 2.5A.

SY6926 has an integrated reverse blocking switch to prevent current leaking from the system side or battery side to the input side and an integrated linear switch to achieve over voltage/current protection at the system side. A half bridge with 1MHz switching frequency is integrated to achieve power conversion for battery charging mode and battery power supply mode. All of them adopt N-channel MOSFETs with 18V rating and extremely low $R_{DS(ON)}$ to optimize operation efficiency and extend battery life-time.

SY6926 is available in QFN4x4 package to minimize the PCB layout size for wide portable applications.

Ordering Information

SY6926 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY6926QYC	QFN4x4-20FC	

Features

- Low Profile Package QFN4x4 for Portable Applications
- Integrated N-Channel MOSFETs with 18V Voltage Rating and Extremely Low RDSON
- 1MHz Switching Frequency to Minimize Peripheral Circuit Design
- Trickle Current / Constant Current / Constant Voltage Charging Mode
- Maximum 5A Battery Charging Current
- Maximum 2.5A Sys current in Battery power supplement mode
- Automatic Input Power Source Detection
- Programmable SYS Voltage for Battery Power Supply Mode
- Programmable Constant Current Charging
- Programmable Over Current Limit for SYS load in Battery power supplement mode
- Programmable Battery Charging Timeout
- Programmable Input Current DPM
- Programmable Input Voltage DPM
- Charging shutdown control
- Charging mode CV tolerance +/-0.5%
- Charging mode CV voltage selectable between 4.2V&4.35V
- Host Enable Control for Standby Mode
- Over Temperature Protection
- Charge Status Indication

Applications

- Single cell Li-Ion Power Bank
- Battery power path management

Typical Applications

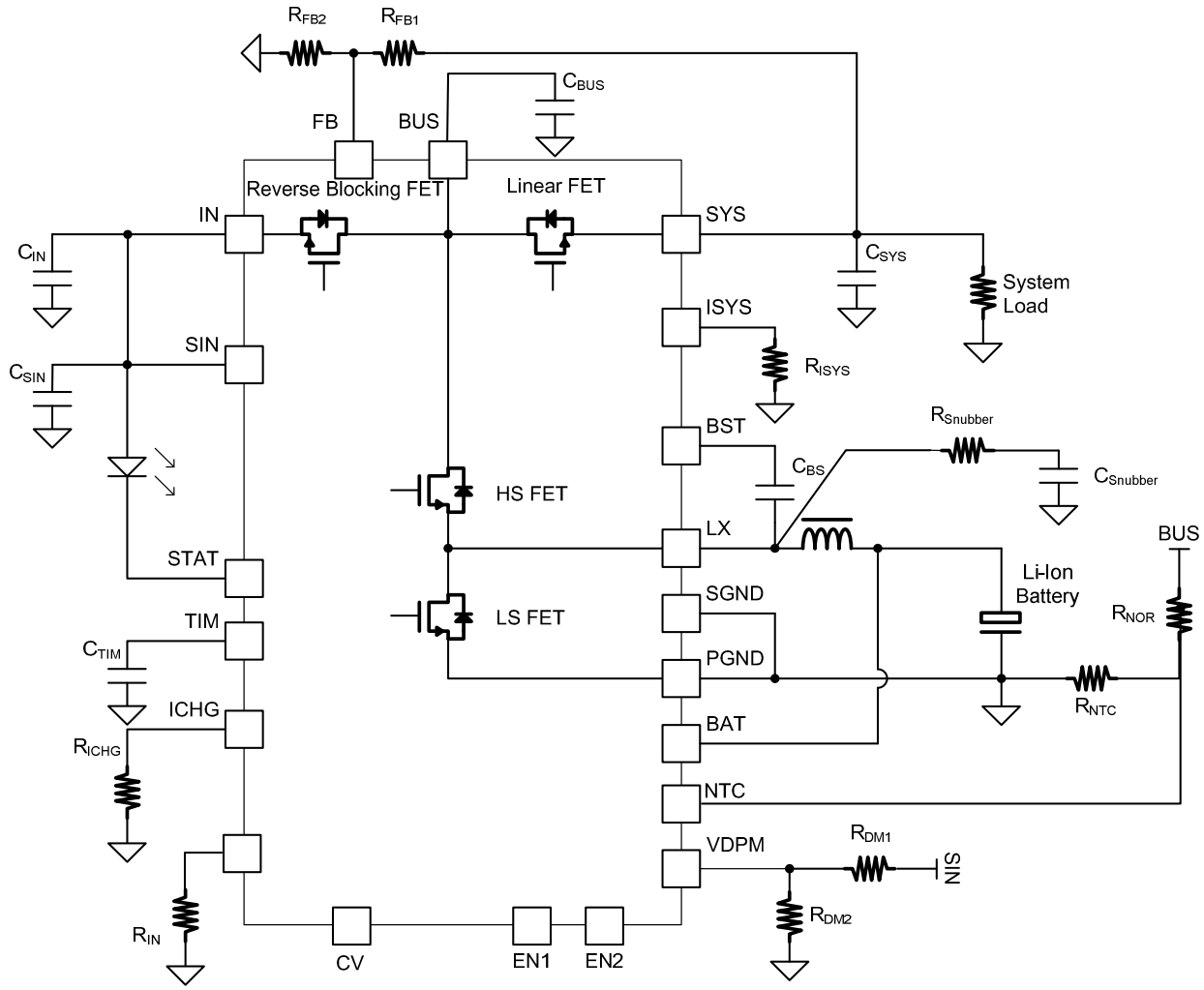
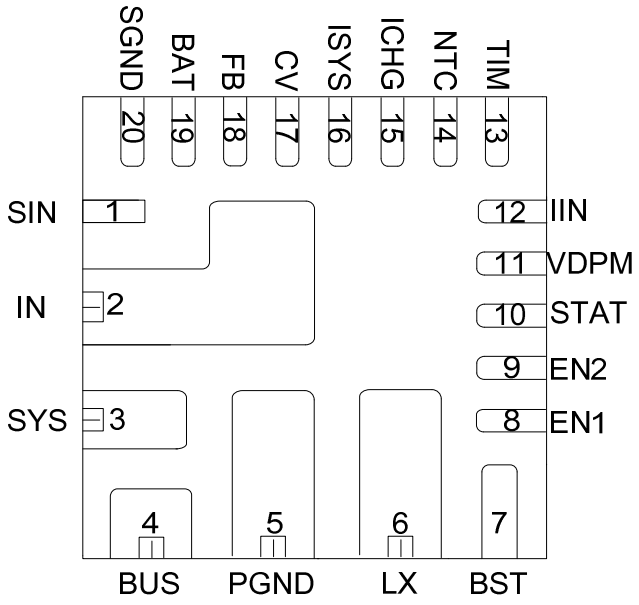


Figure 1. Schematic Diagram

Pinout (Top view)



(QFN4x4-20FC)

Top Mark: AXV*xyz* (device code: **AXV**, ***x=year code, y=week code, z= lot number code)***

Name	PIN Number	Description
SIN	1	Signal Input supply pin.
IN	2	Positive power supply input pin. V_{IN} ranges from 4.1V to 6.5V for normal operation and up to 18V surge. Connect a MLCC from this pin to ground to decouple high frequency noise.
SYS	3	System load pin. Connect a MLCC from this pin to ground to decouple the high frequency noise.
BUS	4	Connection point for reverse blocking FET and bypass linear switch. Connect a MLCC from this pin to ground to decouple the high frequency noise .
PGND	5	Power ground pin.
LX	6	Switch node pin. Connect an external inductor from this pin to BAT pin.
BST	7	Boot strap pin. Connect a MLCC from this pin to LX.
EN1	8	Enable control pin for linear FET. Pull down EN1 to shutdown linear FET.
EN2	9	Enable control pin for linear FET and sync-boost converter both. If the external power source is present, the function of EN2 is disabled all. If the external power source is absent, pull down EN2 to shutdown linear FET and sync-boost converter both to save the leakage power from battery.
STAT	10	Charging status indication pin. It is open drain output pin and can be used to turn on a LED to indicate the charge in process. When the charge is done, LED is off.
VDPM	11	Input DPM voltage program pin. The regulated input voltage equals to $1.19*(1+R_{DPM1}/R_{DPM2})$
IIN	12	Input current limit program pin. Constant input current reference is programmed by a resistor connected from this pin to ground.
TIM	13	Charging time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor to set the charging time limit both for the Trickle Current mode, CV mode and Constant Current mode. Trickle current charging time limit is about 1/9 of Constant current and CV charging time.
NTC	14	Thermal protection pin. UTP threshold is about $61.6\%V_{BUS}$ and OTP threshold is about $30\%V_{BUS}$. Pulling it down lower than 0.3V to disable charger.
ICHG	15	Battery charging current program pin. Constant current charging reference is programmed by a resistor connected from this pin to ground. The trickle charging current would be 1/10 of the constant charging current.
ISYS	16	System over current limit program pin. Connect a resistor from ISYS pin to ground to program the over current limit for system load. It has the max internal default limit.
CV	17	Charge voltage selection pin. Open or pull low for 4.2V. Pull high for 4.35V
FB	18	SYS voltage feedback pin. Program the external resistor divider to program the bus voltage. $Vsys=1.19*(1+R_{FB1}/R_{FB2})$.The maximum sys Voltage set is 6V.
BAT	19	Battery positive pin. Also connect to inductor terminal.
SGND	20	Signal ground pin.

Absolute Maximum Ratings (Note 1)

STAT, LX, BUS, FB, BAT, NTC, SYS, EN1, EN2, ---------- -0.5- 18V
IN, SIN, ---------- -0.5- 18V
ICHG, ISYS,IIN, VDPM, CV, ---------- -0.5-18V
TIM,BST-LX, ---------- -0.5-4V
Power Dissipation, PD @ TA = 25°C, ---------- 2.5 W
Package Thermal Resistance (Note 2)
θJA---------- 40 °C/W
θJC ---------- 20 °C/W
Junction Temperature Range ---------- -40°C to +150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

Recommended Operating Conditions (Note 3)

STAT, LX, BUS, FB, BAT, NTC, SYS, EN1, EN2, ---------- 0-16V
IN, SIN, ---------- 4-6.5V
ICHG, ISYS, IIN, VDPM , CV, ---------- 0-16V
TIM,BST-LX, ---------- 0-4V
Junction Temperature Range ---------- -20°C to 100°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, T_A=T_J, V_{IN}=5V, GND=0V, C_{IN}=20uF, L_B=0.68uH, C_{TIM}=330nF, C_{OUT}=20uF, C_{BUS}=20uF, C_{SYS}=10uF, R_{FB1}=43k, R_{FB2}=13k, R_{DM1}=27k, R_{DM2}=10k, R_{ISYS}=50k, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Quiescent Current						
I_{BAT}	Battery discharge current	EN1 and EN2 pull down, FB pull high to BUS , NTC=0V.			10	uA
I_{IN}	Input quiescent current				1.5	mA
I_{BOOST}	Boost null-load quiescent current	V_{BAT}=4.35V,I_{SYS}=0A, R_{NOR}=100k, Remove R_{FB1} , Remove EN1 、 EN2 pull down resistor.Converter switching.		1.5		mA
Automatic Input Power Supply Detection						
I_{DIS}	Input discharge current	V_{IN}=5V		10		mA
T_{DIS}	Input discharge time interval			100		ms
V_{INUVLO}	Input voltage UVLO threshold	Rising edge	3.9	4.1	4.3	V
V_{UVHYS}	Input voltage UVLO hysteresis	Falling edge		100		mV
System Short Circuit Protection						
T_{REC}	Recovery time interval			5		ms
T_{RECP}	Recovery period			0.7		s
I_{RECP}	Recovery current peak			1700		mA
Linear FET						
I_{SYSMAX}	Maximum system load current		2.5			A
V_{SYSMAX}	Maximum system voltage		5.6	5.8	6.0	V
	System current limit accuracy	R_{ISYS}=72k, boost mode	-20%		20%	
I_{SYSUP}	Charging Current for SYS voltage ramp up	V_{BUS}=5V, V_{SYS}<90%V_{BUS}		500		mA
$V_{SHORTSYS}$	System short circuit protection threshold		2.0	2.3	2.6	V
Half-bridge in Charge Mode						
Voltage and Current Bias						
V_{BUSBAT}	Charging mode voltage threshold	V_{BUS}-V_{BAT} ,rising edge		162		mV
V_{BUS}	Supply voltage for battery charging		4.5		6.5	V
V_{INOVP}	Input voltage over voltage protection	Rising edge	6.7	7	7.4	V
$V_{INOVPHYS}$	Input voltage OVP hysteresis	Falling edge		500		mV
Timer						
T_{TC}	Trickle current charge timeout	C_{TIM}=330nF	0.425	0.5	0.575	hour
T_{CC}	Constant current and CV charge timeout		3.825	4.5	5.175	hour
T_{MC}	Charge mode change delay time			30		ms
T_{TERM}	Termination delay time			30		ms
T_{RCHG}	Recharge time delay			30		ms
Switching Frequency						
f_{SWBK}	Buck Switching frequency			1.0		MHz
Battery Charging						
V_{CV}	Battery 4.35V CV charging mode	0°C <=T_A<=70°C, voltage on BAT pin	4.328	4.35	4.372	V
	Battery 4.2V CV charging mode	0°C <=T_A<=70°C, voltage on BAT pin	4.179	4.2	4.221	V
ΔV_{RCH}	Battery voltage threshold hysteresis	0°C<=T_A<=70°C,falling	50	100	150	mV

	for recharge	edge				
V_{TRK}	Battery trickle charging mode voltage threshold	0°C<=T_A<=70°C,rising edge	2.6	2.8	3.0	V
I_{CCMAX}	Maximum constant charge current		5			A
V_{BTOVP}	Battery voltage OVP threshold		105%	110%	115%	V_{CV}
I_{CC}	Charging current accuracy for Constant Current Mode	I_{CC}=(1V/R_{ICHG})*16k	-20%		20%	
I_{TC}	Charging current accuracy for Trickle Current Mode			10%		Icc
I_{TERM}	Charging current accuracy for Termination Current			10%		Icc
Battery Short Circuit Protection						
$V_{SHORTBT}$	Battery short circuit protection threshold	Falling edge	1.85		2.1	V
f_{FBK}	Frequency fold back	V_{BAT}<2V		12.5 %		f_{OSC}
Input Dynamic Power Management						
I_{IN_LIM}	Input current accuracy for Constant Input Current Mode	R_{IN}=2K	-10		10	%
V_{IN_LIM}	Input voltage limit accuracy	V_{IN_LIM}=1.19*(1+ R_{DPM1}/R_{DPM2})	-1.5		1.5	%
Enable						
V_{ENH}	Enable voltage rising threshold		1.4			V
V_{ENL}	Enable voltage falling threshold				0.4	V
Half-bridge in Boost Mode						
Voltage and Current Bias						
V_{SYSREF}	Feedback reference of SYS voltage		1.166	1.19	1.214	V
V_{BUSCLP}	BUS voltage clamping		5.6	5.8	6	V
V_{BATDIS}	Battery discharging clamping		2.5	2.62	2.75	V
I_{DSBAT}	Battery discharging maximum current limit		6.5			A
V_{BOVP}	Bus voltage over voltage protection			9.5		V
$V_{BOVPHYS}$	Bus voltage OVP hysteresis	Falling edge		400		mV
Switching Frequency						
f_{SWBST}	Boost Switching frequency			1.0		MHz
Other General Parameters						
Battery Thermal Protection NTC						
UTP	Under temperature protection	Rising edge	60 %	61.6 %	63.5 %	
	Under temperature protection hysteresis	Falling edge	5%	7%	9%	
OTP	Over temperature protection	Falling edge	28%	30%	32%	
	Over temperature protection hysteresis	Rising edge	1.5%	2.2%	3%	
$V_{SHUTDOWN}$	Pull NTC low to shutdown charger	Falling edge			0.3	V
Power MOSFET						
R_{HSFT}	$R_{DS(ON)}$ of High-Side NFET			20		mΩ
R_{BKFT}	$R_{DS(ON)}$ of reverse blocking NFET			20		mΩ
R_{LSFT}	$R_{DS(ON)}$ of Low-Side NFET			30		mΩ
R_{LNFT}	$R_{DS(ON)}$ of the linear NFET			30		mΩ
I_{LM}	Half Bridge FET current limit			8.0		A

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

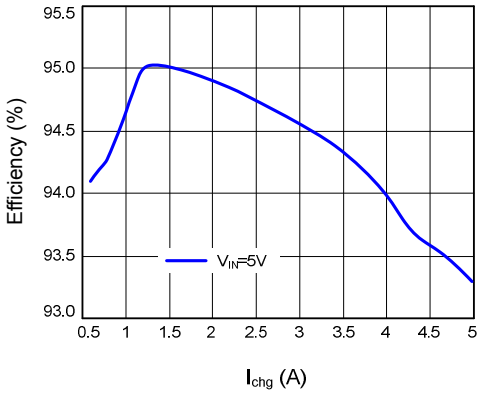
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

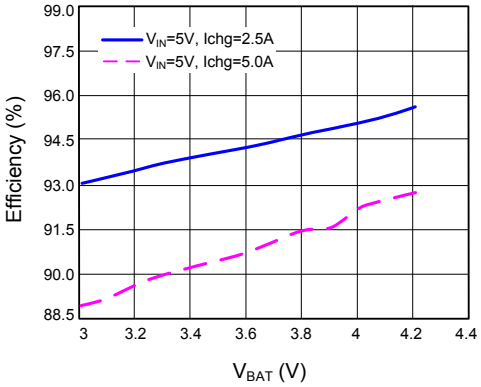
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V , unless otherwise specified.)

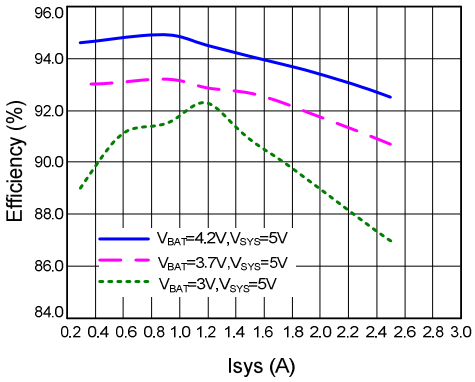
Efficiency vs. Charging current (CV mode)



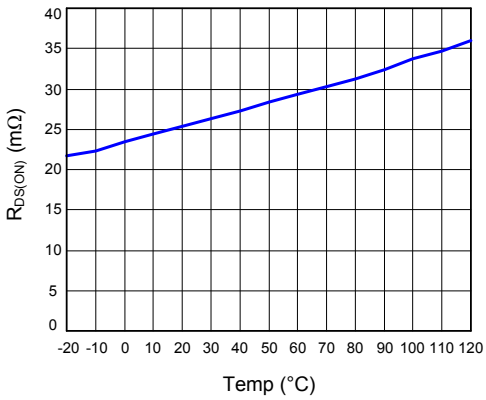
Efficiency vs. Charging Voltage (CC mode)



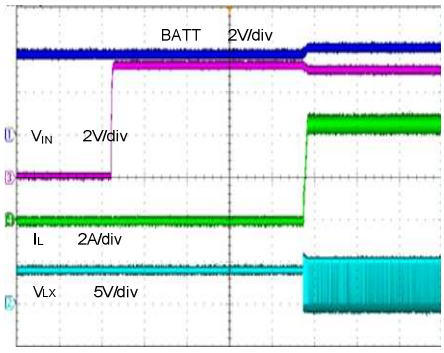
Efficiency vs. Isys (Boost mode)



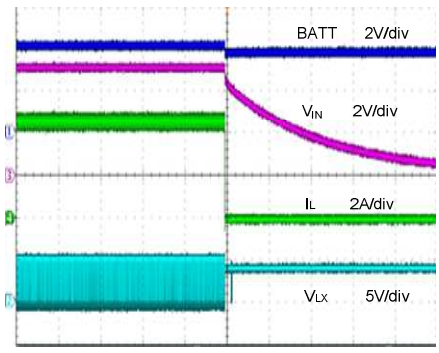
LNFET $R_{DS(ON)}$ vs. Temp



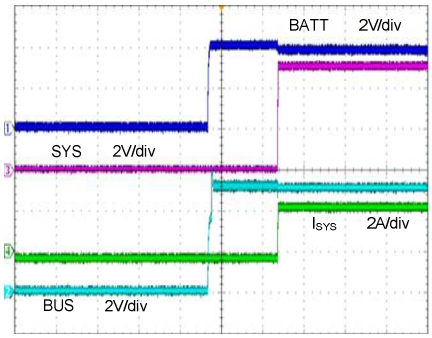
VIN Power on（Adapter）



VIN Power off(Adapter)

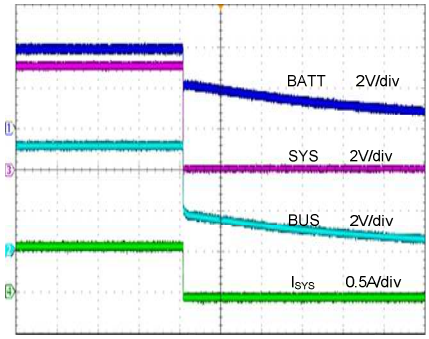


Boost Mode Battery Insert



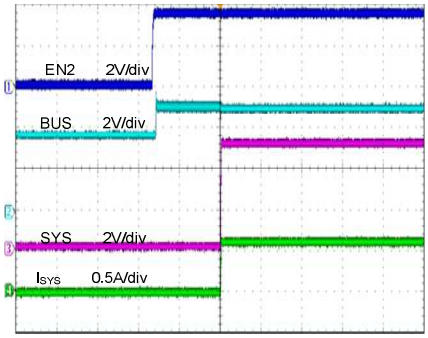
Time (200ms/div)

Boost Mode Battery Remove



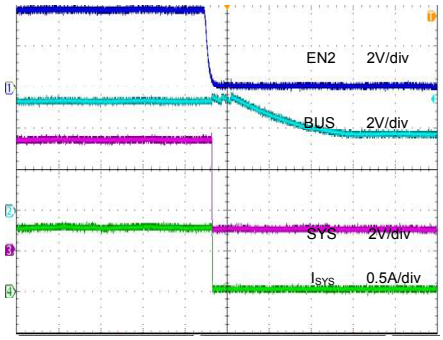
Time (200ms/div)

Boost mode EN2 ON



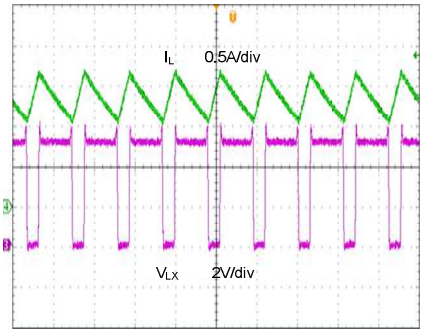
Time (200ms/div)

Boost mode EN2 OFF



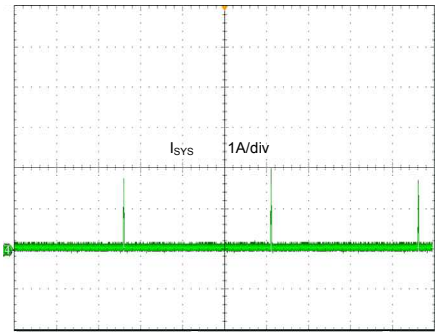
Time (10ms/div)

Boost Steady State



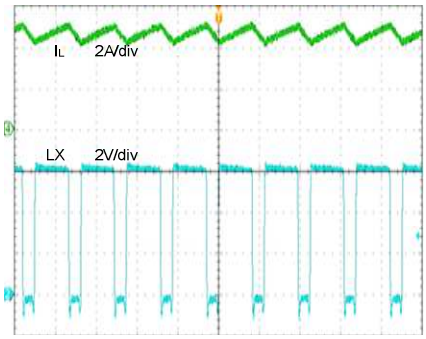
Time (1us/div)

SYS Short



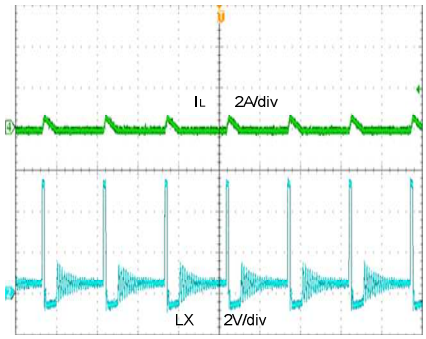
Time (200ms/div)

Constant Current In Charging Mode



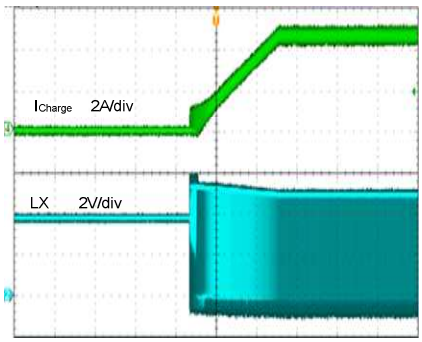
Time (1μs/div)

Battery Short In Charging Mode



Time (4μs/div)

Inductor current soft start in charging mode



Time (10ms/div)

General Function Description

Automatic Input Power Supply Detection

Automatic input power supply detection in SY6926 adopts an internal current source with 10mA maximum capability to discharge the SIN pins for 100ms once V_{SIN} exceeds input UVLO threshold. If the external power supply is present normally, V_{SIN} should keep being higher than the input voltage UVLO even after 100ms discharging.

Programmable Input Current Dynamic Power Management

The input current limit is programmable by R_{in}. Once input current reaches I_{in_lim}, the input current will be limited in I_{in_lim} by regulating the duty of Buck convertor.

Programmable Input Voltage Dynamic Power Management

The input voltage limit is programmable by R_{DM1},R_{DM2}. Once input voltage drops to V_{IN_lim}, the input voltage will be limited in V_{IN_lim} by regulating the duty of Buck convertor.

SYS Over Current Limit

In boost mode, once SYS current exceeds the set SYS current limit the SYS current is limited in the set SYS current limit by regulating the duty of Boost converter .

Charging mode Enable control

Once NTC is lower than 0.3V, Charging is disabled and is not recognized as a fault.

Charging Status Indication Description

1. **Charging-In-Process** – Pull and keep STAT pin to Low;
2. **Charging Done** – Pull and keep STAT pin to High;
3. **Fault Mode** – Output high and low voltage alternatively with 0.7Hz frequency, fault mode includes VIN OVP, BAT OVP, BAT SCP, BAT UTP/OTP, charging time out.

Connect a LED from IN to STAT pin, **LED ON** indicates **Charging-in-Process**, **LED OFF** indicates **Charging Done**, **LED Flash** indicates **Fault Mode**.

Protection Description

During the half-bridge operating as synchronous boost mode, SY6926 has BUS over voltage protection, SYS short circuit protection, BAT over discharging protection, and thermal protection for the Li-Ion battery and the device itself both.

Thermal Protection-Thermal protection for battery is achieved through NTC pin in charging and discharging mode. The basic scheme is shown in application information. Thermal shutdown is active for the device itself. IC recovers to normal work when the temperature returns into normal range again. Charging timer stops and maintains the result without reset.

Short Circuit Protection- There are BAT short circuit protection and SYS short circuit protection in SY6926. When V_{SYS} is lower than $V_{SHORTSYS}$, the linear FET modulates the current to be saw tooth shape from 0A to 1.7A for short circuit protection recovery. SY6926 tries recovery for 5ms per 0.7s.In charging mode once V_{BAT} is lower than $V_{SHORTBT}$, the switching frequency is fold back to 12.5% of the default value.

Over Voltage Protection- When V_{BUS} or V_{BAT} is higher than the over voltage protection threshold, the half bridge stops boost operation or buck operation immediately. It recovers to normal work when the monitored voltage backs to normal level. Input voltage has UVLO and OVP, which would make the device shutdown and recover to normal work when the V_{SIN} backs to normal range.

Battery Over discharge protection

IN battery supplement mode, once battery voltage is lower than V_{BATDIS} , SY6926 will latch off. Only repower IC, or Bus higher than Bat can reset the latch off logic.

Timeout Protection- Programmable timeout protection for the Trickle Current Charge Mode and the Constant Current and CV Charge Mode both. Once timeout is active, the device stops the charge operation and latch-off. Only re-plug in power source can reset the latch logic and restart the normal charging work.

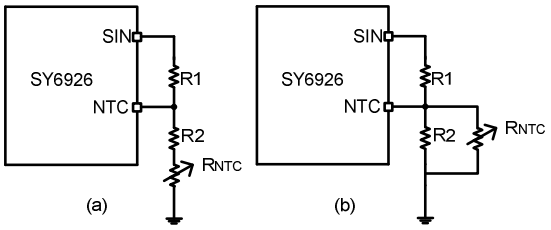
Applications Information

Because of the high integration of SY6926, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, bus capacitor C_{BUS}, battery capacitor C_{BAT}, inductor L, NTC resistors R1, R2, charging current program resistor R_{ICHG}, System over current limit program resistor R_{ISYS} , SYS voltage program resistor R_{FB1}, R_{FB2}, VIN DPM program resistor R_{DM1}, R_{DM2}, Input current limit program resistor R_{IN}, Battery over discharging voltage program resistor R_{DIS1}, R_{DIS2}, and timer capacitor C_{TIM} need to be selected for the targeted applications specifications.

NTC resistor:

SY6926 monitors battery temperature by measuring the BUS voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K (K= V_{NTC}/V_{BUS}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps of figure a are:

1. Define K_{UT}, K_{UT} =60.1~63.1%
2. Define K_{OT}, K_{OT} =28~32%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold and R_{OT} at OTP threshold.
4. Calculate R2

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R1

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values K_{UT} =61.6% and K_{OT}=30%, then

$$R2 = 0.365R_{UT} - 1.365R_{OT}$$

$$R1 = 2.3(R2 + R_{OT})$$

Charging current program resistor R_{ICHG}

The charging current program resistor R_{ICHG} is calculated as below:

$$R_{ICHG} = (1 / I_{CC}) \times 16, \quad \text{Unit: Kohm}$$

While the I_{CC} is the constant charge current，unit is ampere.

System over current limit program resistor R_{ISYS}

The system over current limit program resistor R_{ISYS} is calculated as below:

$$R_{ISYS} = 72 / Isys, \quad \text{Unit: Kohm}$$

While the I_{SYS} is the limited SYSTEM load current, Unit is ampere.

SYS voltage program resistor R_{FB1}, R_{FB2}

SYS voltage is programmed as below:

$$V_{SYS} = 1.19 \times (1 + \frac{R_{FB1}}{R_{FB2}}) \quad \text{Unit: V}$$

Input current limit program resistor R_{IN}

Input current limit is programmed as below:

$$R_{in} = \frac{2}{I_{IN\_lim}} \quad \text{Unit: Kohm}$$

While I_{in_lim}, Unit is ampere.

VIN DPM program resistor R_{DM1}, R_{DM2}

Input voltage limit is programmed as below:

$$V_{IN\_lim} = 1.19 \times (1 + \frac{R_{DM1}}{R_{DM2}}) \quad \text{Unit: V}$$

Timer capacitor C_{TIM}

The charger also provides a programmable charging timer. The charging time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$$C_{TIM} = 2*10^{-11}T_{CC} \quad \text{Unit: F}$$

T_{CC} is the target constant charging time, unit is second.

Input capacitor C_{IN}:

Input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source

impedance to prevent high-frequency-switching current from passing to the input.
To minimize the potential noise problem, place a typical X7R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. At least 20uF ceramic capacitor are suggested.

Bus capacitor C_{BUS}:
1. Buck mode
The capacitor acts as the input capacitor of the buck converter. The input current ripple rms value is larger than:

$$I_{CIN\_MIN} = I_{CHG}\sqrt{D(1-D)}$$

While I_{CHG} is the charge current.
2. Boost mode
C_{BUS} is the output capacitor of boost converter. C_{BUS} reduces the bus voltage ripple and ensures the stability of boost. The output current ripple rms value is :

$$I_{CBUS\_RMS} = \frac{\Delta I}{2\sqrt{3}}$$

While ΔI is the current ripple of inductor.
At least 20uF ceramic capacitor are suggested.

Battery capacitor C_{BAT}:
1. Buck mode
Battery capacitor acts as the output capacitor of Buck converter. C_{BAT} is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X7R or better grade ceramic capacitor. The output voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Buck} = \frac{(1-D)\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L}$$

Where F_{SW} is the switching frequency.
2. Boost mode
C_{BAT} acts as the input capacitor of Boost converter. The input voltage ripple is calculated as below:

$$V_{Ripple\_BAT\_Boost} = \frac{D\times V_{BAT}}{8C_{BAT}F_{SW}{}^2L}$$

Where F_{SW} is the switching frequency.
At least 20uF ceramic capacitor are suggested.
Inductor L:
Inductor selection trades off between cost, size, and efficiency. A lower inductance value corresponds with smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss. An inductor must not saturate under the worst-case condition.
1.Buck mode
1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1-V_{BAT}/V_{IN,\,MAX})}{F_{SW}\times I_{CHG,\,MAX}\times 40\%}$$

Where F_{SW} is the switching frequency and $I_{CHG,MAX}$ is the maximum charge current.
SY6926 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{CHG,\,MAX} + \frac{V_{BAT}(1-V_{BAT}/V_{IN\ MAX})}{2\times F_{SW}\times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

2. Boost mode
1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{BAT}(1-V_{BAT}/V_{BUS\_MAX})}{F_{SW}\times I_{DIS,\,MAX}\times 40\%}$$

Where F_{SW} is the switching frequency and $I_{DIS,MAX}$ is the maximum discharge current.
SY6926 is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > I_{DIS,\,MAX} + \frac{V_{BAT}(1 - V_{BAT}/V_{BUS\_MAX})}{2 \times F_{SW} \times L}$$

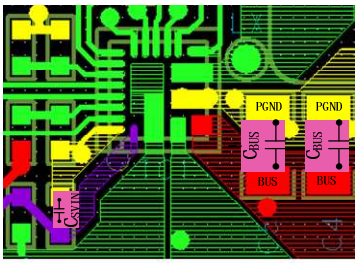
3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement.

Icc(A)	L(uH)
2	1
5	0.68

Layout Design:
The layout design of SY6926 regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, C_{BUS},L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND, C_{BUS} must get close to Pins BUS and GND. The loop area formed by C_{IN} and GND, C_{BUS} and GND must be minimized.
Following figure is the recommended layout design.

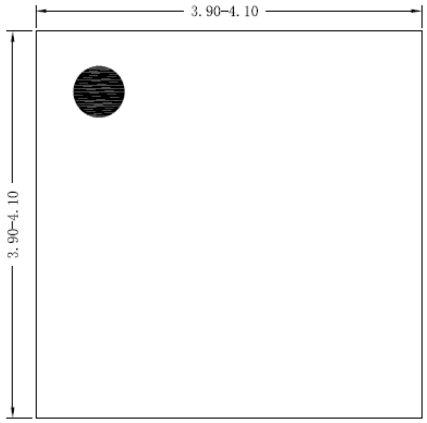


3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

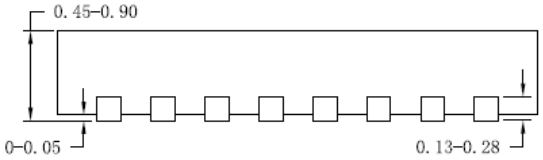
4) The capacitor C_{TIM} and the trace connecting to the TIM pin must not be adjacent to the LX net on the PCB layout to avoid the noise problem. It should be better to ground C_{TIM} to the output capacitor's ground.

5) In high current applications, a RC snubber circuit should be placed between LX and GND for better EMI.

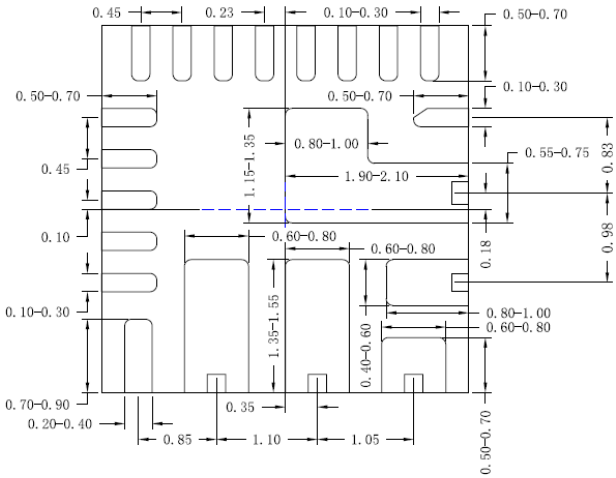
QFN4x4-20 Package Outline Drawing



Top View



Side View



Bottom View

Notes: **All dimension in MM and exclude mold flash & metal burr**

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